IBIS EBD for DDR2/DDR3 Module Board

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IBIS Summit

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Outline

- IBIS EBD
- DDR2/3 Topology Structures
- Challenges and Techniques for EBD
- Simulation Results using between board and EBD
- Conclusions

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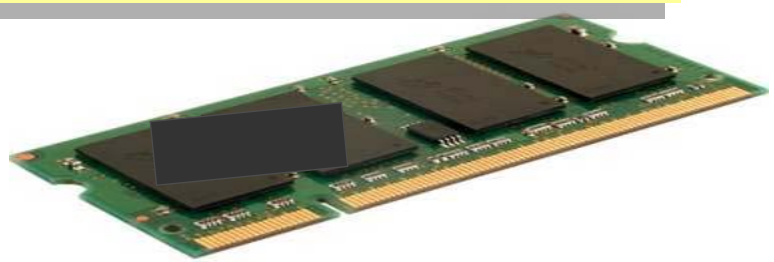
IBIS EBD

```
|================================================================
|================================================================
|
|                              Section 8
|
|          E L E C T R I C A L    B O A R D    D E S C R I P T I O
|
|================================================================
|================================================================
|
| A "board level component" is the generic term to be used to descr
| printed circuit board (PCB) or substrate which can contain compon
| even other boards, and which can connect to another board through
| user visible pins.  The electrical connectivity of such a board l
| component is referred to as an "Electrical Board Description".  F
| a SIMM module is a board level component that is used to attach s
| components on the PCB to another board through edge connector pin
| electrical board description file (a .ebd file) is defined to des
| connections of a board level component between the board pins and
| components on the board.
|
| A fundamental assumption regarding the electrical board descripti
| the inductance and capacitance parameters listed in the file are
| with respect to well-defined reference plane(s) within the board.
| this current description does not allow one to describe electrica
| (inductive or capacitive) coupling between paths.  It is recommen
| coupling is an issue, then an electrical description be extracted
| physical parameters of the board.
|
| What is, and is not, included in an Electrical Board Description
| by its boundaries.  For the definition of the boundaries, see the
| Description section under the [Path Description] Keyword.
|
| USAGE RULES:
|
| A .ebd file is intended to be a stand-alone file, not referenced by or
| or included in any .ibs or .pkg file.  Electrical Board Descriptions are
| stored in a file whose name looks like <filename>.ebd, where <filename> must
| conform to the naming rules given in the General Syntax Section of this
| specification.  The .ebd extension is mandatory.
|
| CONTENTS:
|
| A .ebd file is structured similar to a standard IBIS file.  It must contain
| the following keywords, as defined in the IBIS specification: [IBIS Ver],
| [File Name], [File Rev], and [End].  It may also contain the following
| optional keywords: [Comment Char], [Date], [Source], [Notes], [Disclaimer],
| and [Copyright].  The actual board description is contained between the
| keywords [Begin Board Description] and [End Board Description], and includes
| the keywords listed below:
```

A "board level component" is the generic term to be used to describe a printed circuit board (PCB) or substrate which can contain components or even other boards, and which can connect to another board through a set of user visible pins.



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IBIS EBD

|

[Path Description] Example_net

Pin J25

Len = 0.5 L=8.35n C=3.34p R=0.01 /

Node u21.3

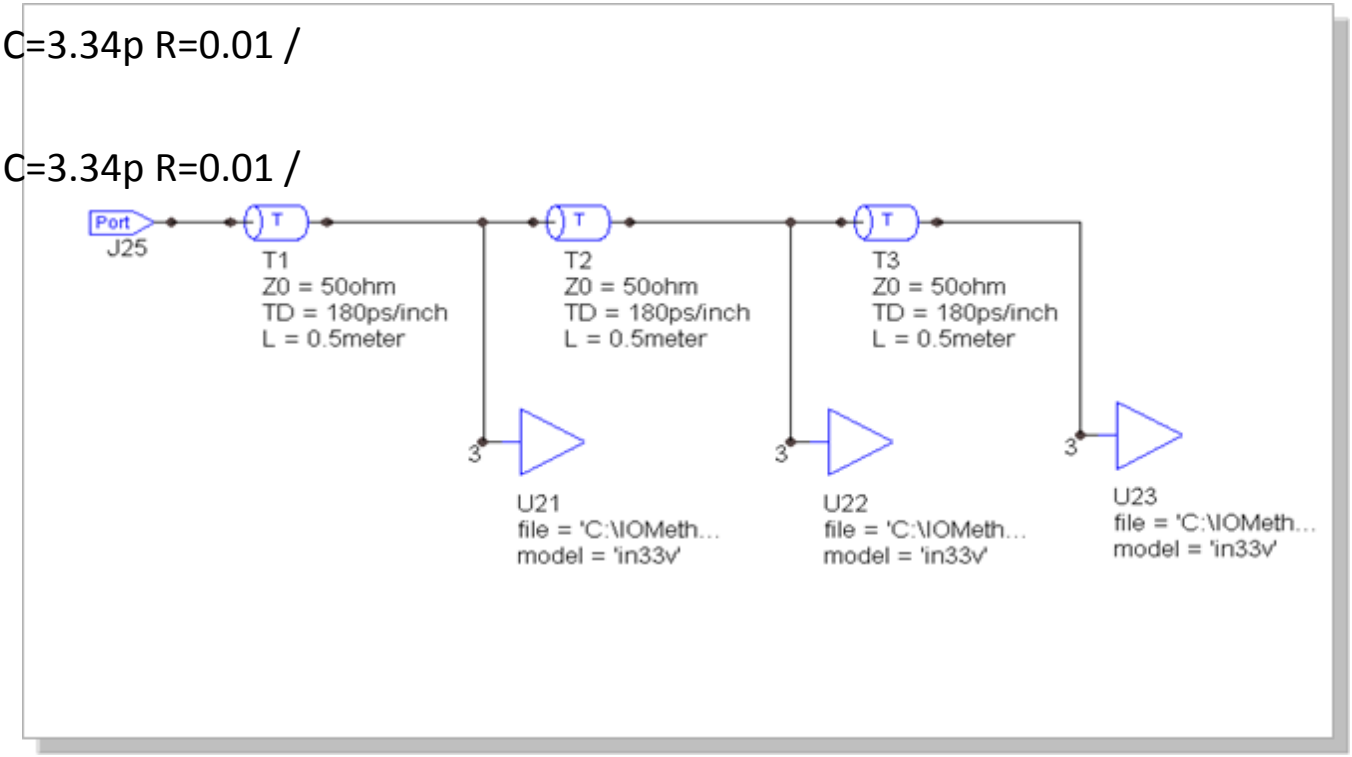
Len = 0.5 L=8.35n C=3.34p R=0.01 /

Node u22.3

Len = 0.5 L=8.35n C=3.34p R=0.01 /

Node u23.3

|



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DDR2/3 Topology Structure

- Point to Point
- Tree
- Fly-by

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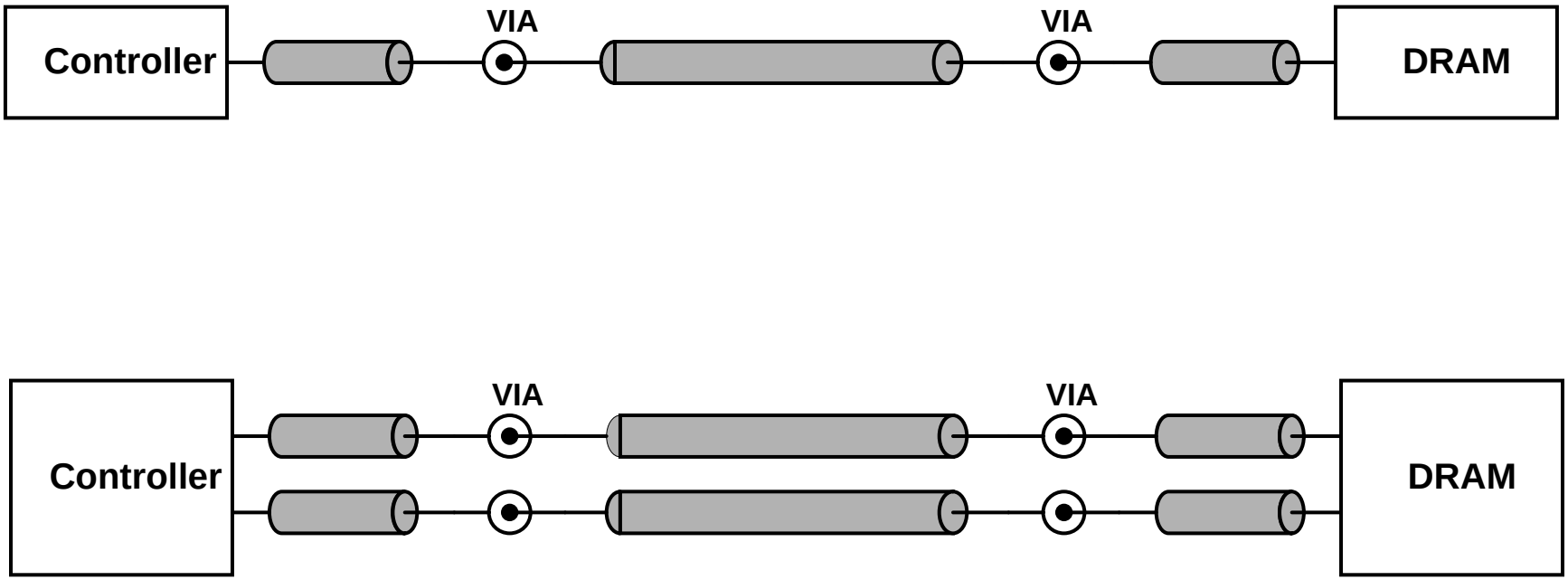
Point to Point
- DDR2/DDR3



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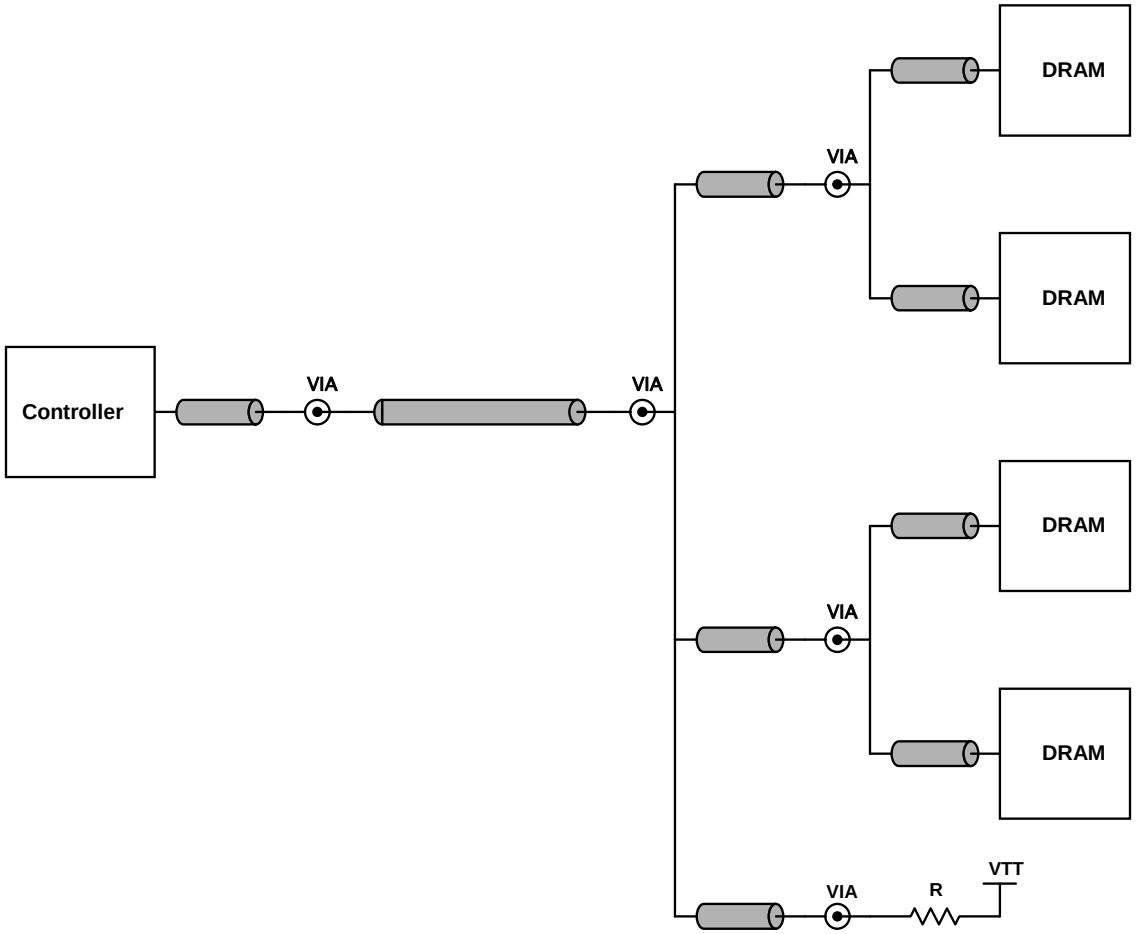
Tree (Single)

- DDR2 Address/Command



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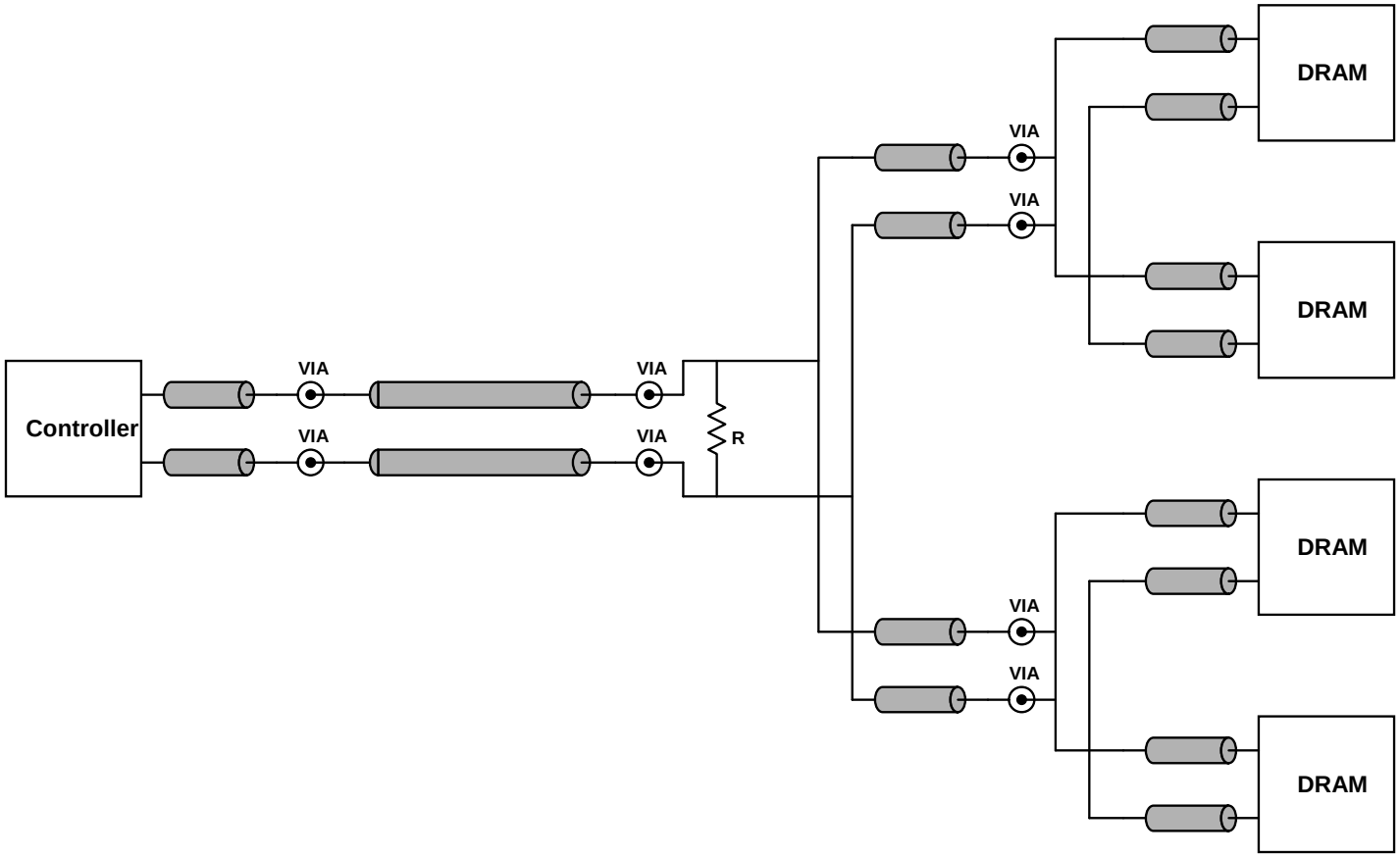
Tree (Differential)

- DDR2 Clock



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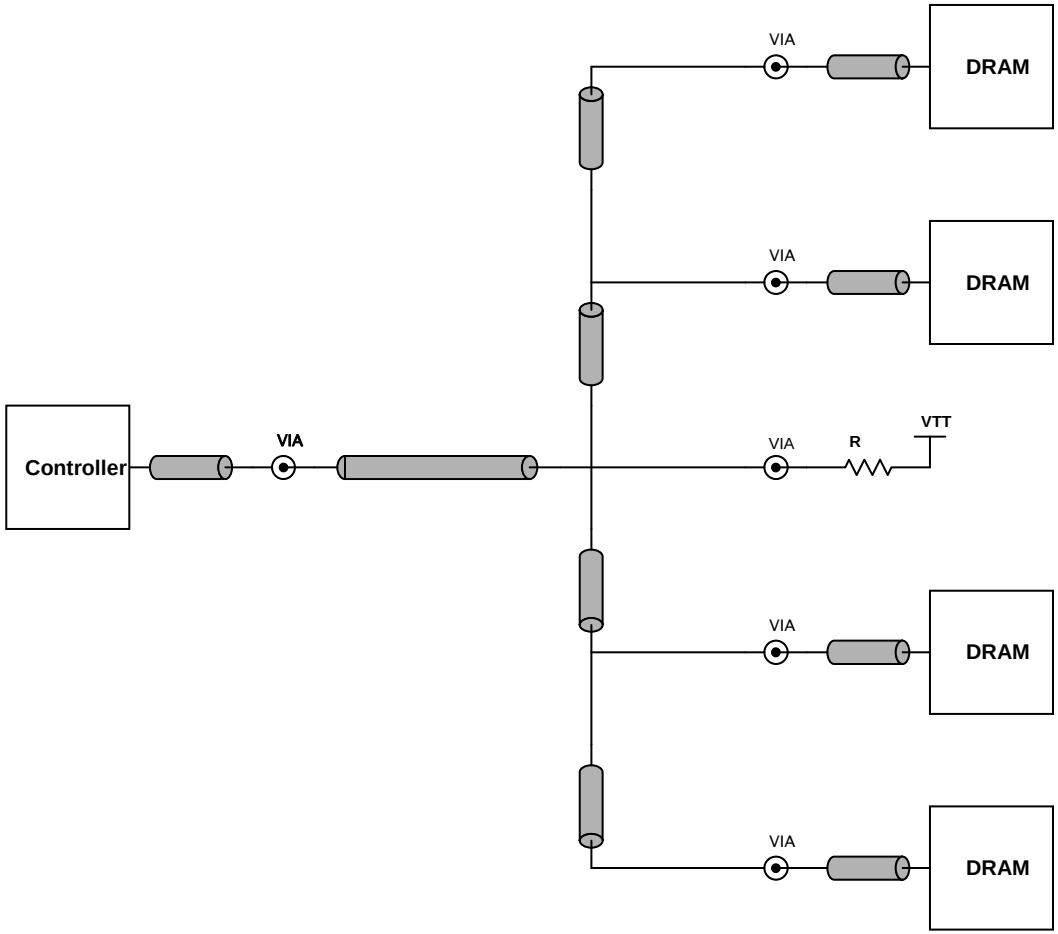
Hybrid Tree
- DDR2



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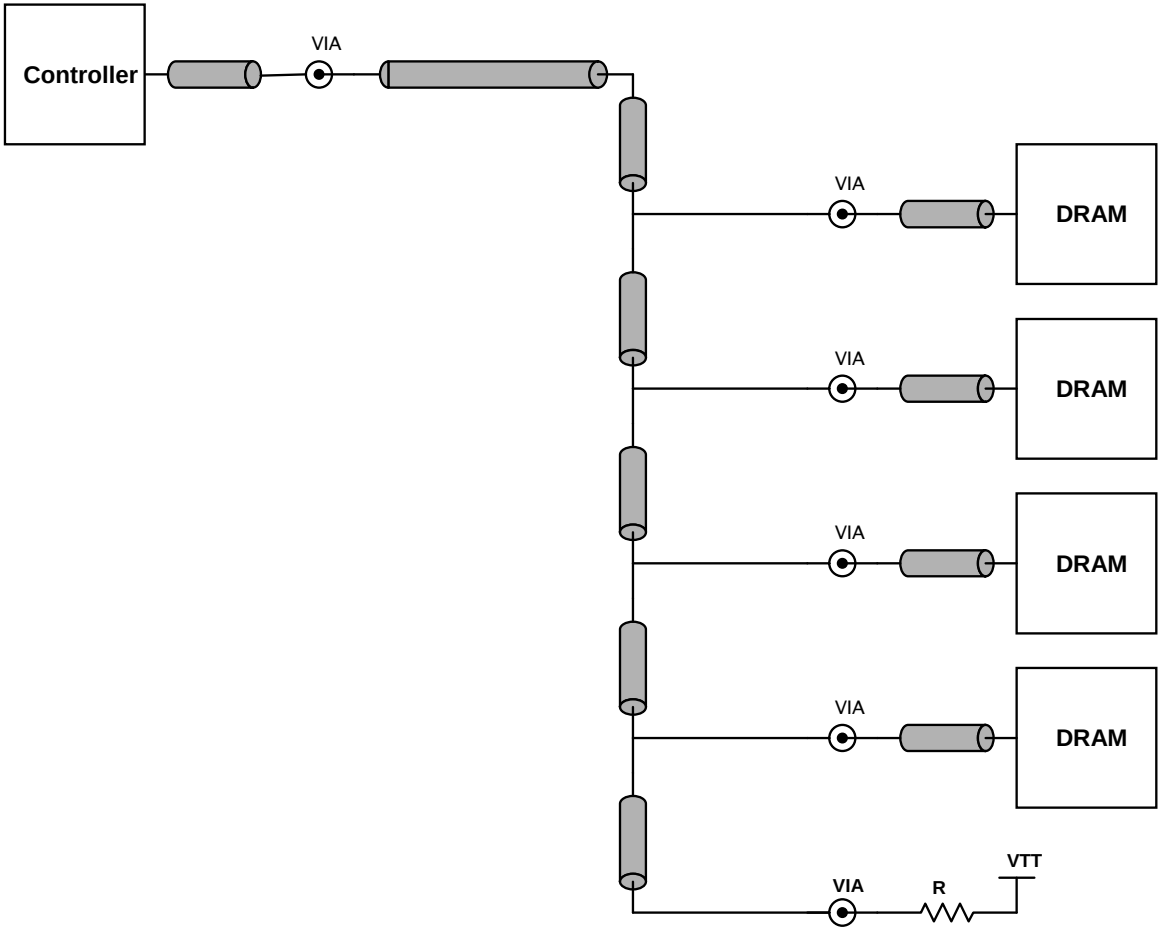
Fly-by (Daisy Chain)

- DDR3 Address/Command



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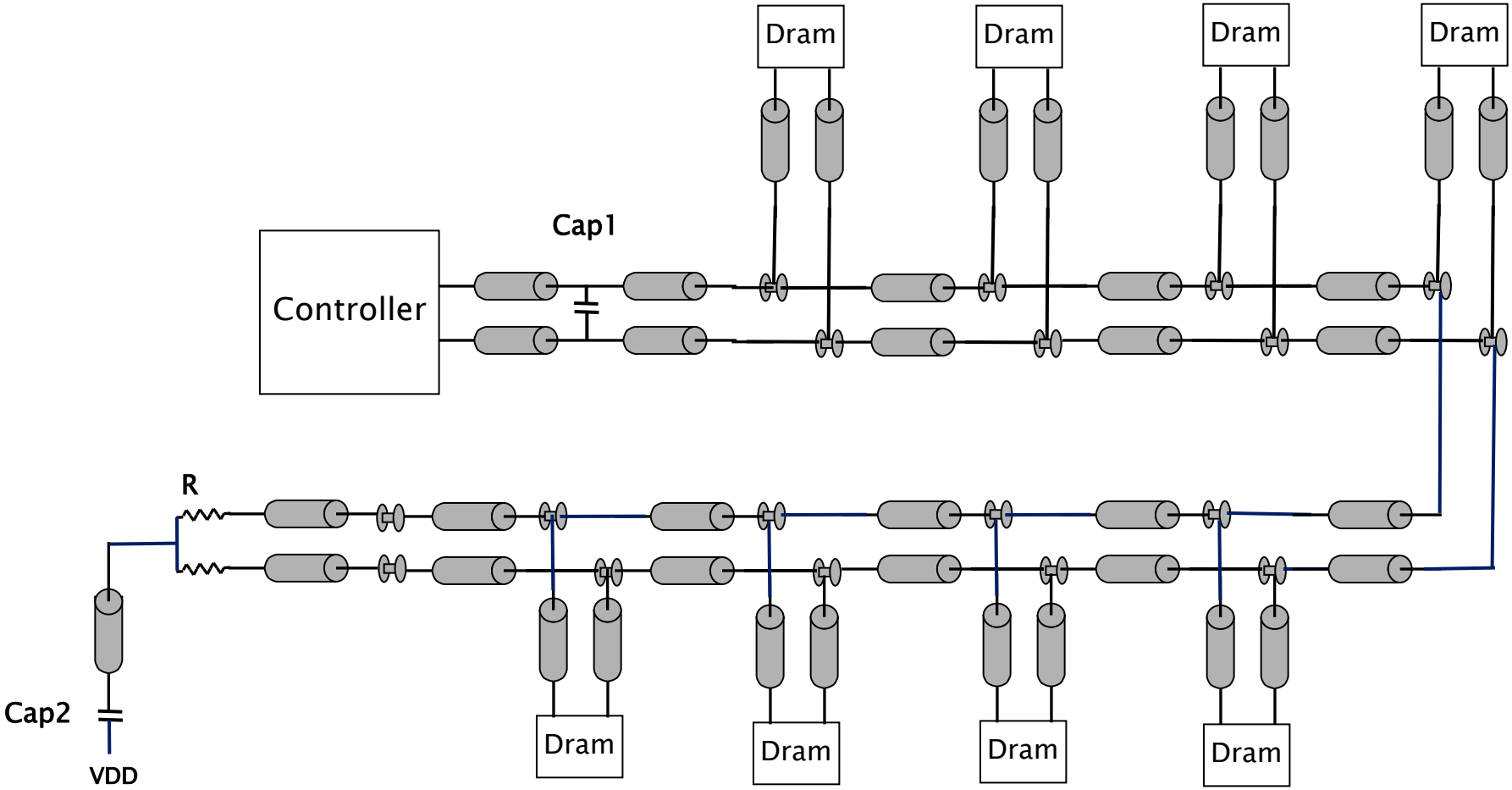
Fly-by
- DDR3 Clock



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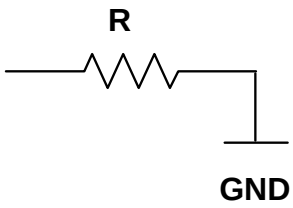
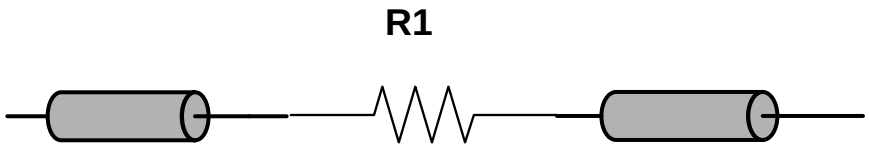
Challenges and Techniques for EBD

Len=0.00329534 L=3.5639e-007 C=1.0568e-010 R=3.7292e+000/



C, L can use the same methodology

Len=0 L=0.0000e+000 C=0.0000e+000 R=60/



Len=0.00329534 L=3.5639e-007 C=1.0568e-010 R=3.7292e+000/

R1.1 -> R1.2 R=13

Len=0 R=13/

Len=0.00329534 L=3.5639e-007 C=1.0568e-010 R=3.7292e+000/

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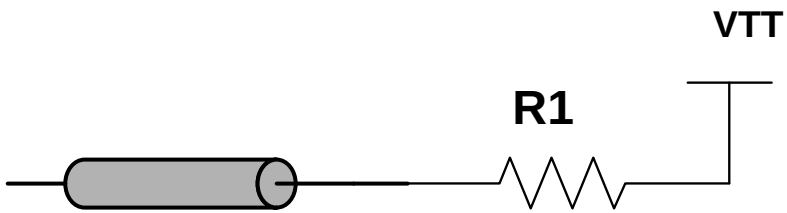
Challenges and Techniques for EBD



Len=0.00329534 L=3.5639e-007 C=1.0568e-010 R=3.7292e+0
Pin R1.1
……
R1 terminators.ibs R_Term_VTT

```
[Component]    R_Term_VTT
[Manufacturer] Created by EBConverter

[Package]
|                typ          min          max
R_pkg            0            NA           NA
L_pkg            0            NA           NA
C_pkg            0            NA           NA
|
[Pin]            signal_name  model_name
1                signal       NC
2                signal       P_VTT
[Series Pin Mapping]  pin_2     model_name
1                     2         series_r39
```

```
[Model]  P_VTT
Model_type  Terminator
|                              typ          min          max
C_comp                         0            NA           NA
[Pullup Reference]             0.9          NA           NA
[Pulldown Reference]           0            NA           NA
[POWER Clamp Reference]        0.9          NA           NA
[GND Clamp Reference]          0            NA           NA
| variable                     typ          min          max
[Rpower]                       0            NA           NA
```

```
[Model]  series_r39
Model_type  Series
|                              typ          min          max
C_comp                         0            NA           NA
[Pullup Reference]             0            NA           NA
[Pulldown Reference]           0            NA           NA
[POWER Clamp Reference]        0            NA           NA
[GND Clamp Reference]          0            NA           NA
| variable     typ          min          max
[R Series]     39           NA           NA
```

C, L can use the same methodology

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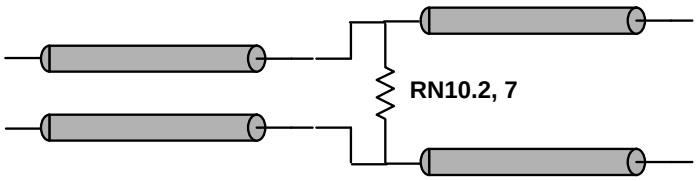
Challenges and Techniques for EBD



Make sure to put both nets in the same [Path Description]

```
! Net CLK_P
Pin 170
.....
Len=0.00329534 L=3.5639e-007 C=1.0568e-010 R=3.7292e+000/
| RN10.2 -> RN10.7 R=13
Len=0  R=13/
| Net: CLK_N
Len=0.00182395 L=3.5639e-007 C=1.0568e-010 R=3.7292e+000/
.....
Pin 171
```

BIRD 111.1 describes another method

C, L can use the same methodology

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Simulation Results using between board and EBD

- BRD Files:
  - PC3-10600-UDIMM-V0_50_RC_Cx_20070530.brd (DDR3)
  - PC2-6400_RDIMM_V330_RC_R0_20060505.brd (DDR2)
- Corner:
  - typical
- Data Rate
  - 800, 1067Mbps

  (A#=400, 533MHz, DQ#=400, 533MHz, CK#=400, 533MHz)
- Simulator:
  - Cadence PCB SI

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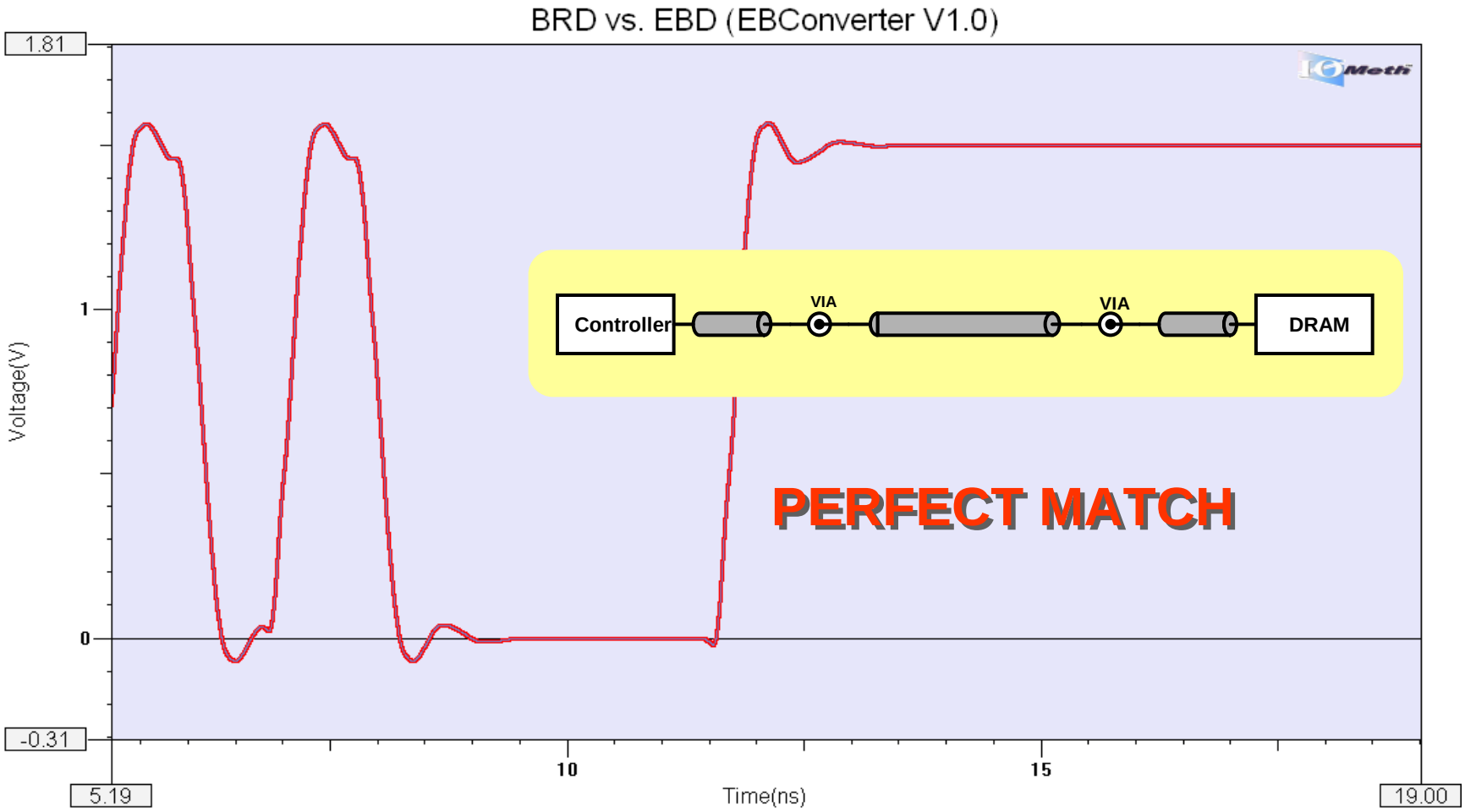
Net: DQ# @ U1
Timing:0.002ps @750mv DPI: 0.00% DAI: 0.00%



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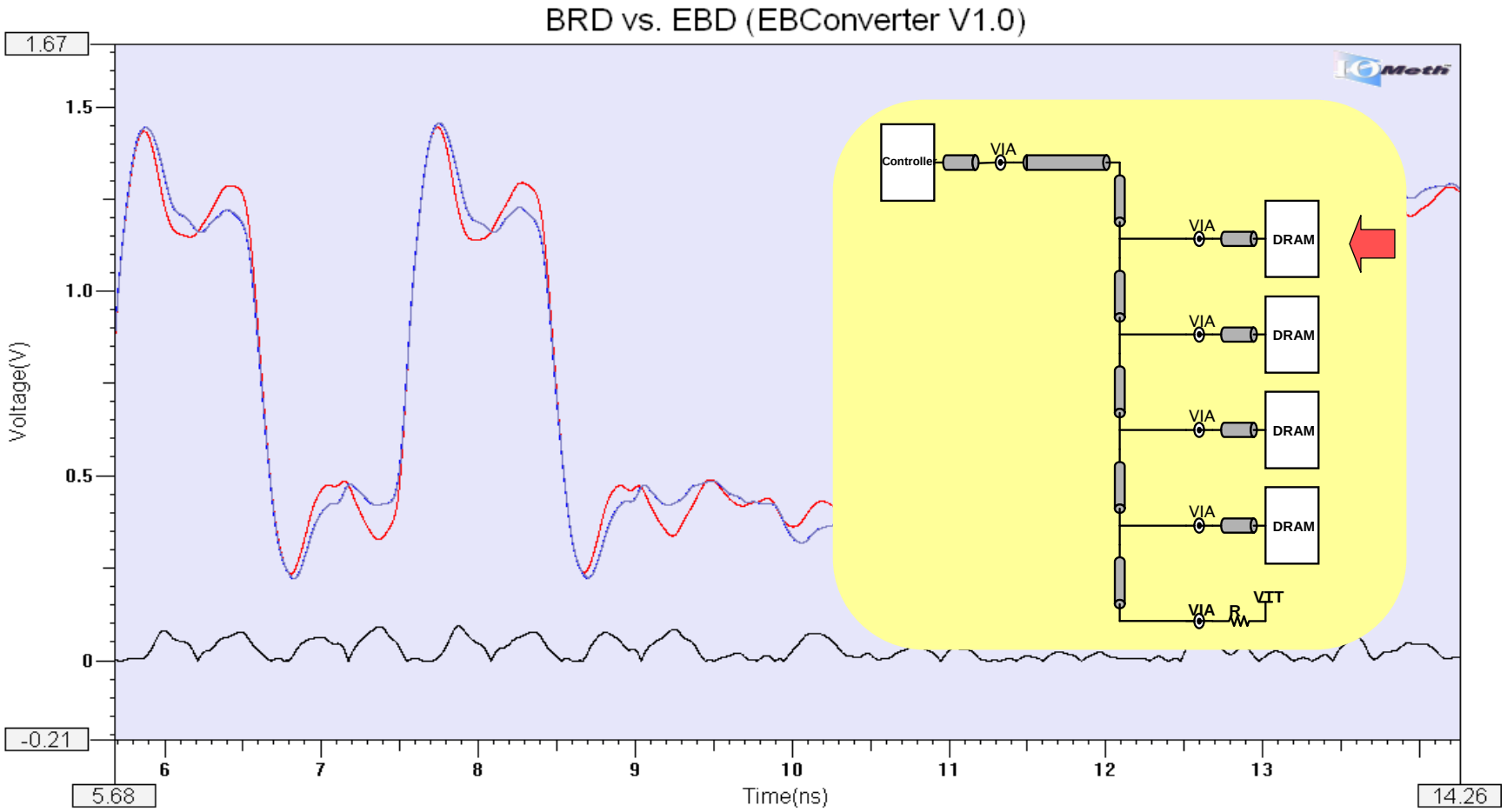
A# @ U1
Timing: -2.5ps @800mv DPI: 7.87% DAI: 2.58%



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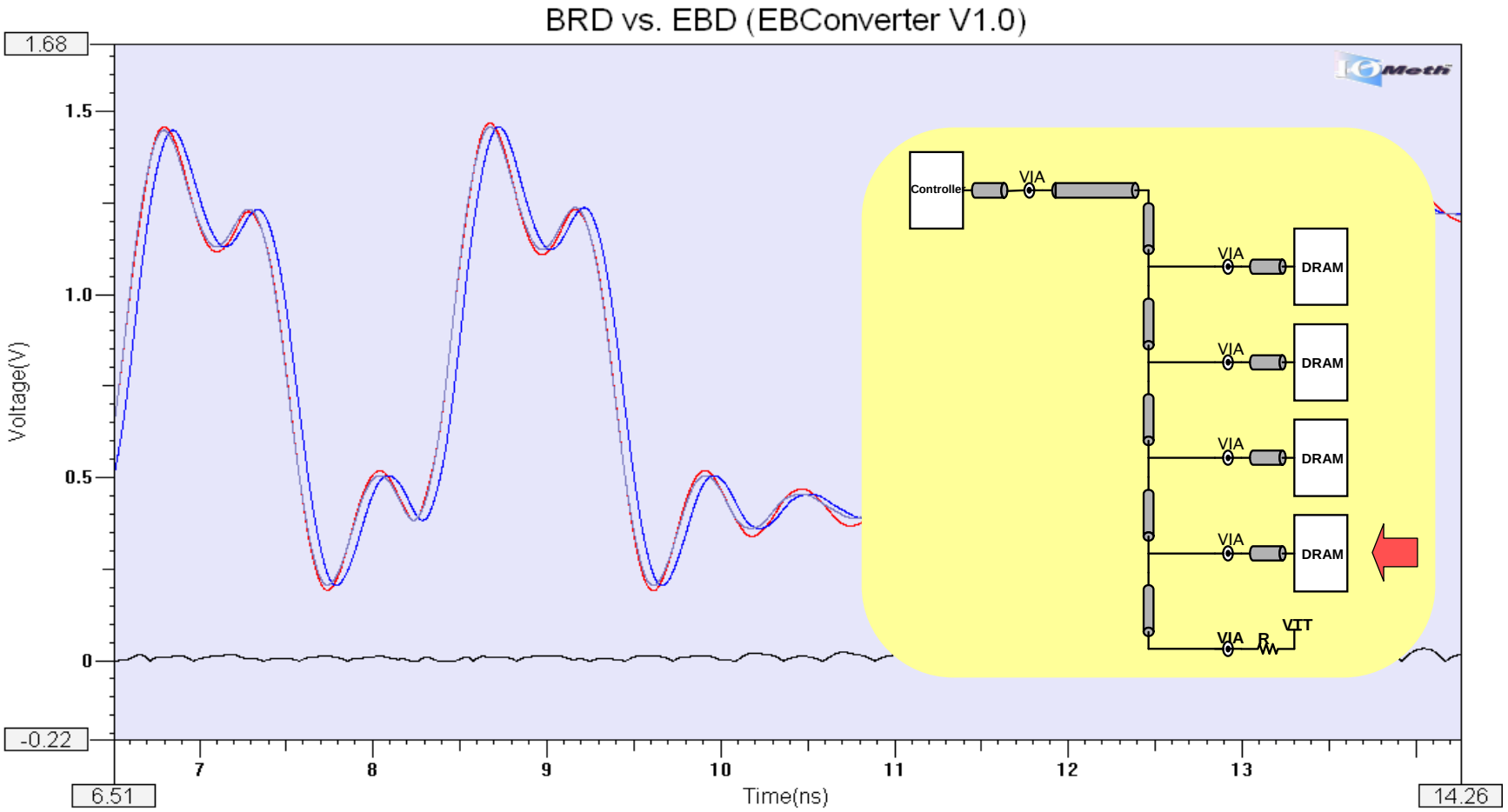
A# @ U4
Timing:51ps @800mv DPI: 2.67% DAI: 0.86%



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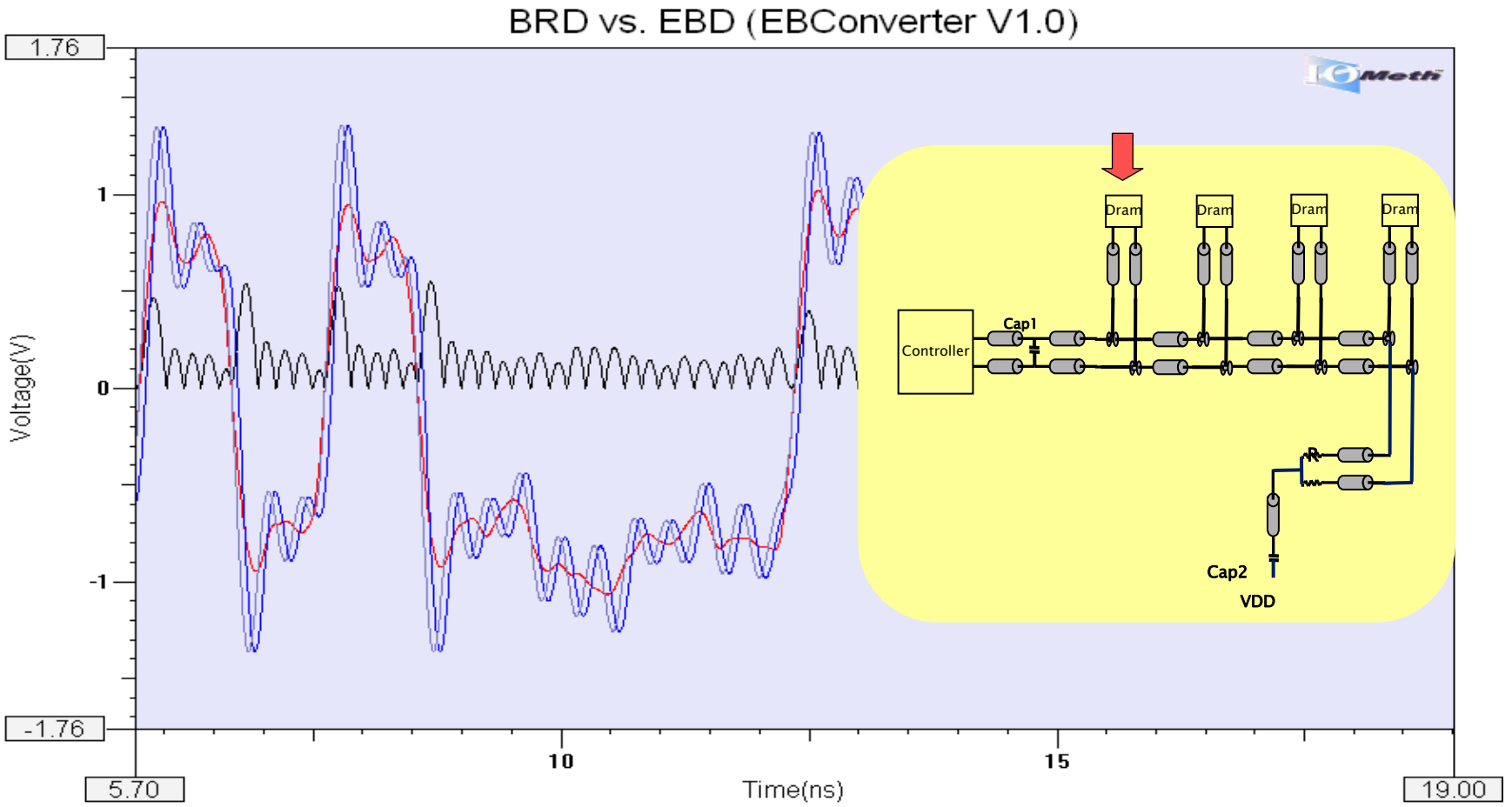
CK#/CK#_ @ U1
Timing:66ps @0v DPI: 26.63% DAI: 5.60%



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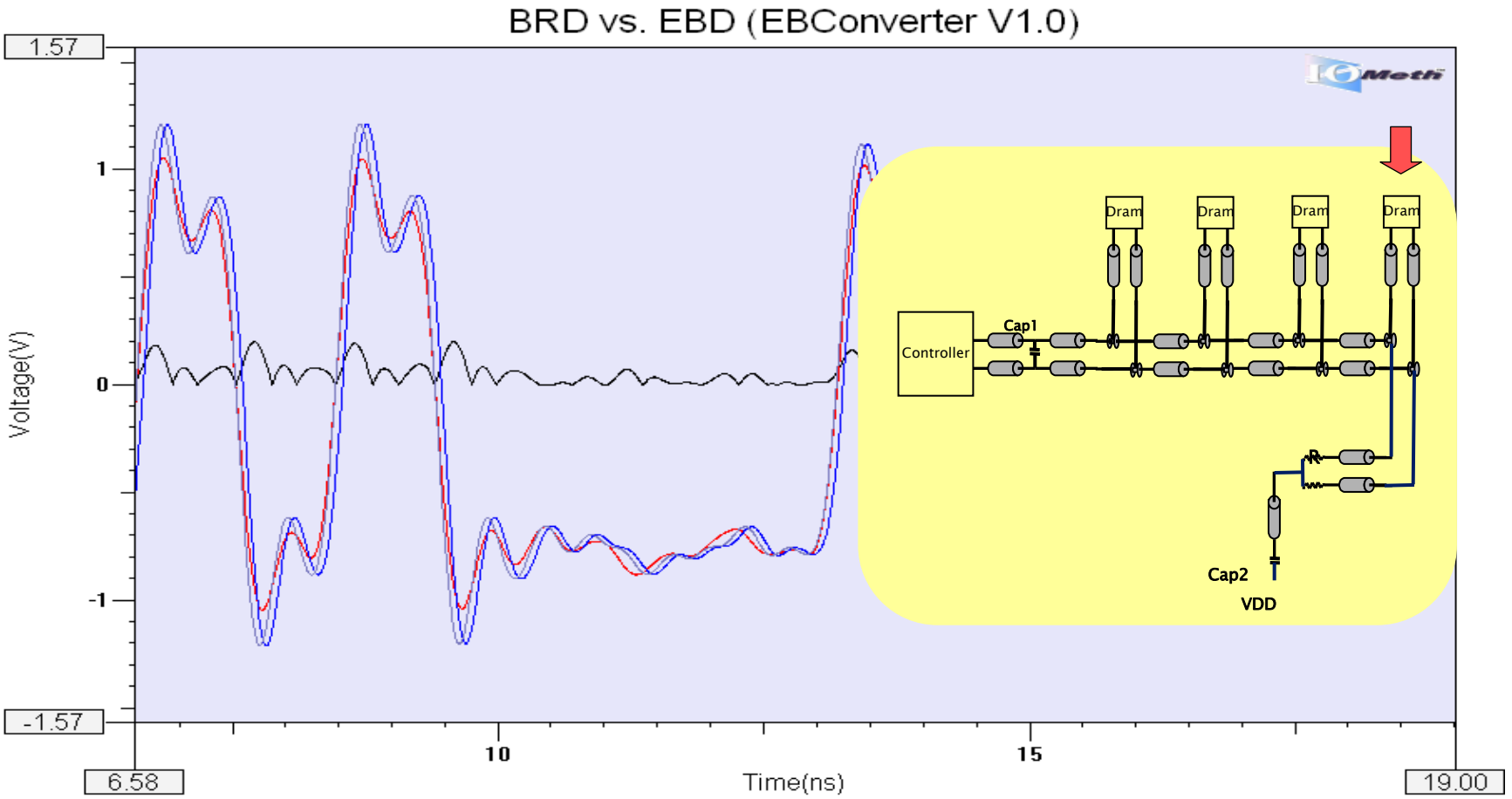
CK#/CK#_ @ U4
Timing:63ps @0v DPI: 9.57% DAI: 1.86%



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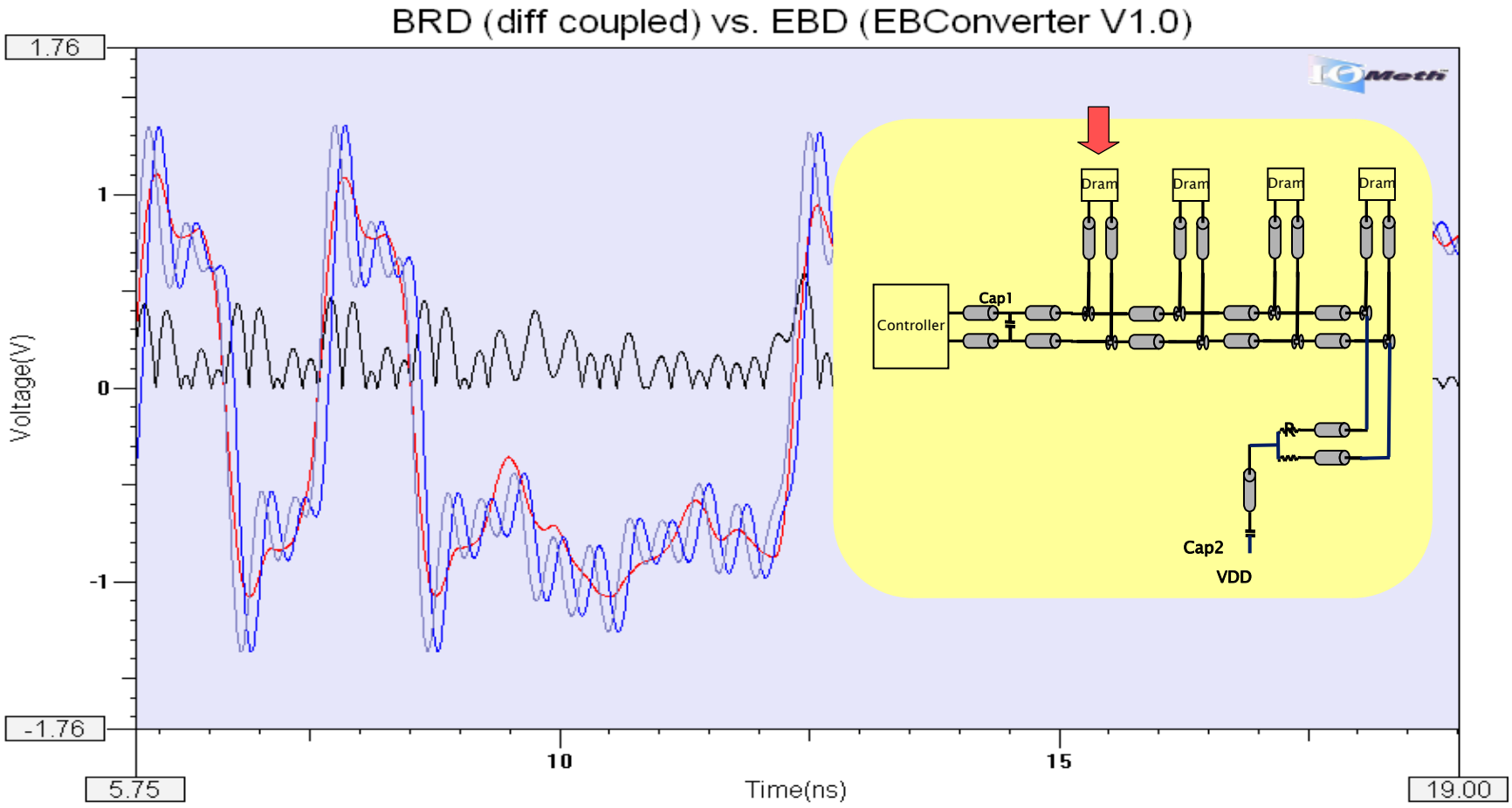
CK#/CK#_ @ U1 (Diff Coupled)
Timing:101ps @0v DPI: 27.35% DAI: 6.23%



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Conclusions

- EBD provides a secure and interoperable way for DDR2/3 modules in the high-speed memory market
- It is accepted by the most of EDA software now
- Needs to be careful to model EBD using correct method
- Good for point-to-point, Tree structure topologies
- Good Signal Quality for Fly-By structure, not good for Timing (Single-end)
- Acceptable Signal Quality for Fly-By structure, not good for Timing (Differential)
  - Signal Quality might also effected by timing on reflections
- Two new elements needs to be added:
  - Delay/Lossy Element
    - Adding frequency-dependent Rs, Gd elements into RLC (easy to convert from W-element like lossy transmission line syntax)
  - Coupling Element
    - Mutual Capacitance

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