IBIS EBD for DDR2/DDR3 Module Board

Lance Wang
(lwang@iometh.com)
IBIS Summit
DesignCon 2009
February 5th, 2009
Outline

- IBIS EBD
- DDR2/3 Topology Structures
- Challenges and Techniques for EBD
- Simulation Results using between board and EBD
- Conclusions
A "board level component" is the generic term to be used to describe a printed circuit board (PCB) or substrate which can contain components or even other boards, and which can connect to another board through a set of user visible pins. The electrical connectivity of such a board level component is referred to as an "Electrical Board Description".

A SJKX file is a board level component that is used to attach components on the PCB to another board through edge connector pins. The electrical board description file (or .ebd file) is defined to describe connections of a board level component between the board pins and components on the board.

A fundamental assumption regarding the electrical board description is that the inductance and capacitance parameters listed in the file are with respect to well-defined reference plane(s) within the board. This current description does not allow one to describe electrical (inductive or capacitive) coupling between paths. If in common coupling is an issue, then an electrical description be extracted from physical parameters of the board.

What is, and is not, included in an Electrical Board Description by the boundaries. For the definition of the boundaries, see the Description section under the [Path Description] Keyword.

**RULES:**

A .ebd file is intended to be a stand-alone file, not referenced by or included in any .ibs or .pkg file. Electrical Board Descriptions are stored in a file whose name looks like <filename>.ebd, where <filename> must conform to the naming rules given in the General Syntax Section of this specification. The .ebd extension is mandatory.

**CONTENTS:**

A .ebd file is structured similar to a standard IBIS file. It must contain the following keywords, as defined in the IBIS specification: [IBIS Ver], [File Name], [File Rev], and [End]. It may also contain the following optional keywords: [Comment Char], [Date], [Source], [Notes], [Disclaimer], and [Copyright]. The actual board description is contained between the keywords [Begin Board Description] and [End Board Description], and includes the keywords listed below:

**IBIS EBD**

Copyright © 2006-2009
IO Methodology Inc.
[Path Description] Example_net
Pin J25
Len = 0.5 L=8.35n C=3.34p R=0.01 /
Node u21.3
Len = 0.5 L=8.35n C=3.34p R=0.01 /
Node u22.3
Len = 0.5 L=8.35n C=3.34p R=0.01 /
Node u23.3
DDR2/3 Topology Structure

- Point to Point
- Tree
- Fly-by
Point to Point
- DDR2/DDR3
Tree (Single)
- DDR2 Address/Command
Tree (Differential)
- DDR2 Clock
Hybrid Tree
- DDR2
Fly-by (Daisy Chain) - DDR3 Address/Command
Fly-by
- DDR3 Clock
Challenges and Techniques for EBD

C, L can use the same methodology

Len=0.00329534 L=3.5639e-007 C=1.0568e-010 R=3.7292e+000/

Len=0 L=0.0000e+000 C=0.0000e+000 R=60/

Len=0.00329534 L=3.5639e-007 C=1.0568e-010 R=3.7292e+000/

| R1.1 -> R1.2 R=13
Len=0 R=13/
Len=0.00329534 L=3.5639e-007 C=1.0568e-010 R=3.7292e+000/
Challenges and Techniques for EBD

Len=0.00329534 L=3.5639e-007 C=1.0568e-010 R=3.7292e+000
Pin R1.1
......
R1 terminators.ibs R_Term_VTT

C, L can use the same methodology
Challenges and Techniques for EBD

Make sure to put both nets in the same [Path Description]

BIRD 111.1 describes another method

C, L can use the same methodology

! Net CLK_P
Pin 170
......
Len=0.00329534 L=3.5639e-007 C=1.0568e-010 R=3.7292e+000/
| RN10.2 -> RN10.7 R=13
Len=0  R=13/
| Net: CLK_N
Len=0.00182395 L=3.5639e-007 C=1.0568e-010 R=3.7292e+000/
......
Pin 171
Simulation Results using between board and EBD

- **BRD Files:**
  - PC3-10600-UDIMM-V0_50_RC_Cx_20070530.brd (DDR3)
  - PC2-6400_RDIMM_V330_RC_R0_20060505.brd (DDR2)

- **Corner:**
  - typical

- **Data Rate**
  - 800, 1067Mbps
    - \( A\# = 400, 533\text{MHz} \), \( DQ\# = 400, 533\text{MHz} \), \( CK\# = 400, 533\text{MHz} \)

- **Simulator:**
  - Cadence PCB SI
Net: DQ# @ U1
Timing: 0.002ps @ 750mv DPI: 0.00% DAI: 0.00%

PERFECT MATCH
A# @ U1
Timing: -2.5ps @800mv DPI: 7.87% DAI: 2.58%
A# @ U4
Timing: 51ps @ 800mv DPI: 2.67% DAI: 0.86%
CK#/CK# @ U1
Timing: 66ps @ 0v DPI: 26.63% DAl: 5.60%
CK#/CK#_ @ U4
Timing: 63ps @0v DPI: 9.57% DAI: 1.86%
CK#/CK#_ @ U1 (Diff Coupled)
Timing: 101ps @ 0v DPI: 27.35% DAI: 6.23%
Conclusions

- EBD provides a secure and interoperable way for DDR2/3 modules in the high-speed memory market
- It is accepted by the most of EDA software now
- Needs to be careful to model EBD using correct method
- Good for point-to-point, Tree structure topologies
- Good Signal Quality for Fly-By structure, not good for Timing (Single-end)
- Acceptable Signal Quality for Fly-By structure, not good for Timing (Differential)
  - Signal Quality might also effected by timing on reflections
- Two new elements needs to be added:
  - Delay/Lossy Element
    - Adding frequency-dependent Rs, Gd elements into RLC (easy to convert from W-element like lossy transmission line syntax)
  - Coupling Element
    - Mutual Capacitance
The High-Speed Design Utility Tool and Service Provider
www.iometh.com