SI/PI Co-Analysis and Linearity Indicator

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Acknowledgements:
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Agenda

- Need for SI/PI Co-analysis
- Ingredients for SI/PI analysis
- Controllable/ Uncontrollable Parameters
- Different Cases and Decomposition
- Linearity Indicator
- Summary

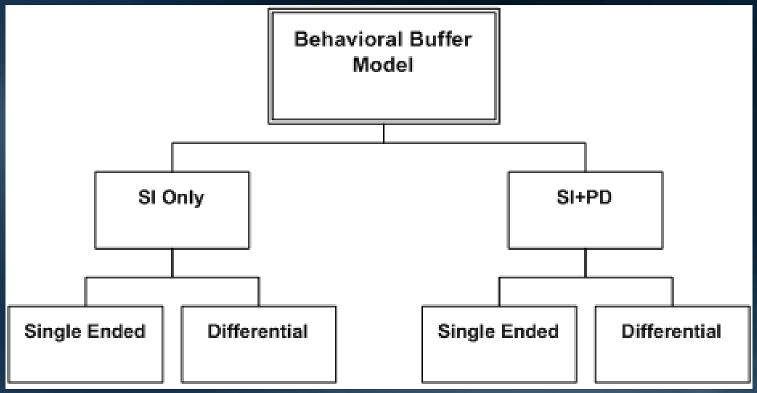
Need for SI/PI Co-analysis

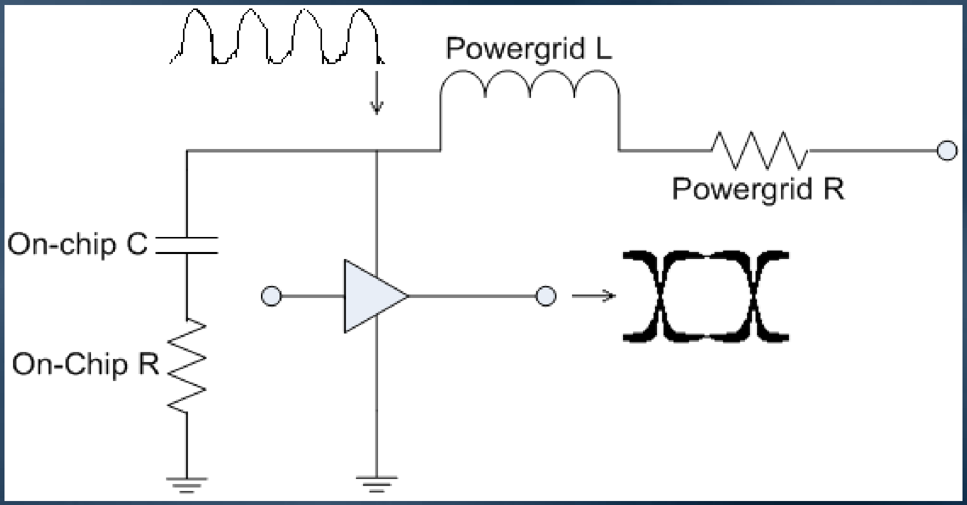
- There are 3 major noise sources in the channel analysis
  - Crosstalk, ISI, and SSO
- SI Only: Crosstalk and ISI; PI only: SSO
- For high speed low cost systems the separate analysis is not sufficient
  - Second and third order effects become prominent.
- SI/PI co-analysis is becoming increasingly important.

SI/PI steps

- Model Generation
  - Passive Models
    - PCB, Package, on-chip: 2D/ 3D EM Models
  - Buffer Models: PD info in Buffer models
- Power Grid Models
- Pattern Generation
- Full time domain simulations
  - Different cases for identifying 2^{nd}/ 3^{rd} order effects
- Controllable parameters and their variations

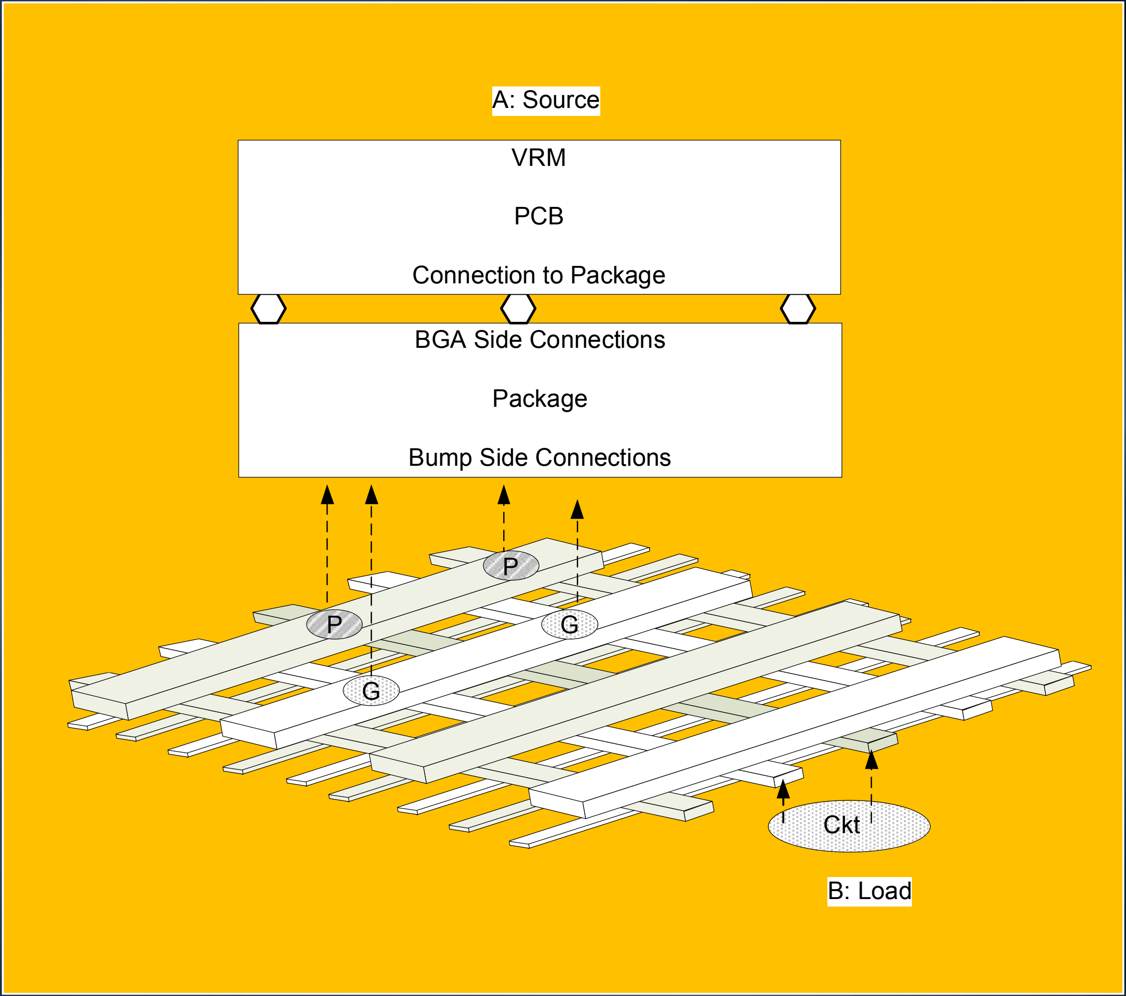
IBIS SSO Simulation





Simplified On-chip Power Grid and On-chip PDN Capacitor with Buffer Connection and PDN noise impact on eye jitter

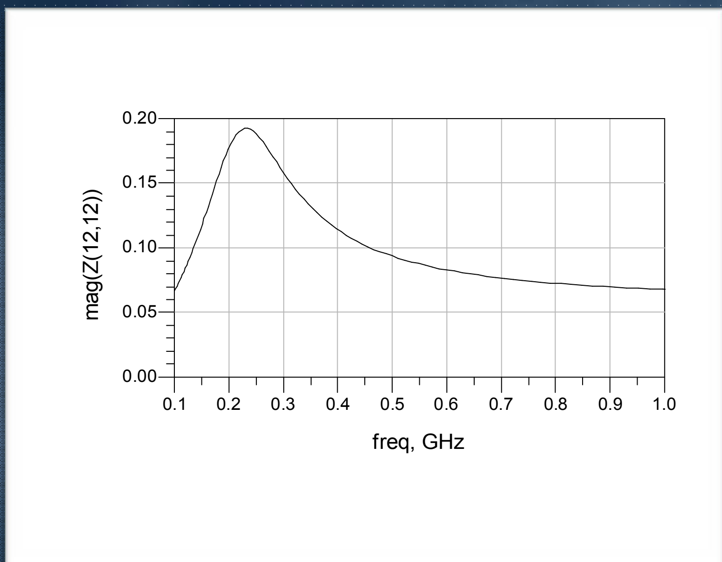
End to End PDN model



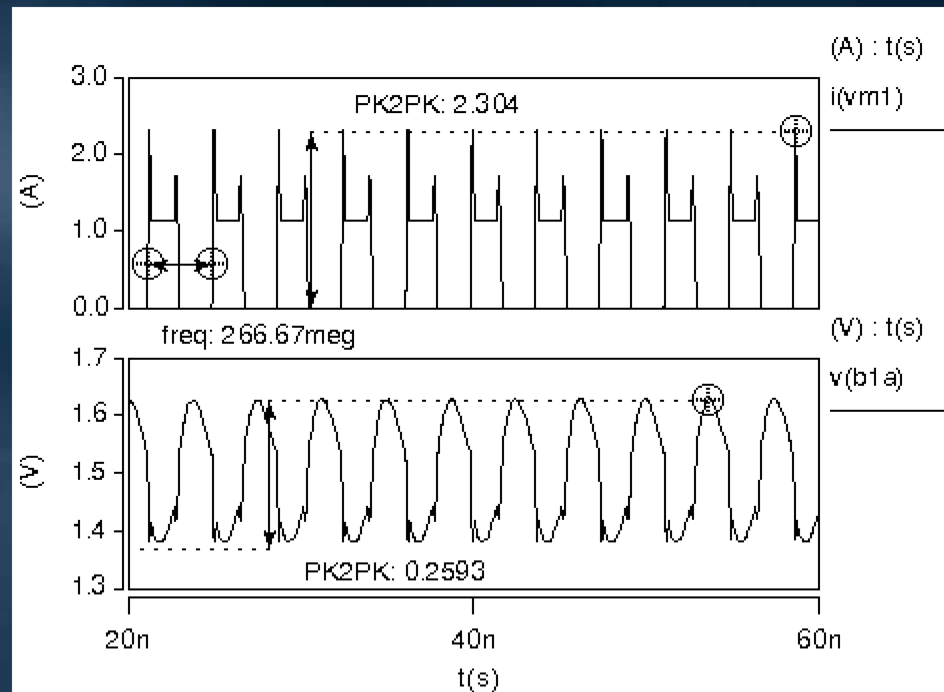
- PDN Model
  - Grid, Pkg, PCB
- It needs to be with the SI channel models
- Coupling between power and signal needs to be considered during the modeling
  - reference transition
  - via coupling, etc.

Example: PDN Response

Z11 profile at the Power node of Driver



Simulated Noise at the Power node of Driver



- PDN Noise analysis determines the noise at different data rates. This noise gets coupled to signals at the chip level.
- Interconnect impact needs to be determined by SI/PI analysis

SI/PI Parameters

Examples	SI/PI Controllable Variables	SI/PI Uncontrollable Variables
Silicon	Ron, Slew rate, ODT, PDcap and Rdamp, Bumpout, I/O & EQ scheme, Power Grid Routing	I/O count, I/O device capacitor Unintentional PD Cap, Integrated passive element tolerances, Silicon process variations
Package/socket	Trace width and spacing between lines, Pin-map, Referencing scheme	I/O pincount, Package manufacturing tolerances, Passive element tolerances, Stackup parameters (dielectric height and constant), Limited signal trace width and spacing
PCB	Trace width and spacing between lines, Rtt, Interconnect topology, Rs in memory channel, Referencing scheme	PCB manufacturing tolerances, passive element tolerances, Stackup parameters (dielectric height and constant), Limited signal trace width and spacing
DIMM/Connector	Trace width and spacing between lines, Connector pin-map, Rtt, Interconnect topology, Stub resistor (Rstub), Referencing scheme	Total I/O pincount, PCB manufacturing tolerances, Passive element tolerances, Stackup parameters (dielectric height and constant), Limited signal trace width and spacing

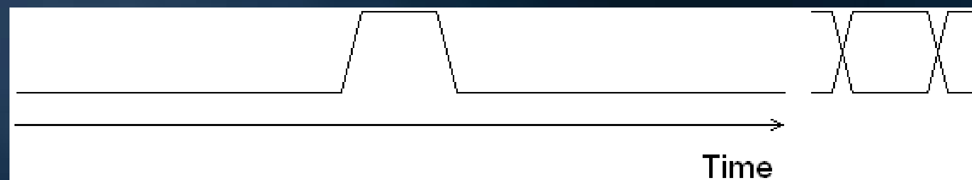
Different Cases

- Combination of different cases can be run for SI/PI co-analysis
- Response Decomposition can be performed

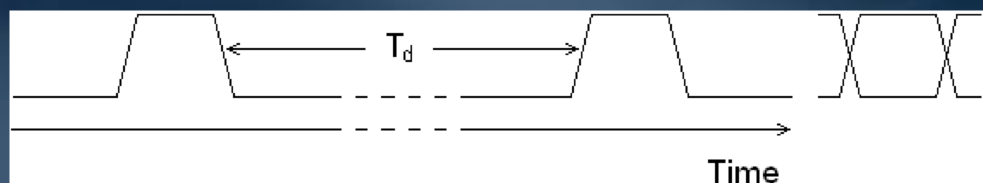
Forced Stimulus Setups for SI-PI Co-simulation				
	Case #	ISI	Cross-talk	SSO
ISI	1	Minimal	Minimal	Minimal
	2	Yes	Minimal	Minimal
SSO, ISI	3	Minimal	Minimal	Yes
	4	Yes	Minimal	Yes
Cross-talk, ISI	5	Minimal	Yes	Minimal
	6	Yes	Yes	Minimal
Cross-talk, ISI, SSO	7	Minimal	Yes	Yes
	8	Yes	Yes	Yes

Minimal ISI Implementation

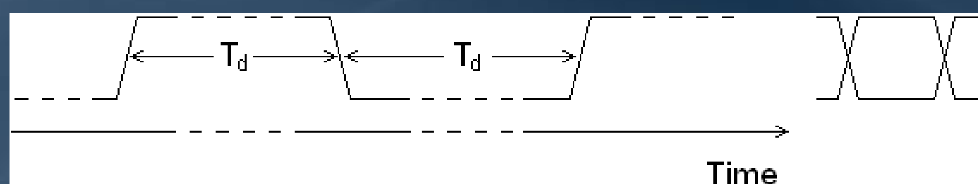
Construction of ISI needs only one or more rising and falling edge.



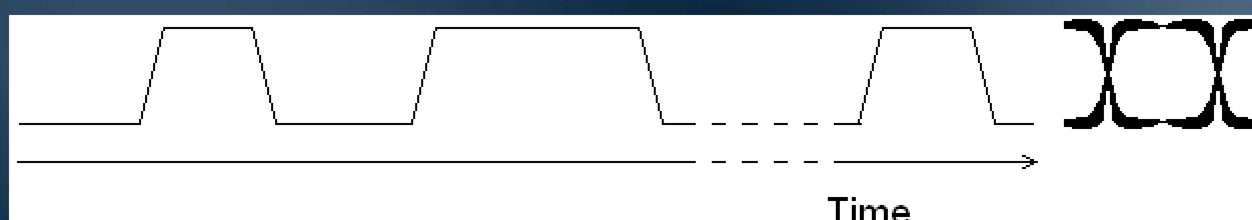
A lone bit excitation of ISI node for minimal ISI Eye construction by wrapping the waveform twice in time domain for the UI



Delayed bits excitation of ISI node for minimal ISI Eye construction

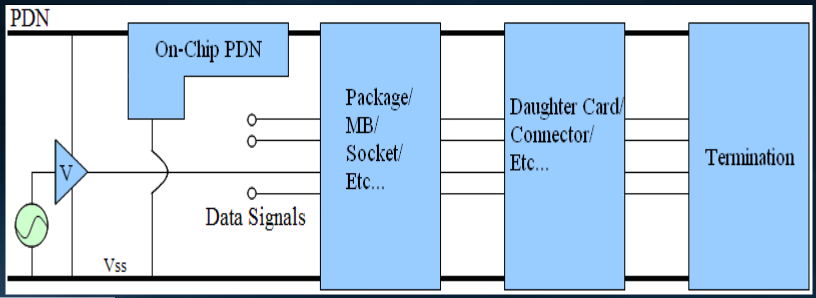


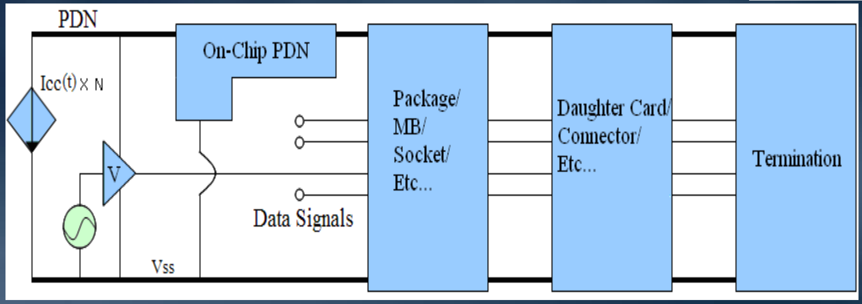
Delayed transition excitation of ISI node for minimal ISI Eye construction



SI/PI Simulation Cases

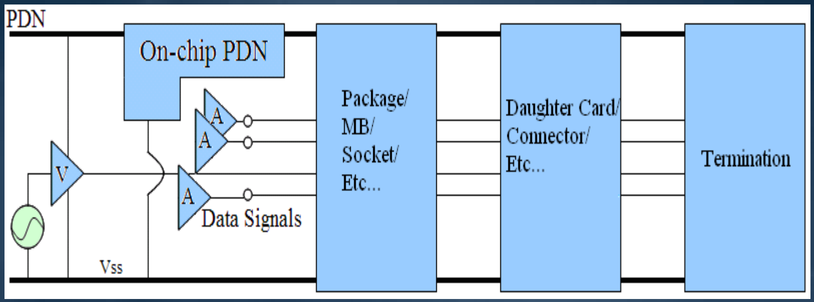
- Minimal ISI only

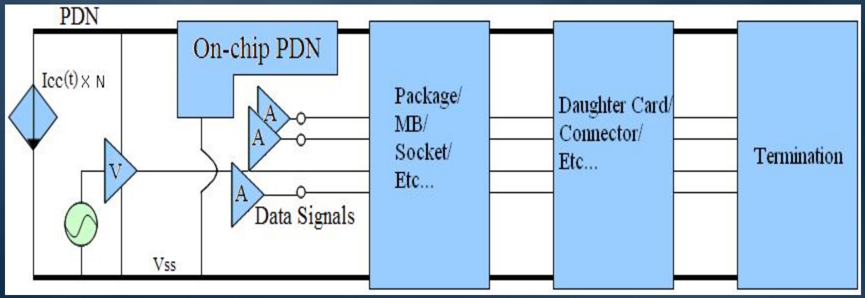




❑ **ISI and SSO**

❑ **ISI and Xtalk**



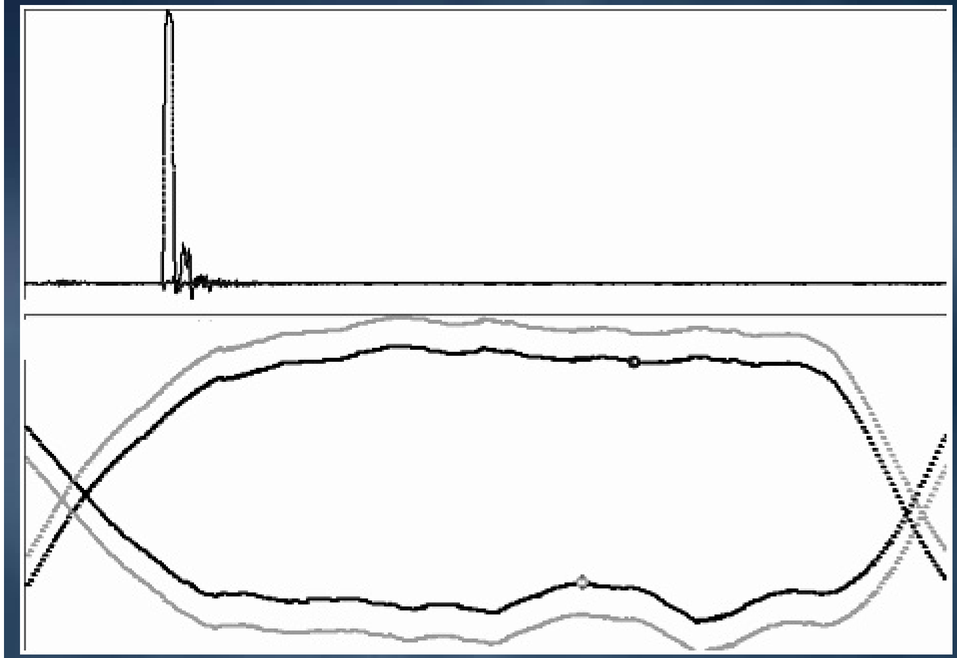


❑ **ISI, Xtalk, SSO**

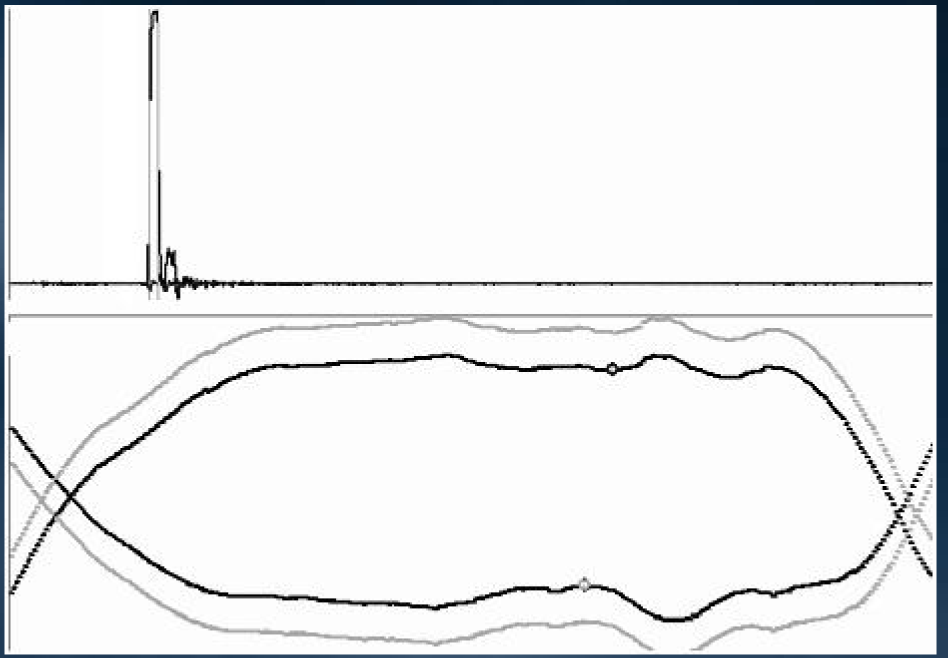
SE WC Results Example

PDA Results

uStrip



Strip

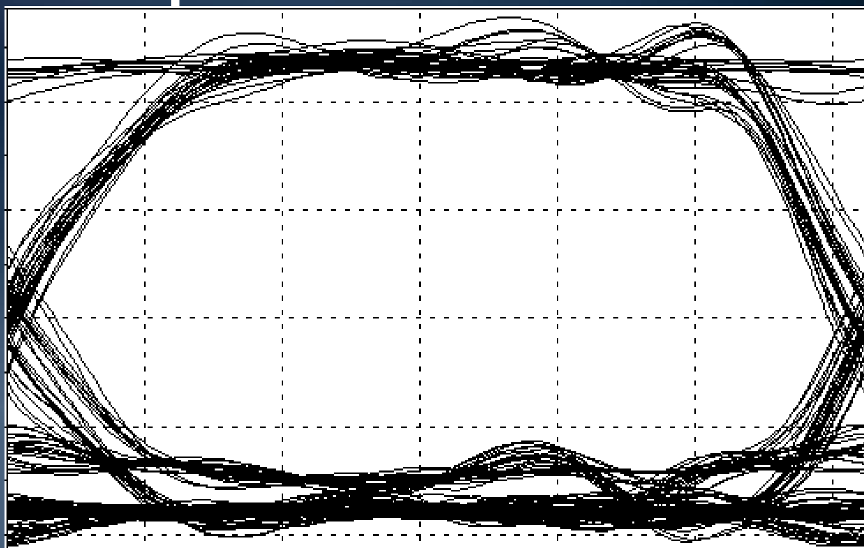


PDA(Peak Distortion Analysis) produce WC eye and WC patterns
Full Time Domain SI-PI simulation might have eyes similar to PDA WC eye but the values are different because of SI-PI impact

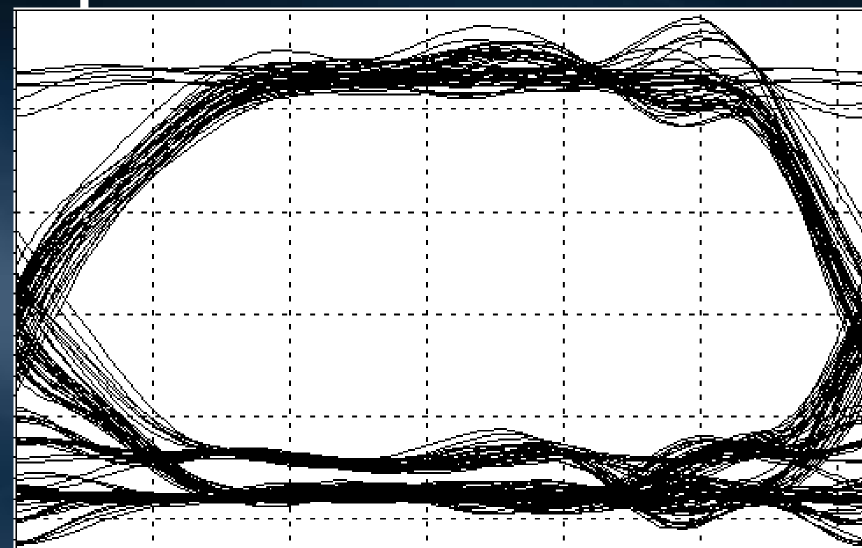
SE WC Results Example

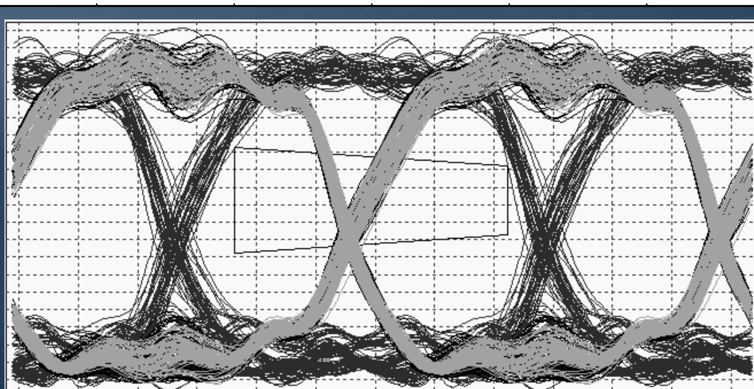
Full Time Domain SI-PI Co-sim Results Ex

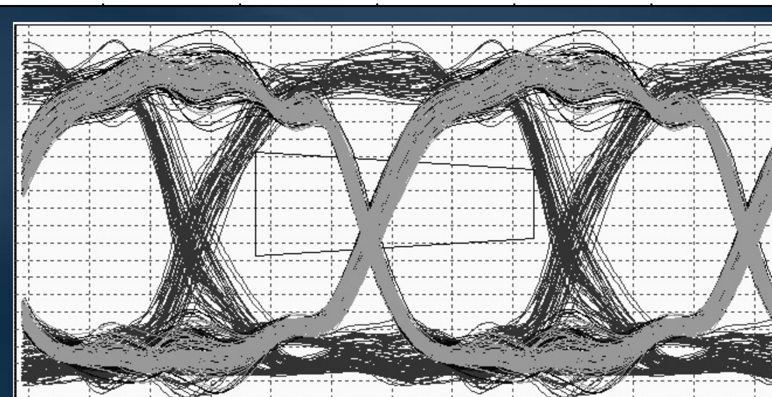
uStrip



Strip

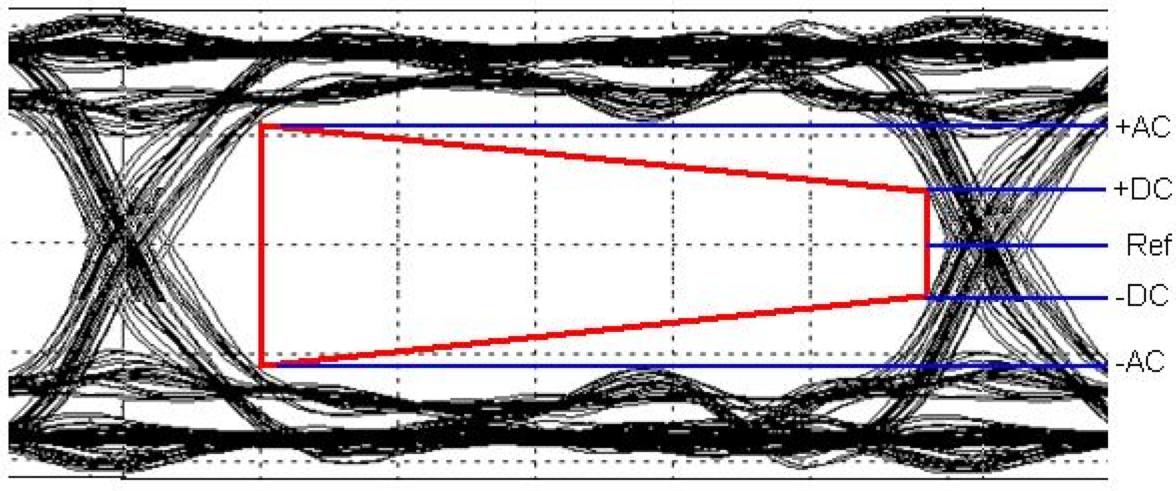




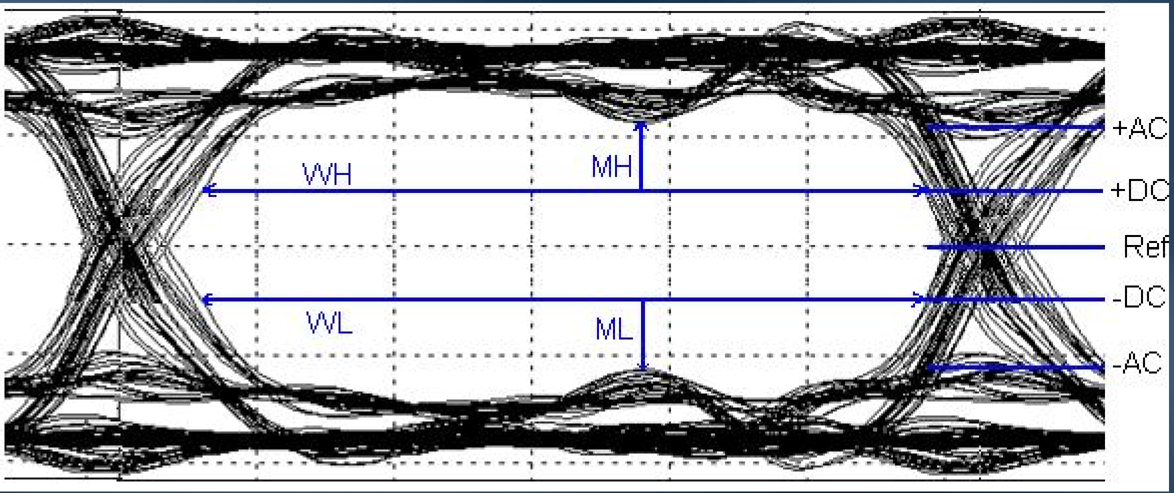


Full Time Domain SI-PI simulation might have eyes similar to PDA WC eye but the values are different because of SI-PI impact

Eye Diagram Measurement

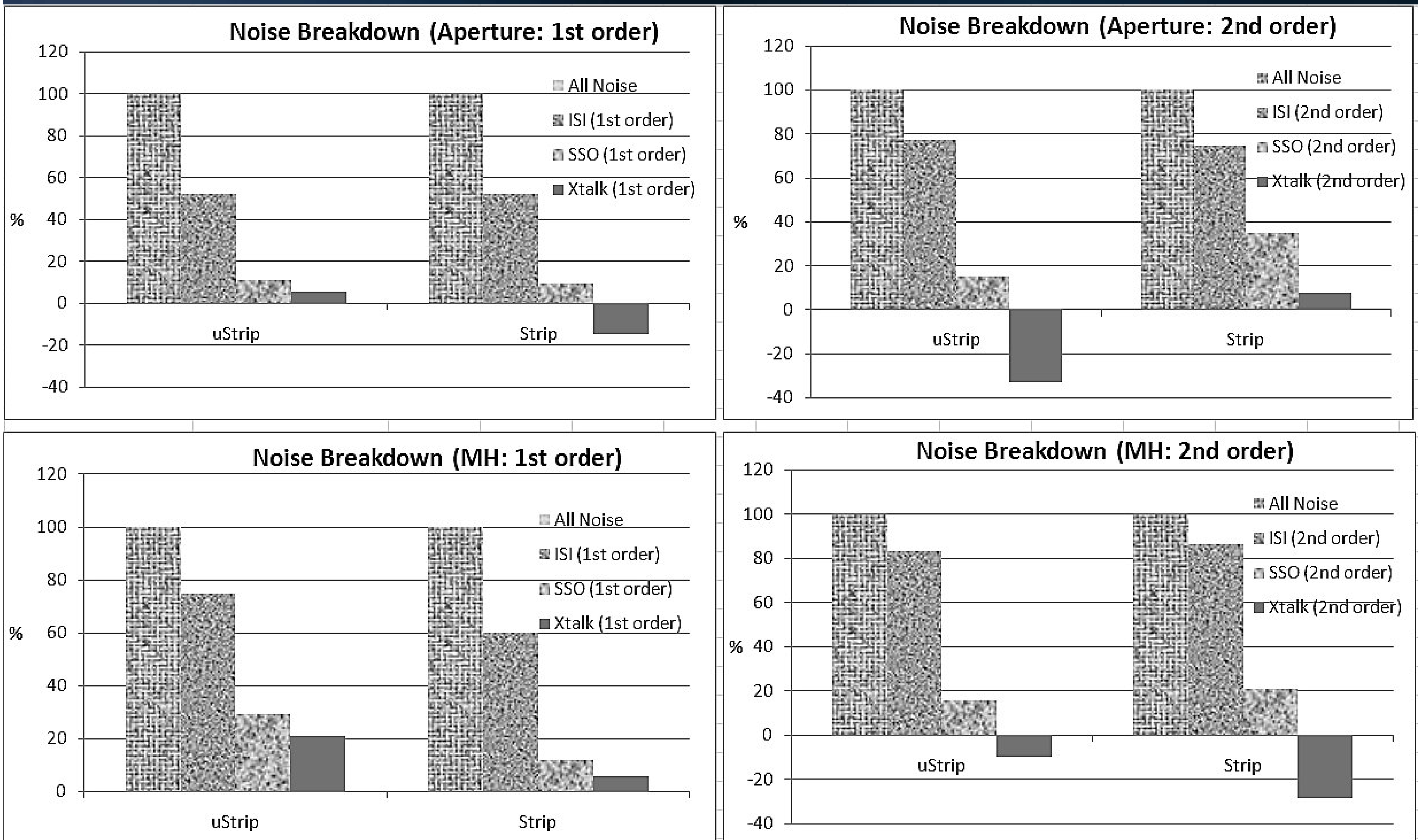


Aperture Measurement using AC/DC spec



Eye Diagram Measurement Scheme

Noise Breakdown Example



Linearity Example: Single Ended

- What is Linearity Indicator (LI)??

$$L.I._{EH}^{1st} = \frac{\Delta EH_{SI}^{1st} + \Delta EH_{SSO}^{1st} + \Delta EH_{Xtalk}^{1st}}{\Delta EH_{All}}$$

$$L.I._{EH}^{2nd} = \frac{\Delta EH_{SI}^{2nd} + \Delta EH_{SSO}^{2nd} + \Delta EH_{Xtalk}^{2nd}}{\Delta EH_{All}}$$

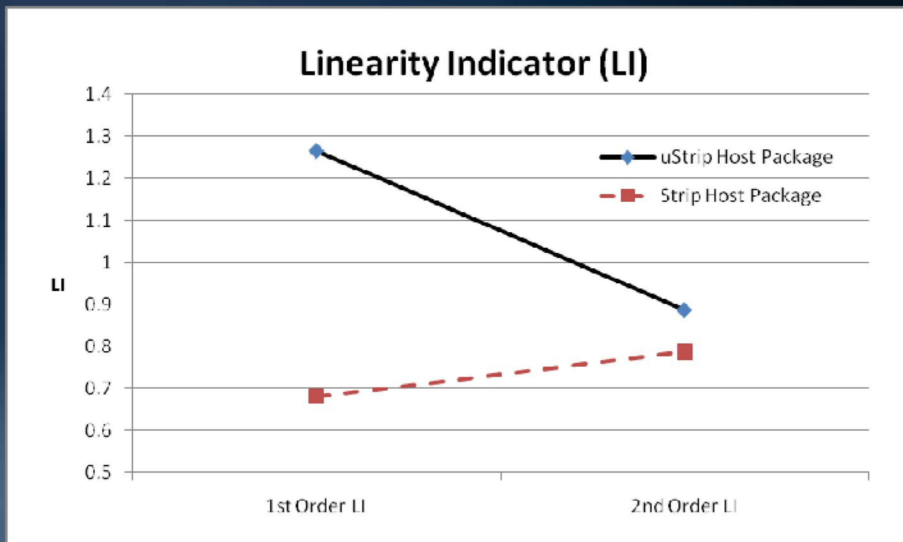
If you are doing SI-only or PI-only Sim/Analysis and
LI>1 : you are overestimating noise
LI<1 : you are underestimating noise

- Ratio of Eye degradation when analysis is done separately to that when it is done combined.
  - 1^{St} order: Only 1 noise generating element
  - 2^{nd} order: 2 noise generating elements

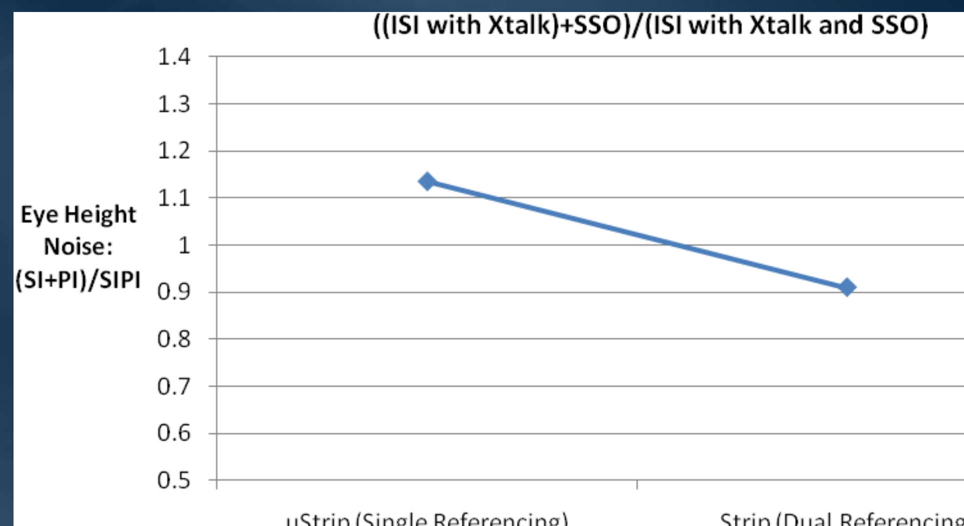
Outlier:
Spec dependent

		Linearity (1st order)	Linearity (2nd order)
uStrip	Aperture Based:	**0.784**	**0.626**
	Mh_based:	**1.266**	**0.887**
Strip	Aperture Based:	**0.891**	**0.978**
	Mh_based:	**0.681**	**0.788**

LI for SE Signaling Example

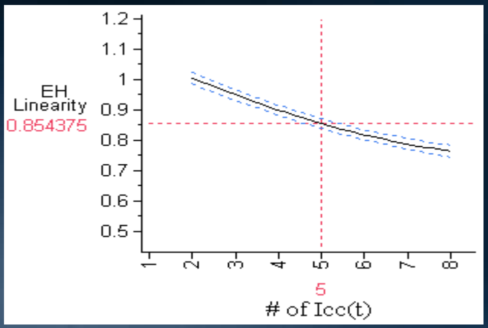


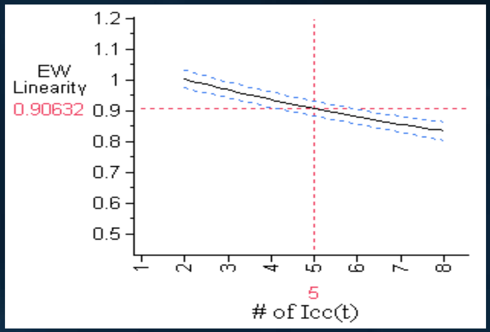
$$\frac{\text{Signal Integrity Noise} + \text{Power Integrity Noise}}{\text{SI-PI Noise}} \approx \frac{(EH_{Case\#1} - EH_{Case\#6}) + (EH_{Case\#1} - EH_{Case\#3})}{(EH_{Case\#1} - EH_{Case\#8})}$$



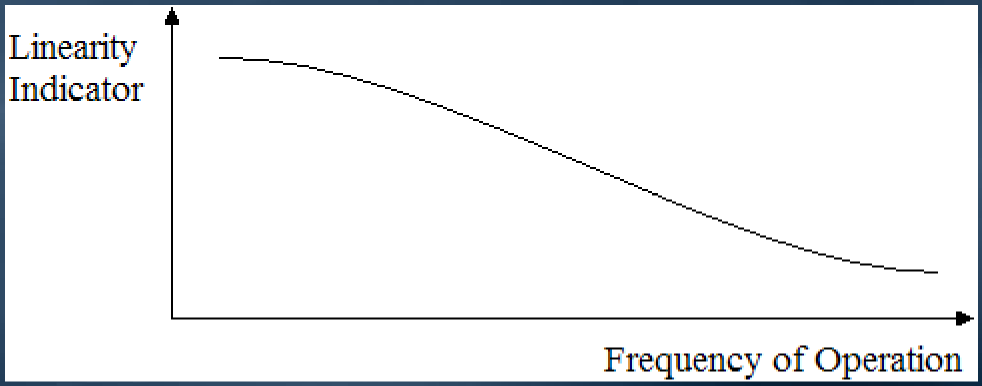
Linearity Examples

- It is system dependent
- Linearity goes down with more no. of SSO bits

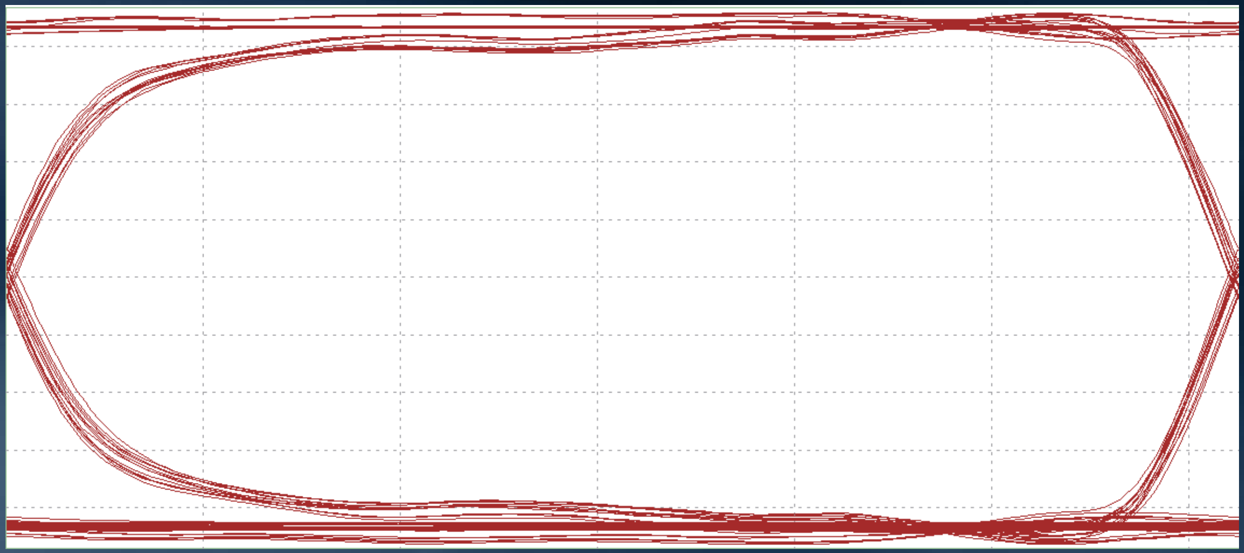




- As the frequency of operation goes up, the linearity suffers. Designer could underestimate noise impact @ higher frequency of operation



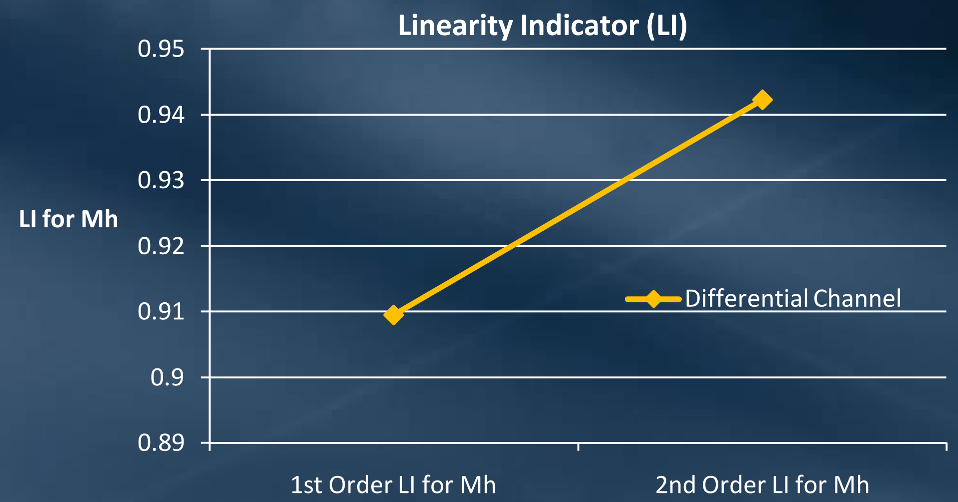
Differential SI-PI Eye Example



- Pseudo-differential buffers driving differential channel
- More linear than Single ended in this example

Diff. Signaling Linearity Example

		Linearity (1st order)	Linearity (2nd order)
Diif. Sig. Ex	Aperture Based:	**0.854**	**0.900**
	Mh_based:	**0.910**	**0.942**



- L.I. for Differential Channel is ~ 0.9 ie. It is close to 1
- It implies that when SI/PI co-simulations are done, the EYE margin reduction is still more, than that compared to if it is done separately. However, the impact is smaller. (compared to single ended)

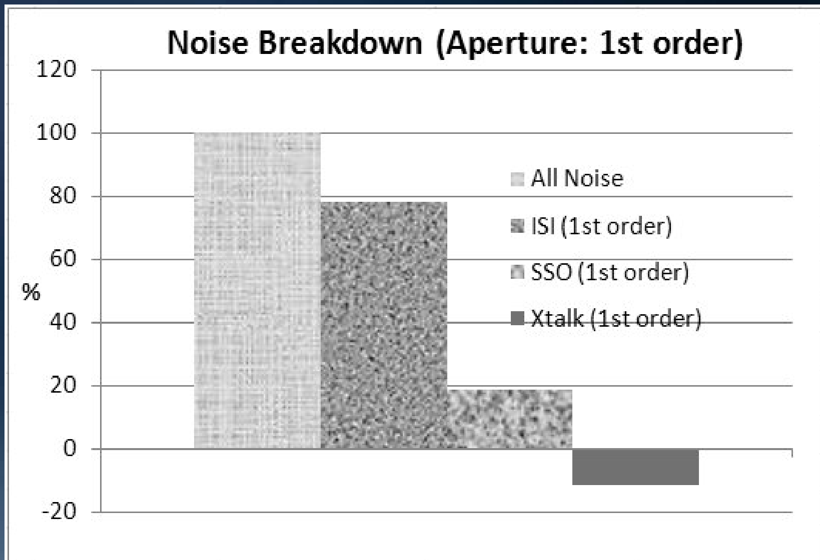
LI for Differential Signaling Example

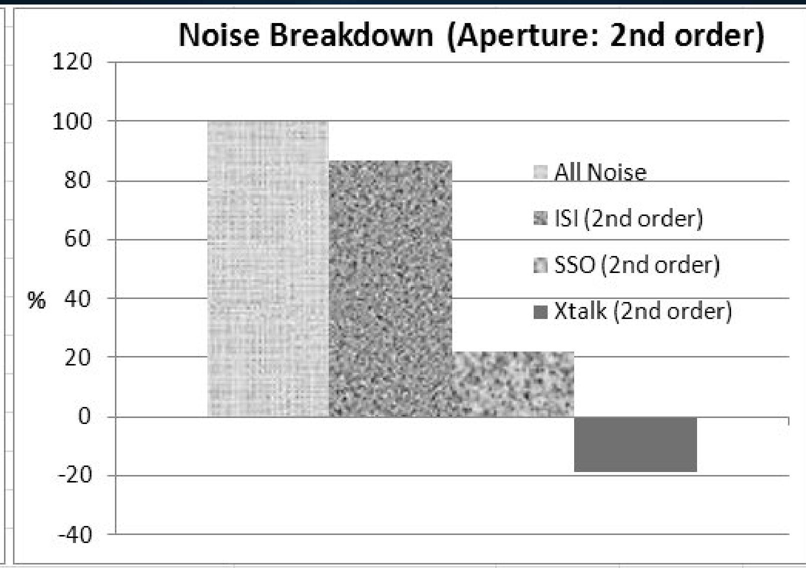
$$\frac{\text{Signal Integrity Noise} + \text{Power Integrity Noise}}{\text{SI-PI Noise}}$$

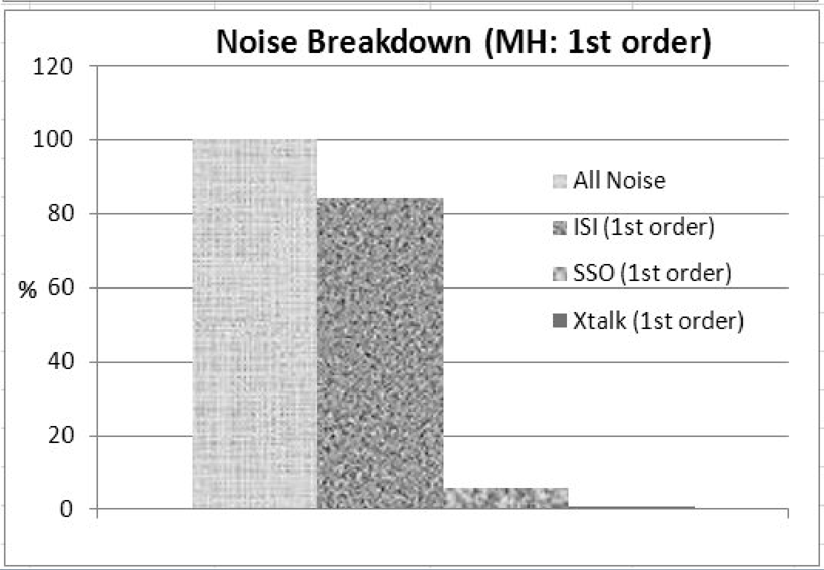
$$\approx \frac{(EH_{Case\#1} - EH_{Case\#6}) + (EH_{Case\#1} - EH_{Case\#3})}{(EH_{Case\#1} - EH_{Case\#8})} = 0.989$$

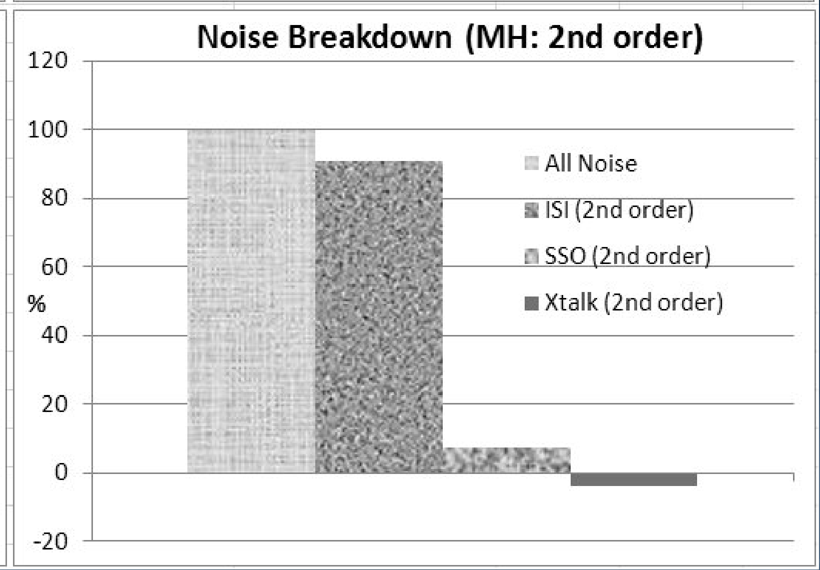
Differential signaling channel has LI close to ~1
Might not need SI-PI

Differential SI-PI Noise Breakdown Example









- Differential channel receiver eye’s 1st order and 2nd order Noise interactions are more linear

IBIS Requirements

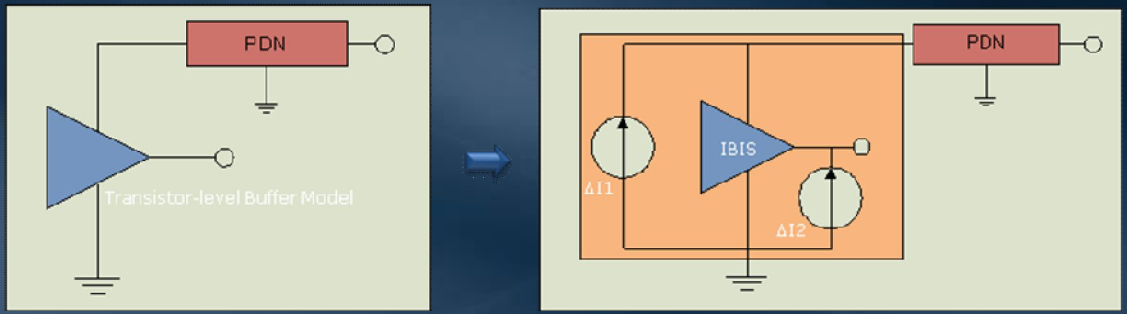
- Accuracy
  - SI
  - PI
    - Icc(t)
  - SI-PI co-simulation
    - Single Ended
    - Differential: Support is critical
- Convenience
  - Automation
- Multiple Domain Power
  - Support is critical

Summary

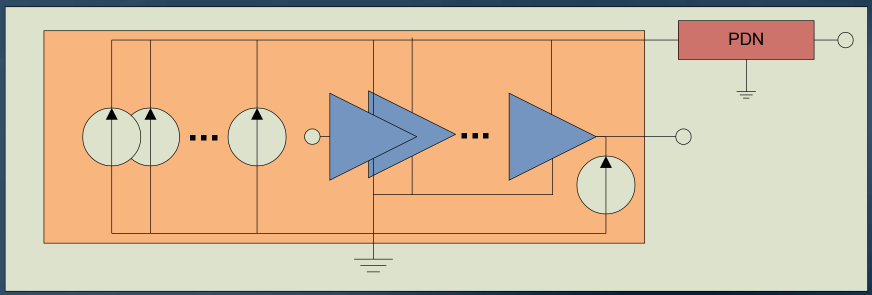
- Running separate SI and PI simulations may underestimate the Eye Degradation
- Full time domain simulations for the system (end to end models required)
- Linearity Indicator
- Single Ended and Differential Systems are evaluated with SI/PI analysis
  - Single Ended Channel L.I.~ 06 to 0.9
  - Differential Channel L.I.~ 0.9
  - For both scenarios, the combined analysis shows more Eye degradations than separate ones. But the effect is more prominent for Single ended channel.

Backup

SI-PI Compatible Behavior Model

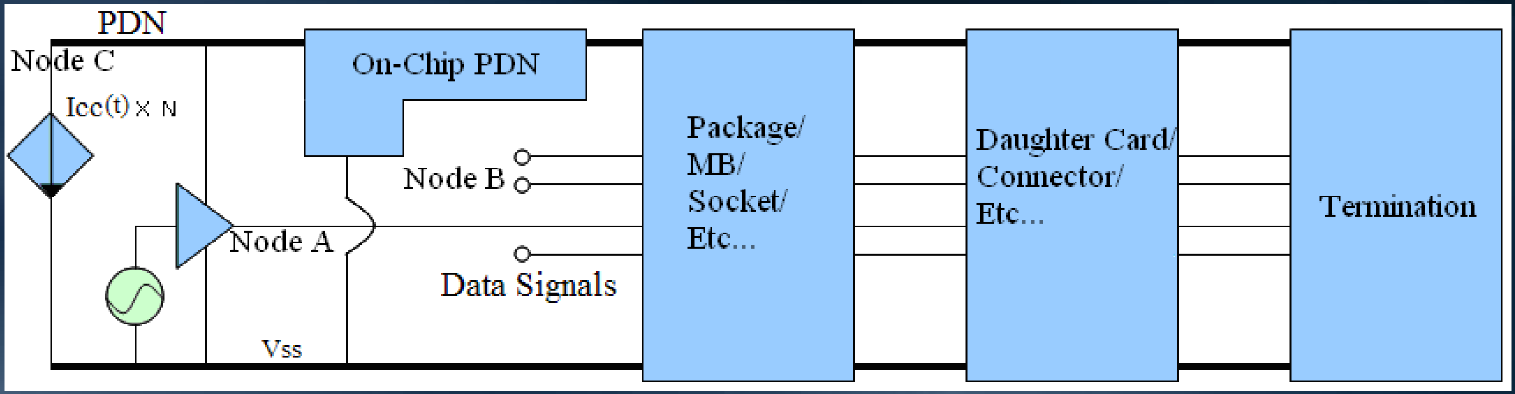


Behavioral model construction for SI-PI co-simulation



SI-PI co-simulation compatible model with variable currents with variable power node voltages

Simulation for ISI, Cross-talk, and SSO Profiling

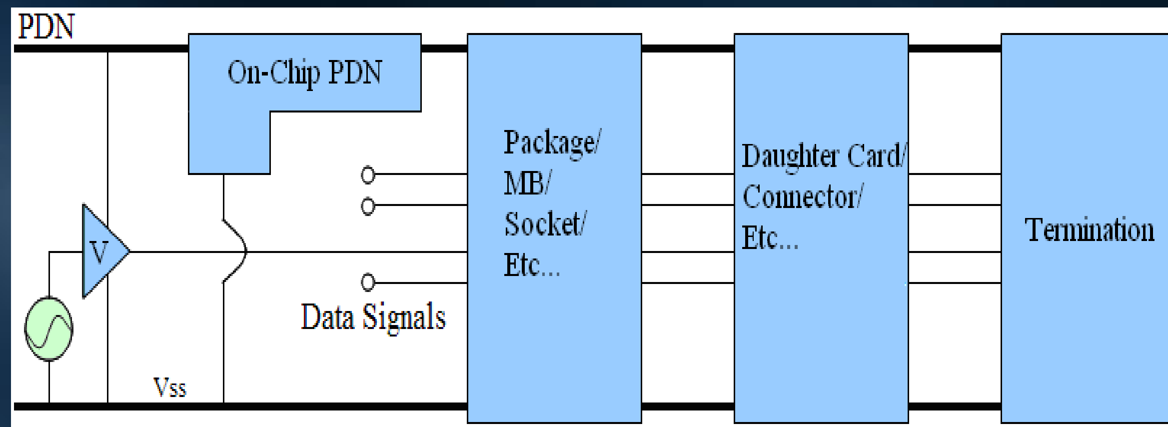


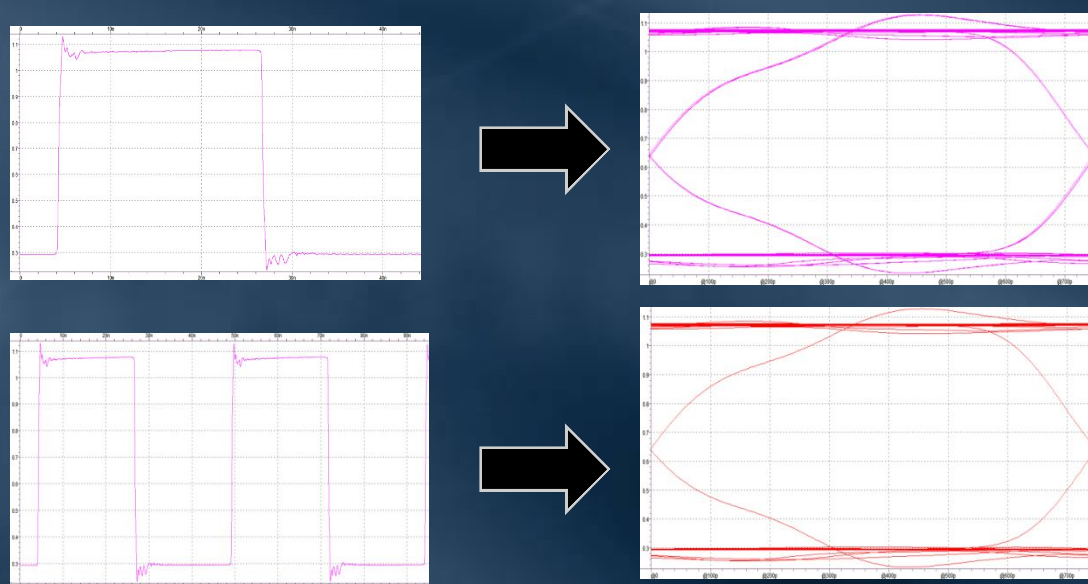
Forced Stimulus Setups for SI-PI Co-simulation

	Case #	ISI	Cross-talk	SSO
ISI	1	Minimal	Minimal	Minimal
	2	Yes	Minimal	Minimal
SSO, ISI	3	Minimal	Minimal	Yes
	4	Yes	Minimal	Yes
Cross-talk, ISI	5	Minimal	Yes	Minimal
	6	Yes	Yes	Minimal
Cross-talk, ISI, SSO	7	Minimal	Yes	Yes
	8	Yes	Yes	Yes

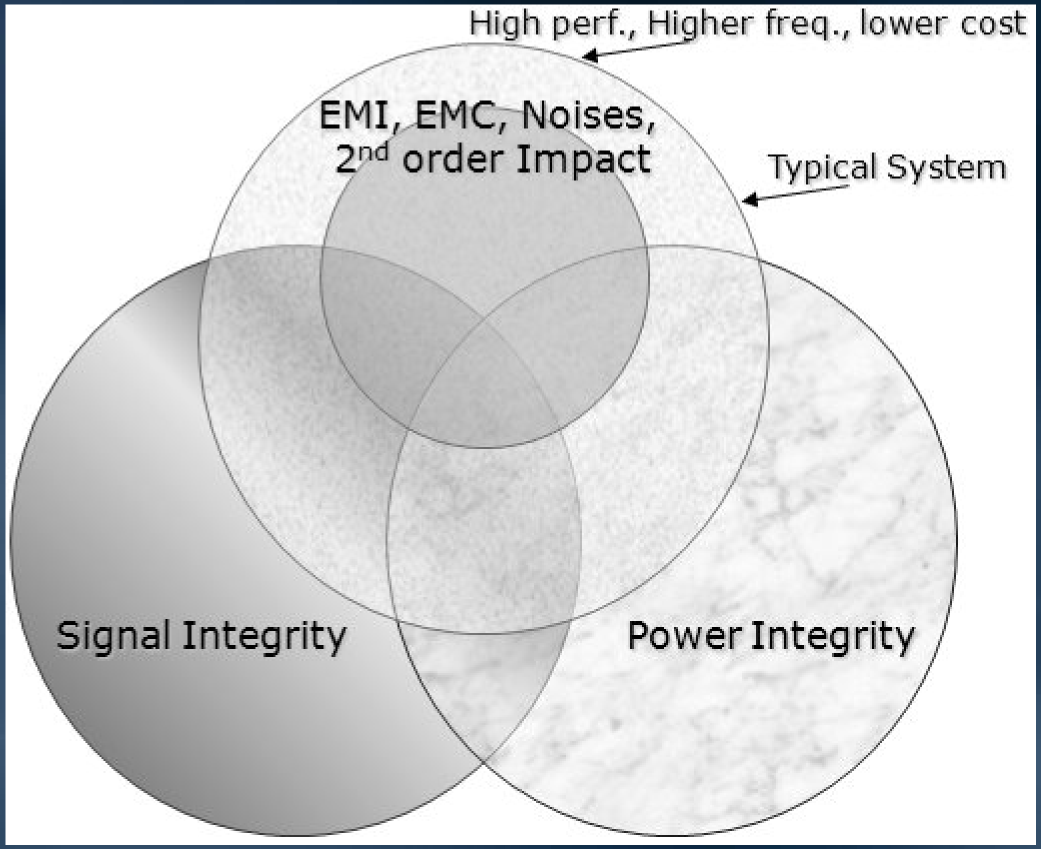
Simulation for ISI & Minimal ISI

- One rising edge & One falling edge





SI-PI Interaction



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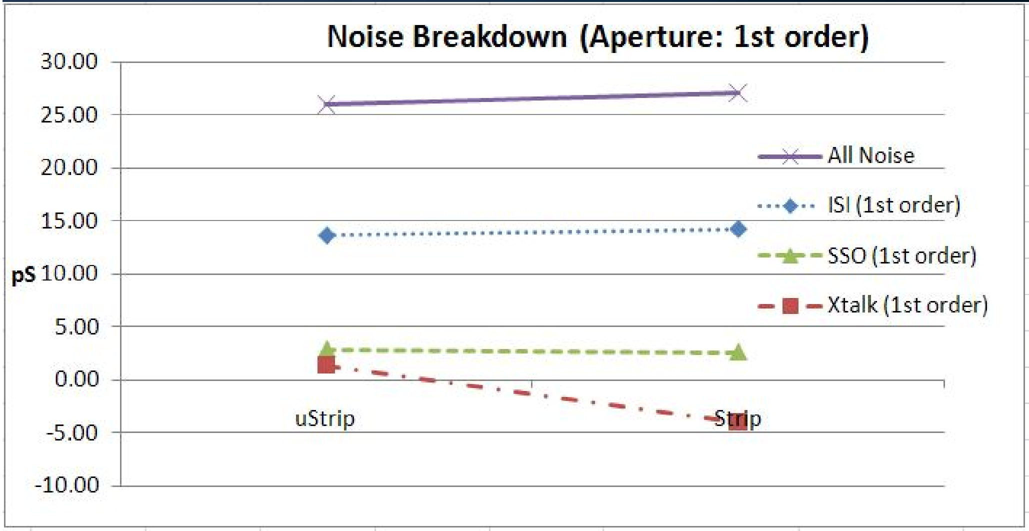
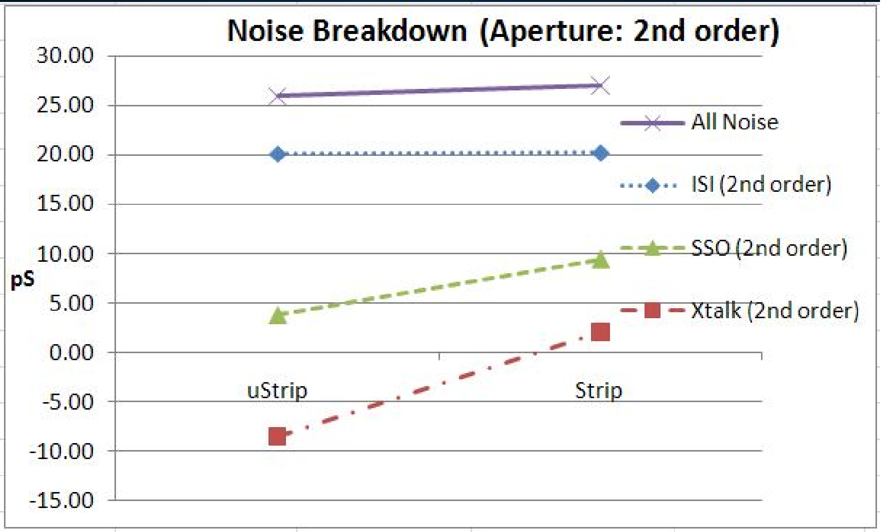
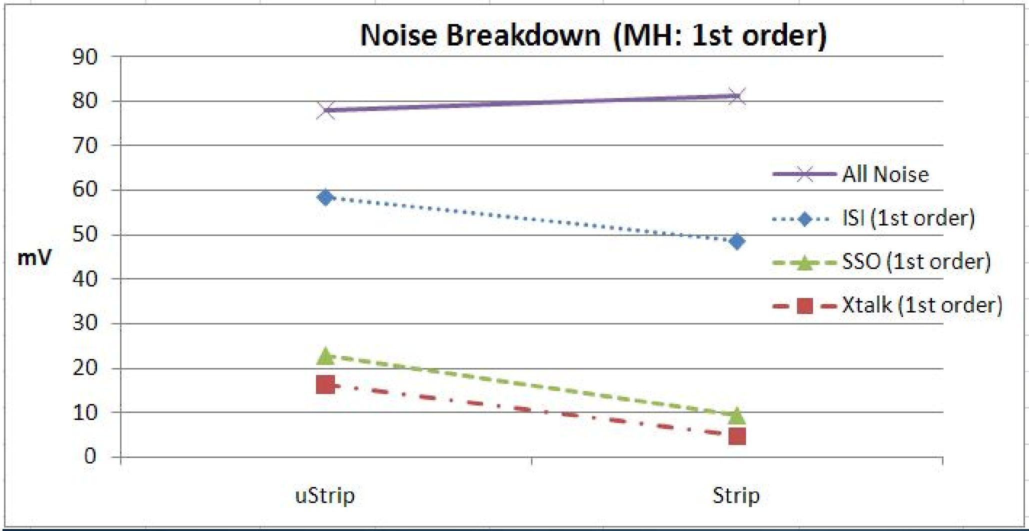
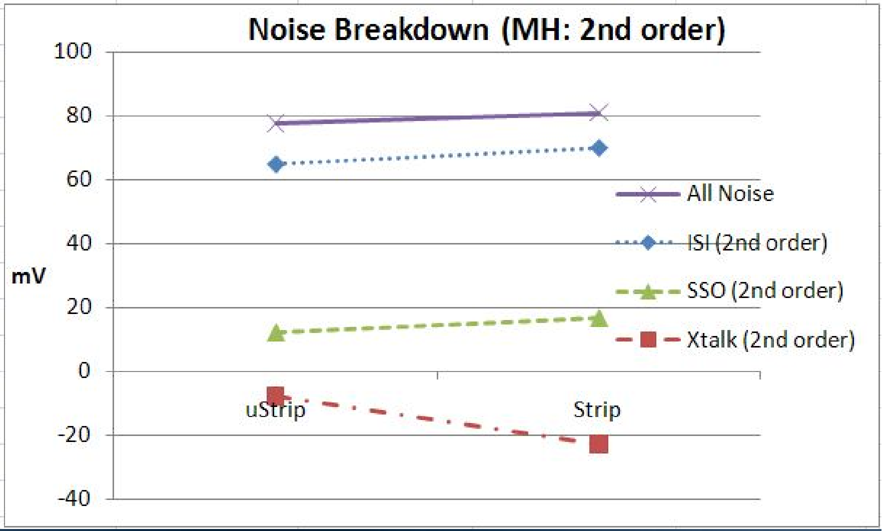
Noise Breakdown Example

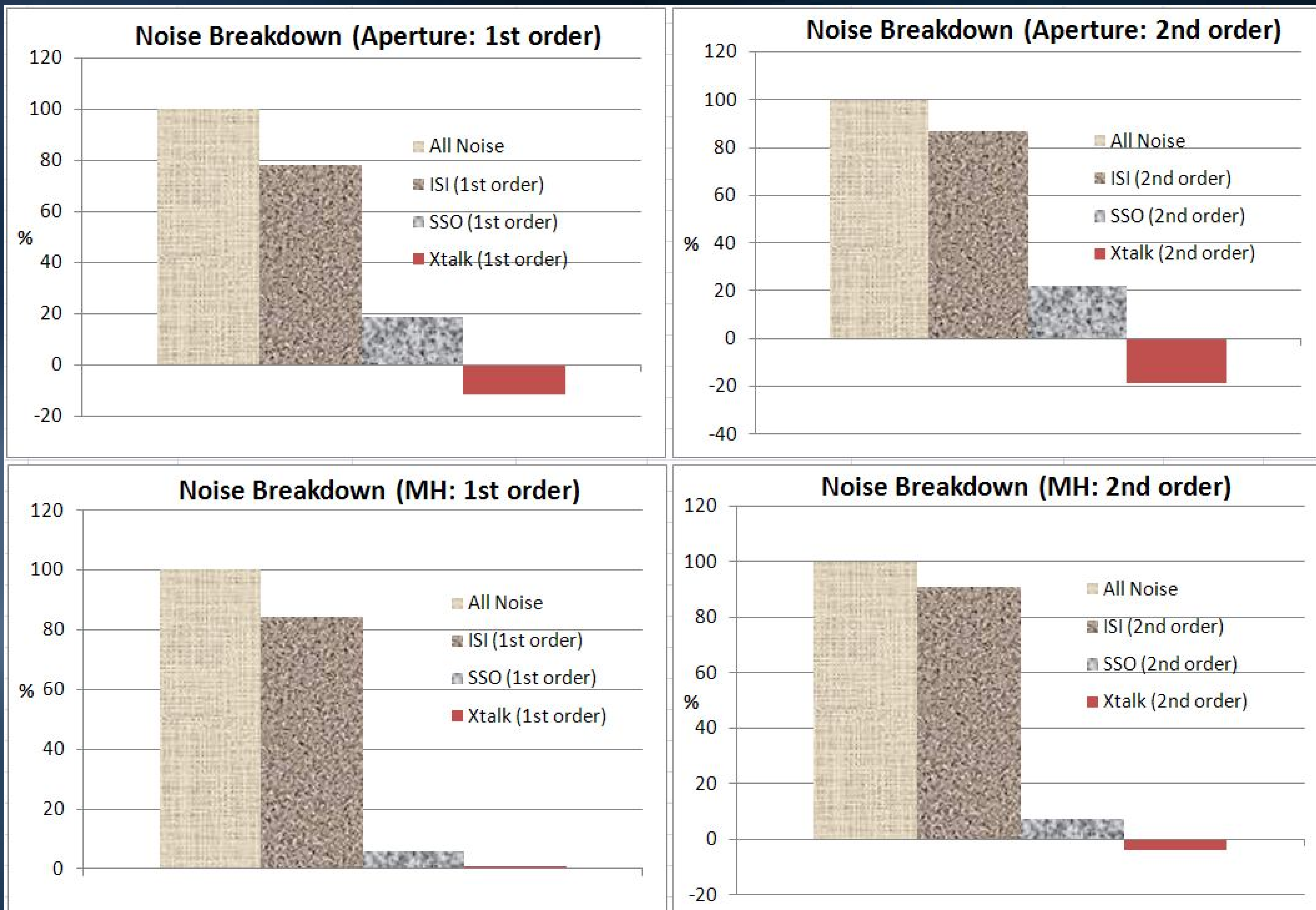






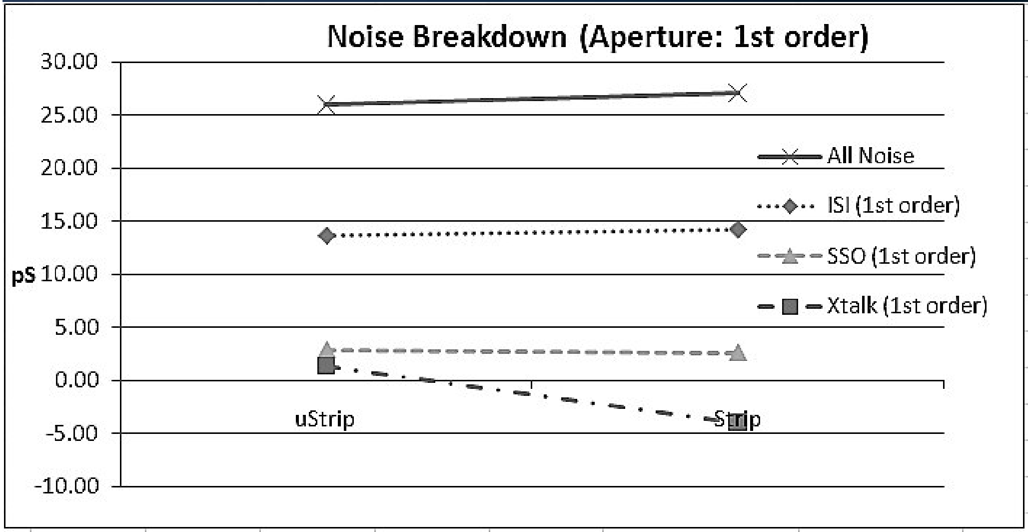


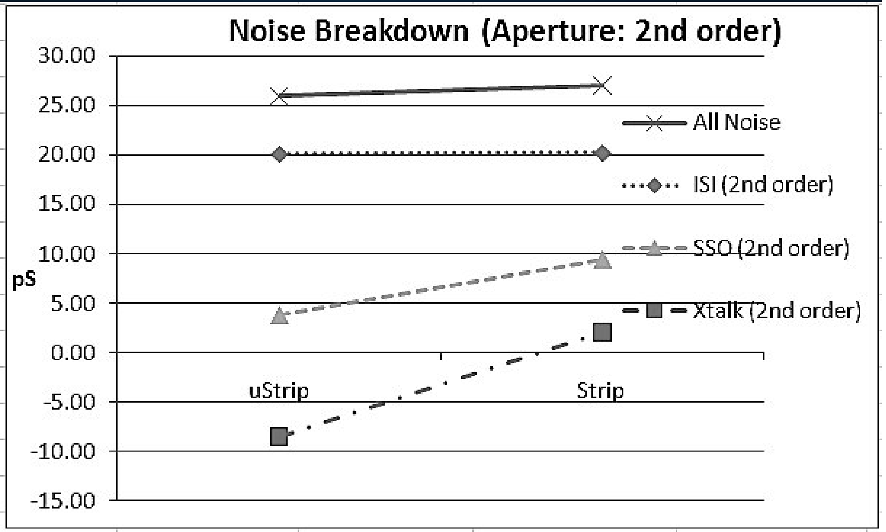
Differential SI-PI Noise Breakdown Example

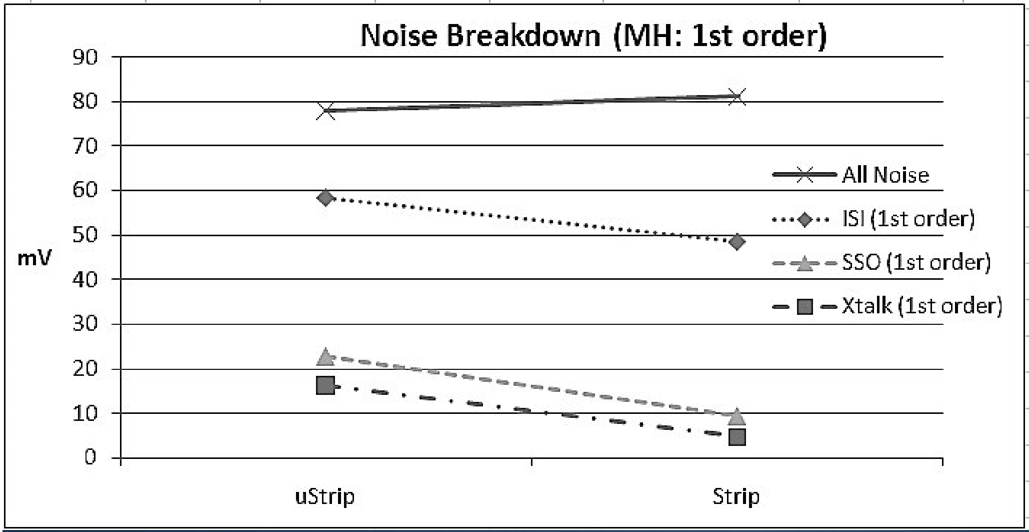


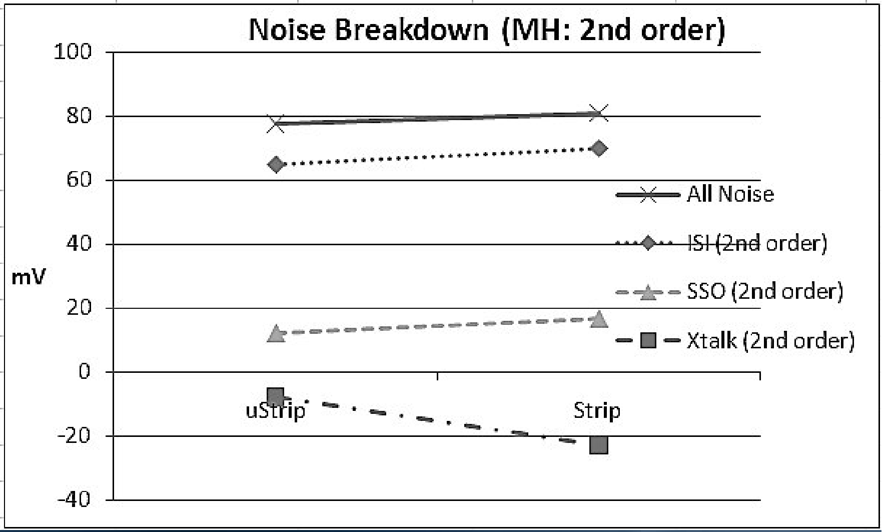
- Differential channel receiver eye's 1st order and 2nd order Noise interactions are more linear

Noise Breakdown Example

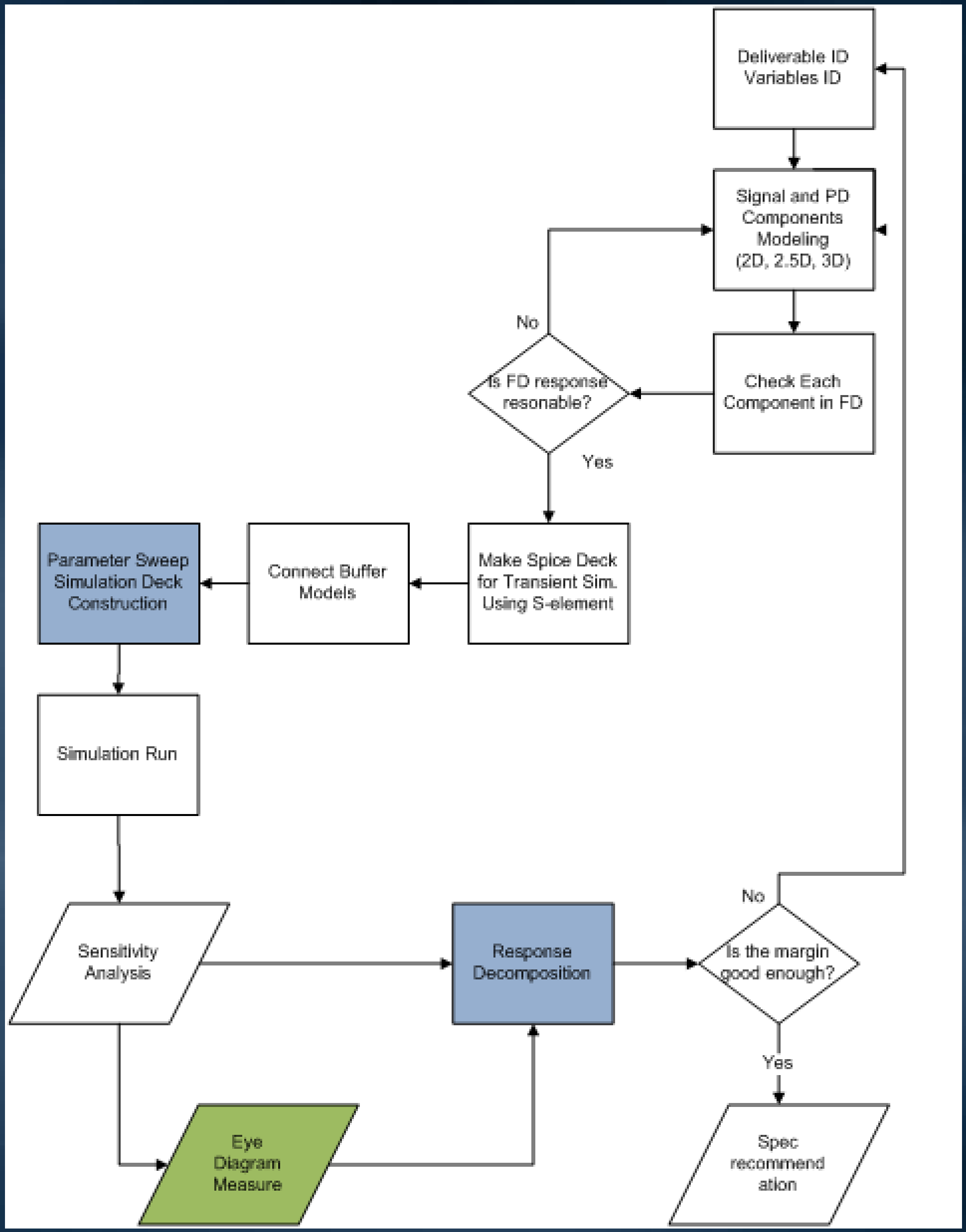








SI-PI General Flow



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LI 1/2

$$\Delta EH_{ISI}^{1st} = EH_{Case\#1} - EH_{Case\#2}$$
$$\Delta EW_{ISI}^{1st} = EW_{Case\#1} - EW_{Case\#2}$$
$$\Delta EH_{SSO}^{1st}$$
$$\Delta EW_{SSO}^{1st}$$
$$\Delta EH_{SSO}^{1st} = EH_{Case\#1} - EH_{Case\#3}$$
$$\Delta EW_{SSO}^{1st} = EW_{Case\#1} - EW_{Case\#3}$$
$$\Delta EH_{Xtalk}^{1st}$$
$$\Delta EW_{Xtalk}^{1st}$$
$$\Delta EH_{Xtalk}^{1st} = EH_{Case\#1} - EH_{Case\#5}$$
$$\Delta EW_{Xtalk}^{1st} = EW_{Case\#1} - EW_{Case\#5}$$
$$\Delta EH_{Xtalk}^{2nd}$$
$$\Delta EW_{Xtalk}^{2nd}$$
$$\Delta EH_{Xtalk}^{2nd} = EH_{Case\#4} - EH_{Case\#8}$$
$$\Delta EW_{Xtalk}^{2nd} = EW_{Case\#4} - EW_{Case\#8}$$

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LI (2/2)

$$\Delta EH^{2nd}_{SSO} = EH_{Case\#6} - EH_{Case\#8}$$

$$\Delta EW^{2nd}_{SSO} = EW_{Case\#6} - EW_{Case\#8}$$

$$\Delta EH^{2nd}_{ISI}$$

$$\Delta EW^{2nd}_{ISI}$$

$$\Delta EH^{2nd}_{ISI} = EH_{Case\#7} - EH_{Case\#8}$$

$$\Delta EW^{2nd}_{ISI} = EW_{Case\#7} - EW_{Case\#8}$$

$$\Delta EH_{All}$$

$$\Delta EW_{All}$$

$$\Delta EH_{All} = EH_{Case\#1} - EH_{Case\#8}$$

$$\Delta EW_{All} = EW_{Case\#1} - EW_{Case\#8}$$

$$L.I.^{1st}_{EH} = \frac{\Delta EH^{1st}_{ISI} + \Delta EH^{1st}_{SSO} + \Delta EH^{1st}_{Xtalk}}{\Delta EH_{All}}$$

$$L.I.^{1st}_{EW} = \frac{\Delta EW^{1st}_{ISI} + \Delta EW^{1st}_{SSO} + \Delta EW^{1st}_{Xtalk}}{\Delta EW_{All}}$$

$$L.I.^{2nd}_{EH} = \frac{\Delta EH^{2nd}_{ISI} + \Delta EH^{2nd}_{SSO} + \Delta EH^{2nd}_{Xtalk}}{\Delta EH_{All}}$$

$$L.I.^{2nd}_{EW} = \frac{\Delta EW^{2nd}_{ISI} + \Delta EW^{2nd}_{SSO} + \Delta EW^{2nd}_{Xtalk}}{\Delta EW_{All}}$$