

Top 10 Issues As Seen During IBIS Model Reviews

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The IBIS Model Review Committee

- Chair receives IBIS files
 - Table-based models
 - VHDL-AMS / Verilog-AMS
 - Touchstone
- Files are parsed
- Graphical checks are performed
- Files are distributed to reviewers
- Issues communicated to originator

Current Reviewers

Green Streak Programs (chair)

Cadence Design Systems

IO Methodology

Mentor Graphics

Signal Integrity Software

Sigrity

Zuken

The Good News

- Migration from s2ibis2 to s2ibis3
- More files passing ibischk5

The Bad News

- Everyone still has a “little list”
- Some old (well-known?) issues
- Some new ones

The “Top 10”: Headers & Setup

1. Characters other than [A-Z a-z 0-9 ,_-.] within IBIS files

Especially parentheses

Mainly in [Notes] and [Copyright], !comments

These might break EDA tools

2. No [Notes] or [Source]

Other than legal disclaimer

3. TYP [Temperature] near room temperature

4. Rref above 200 Ohms

The “Top 10”: Data

- 5. Non-monotonicity in total current
- 6. I-V tables not passing through 0A at 0V

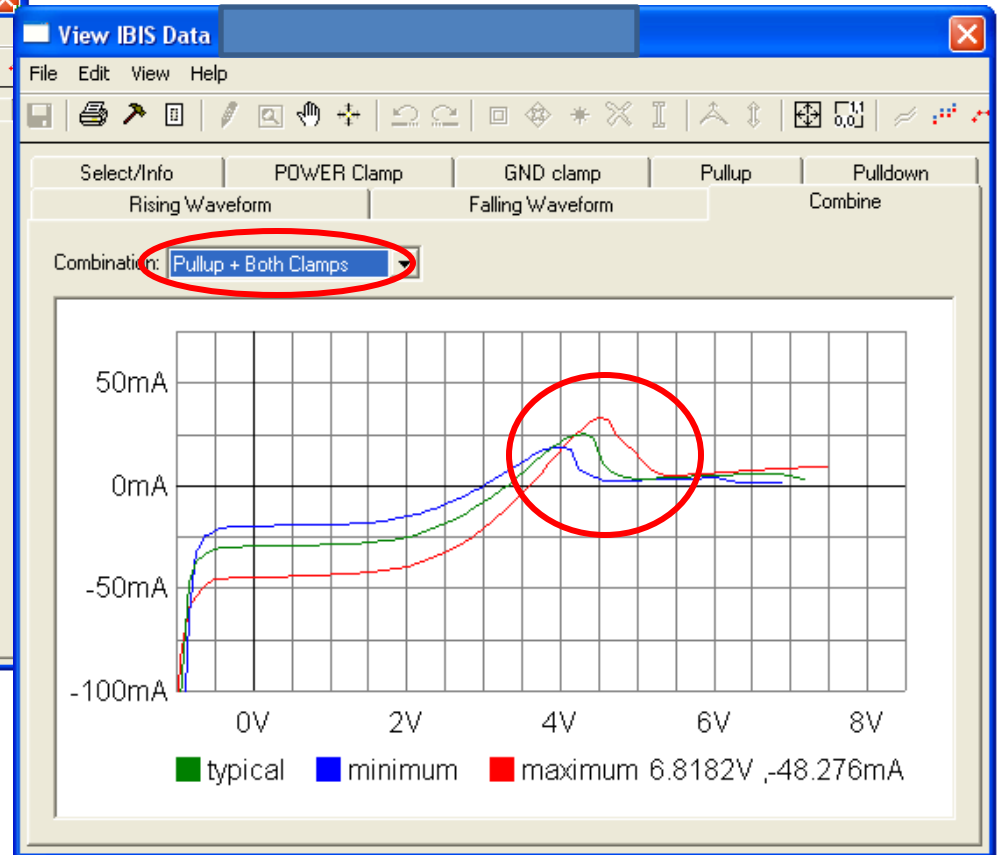
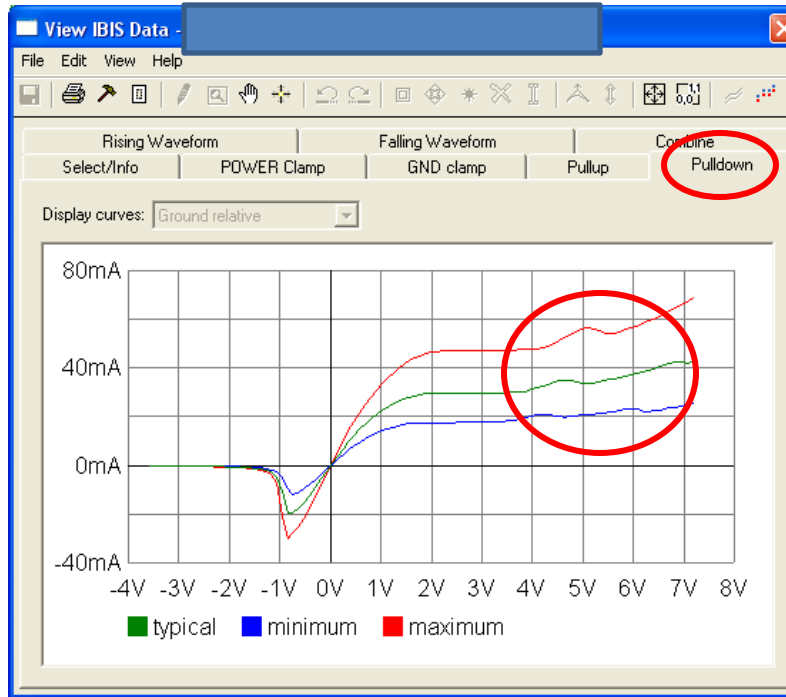
Data extraction or reference voltage?

More common in differential I/O

Exposure to tool extrapolation / interpolation

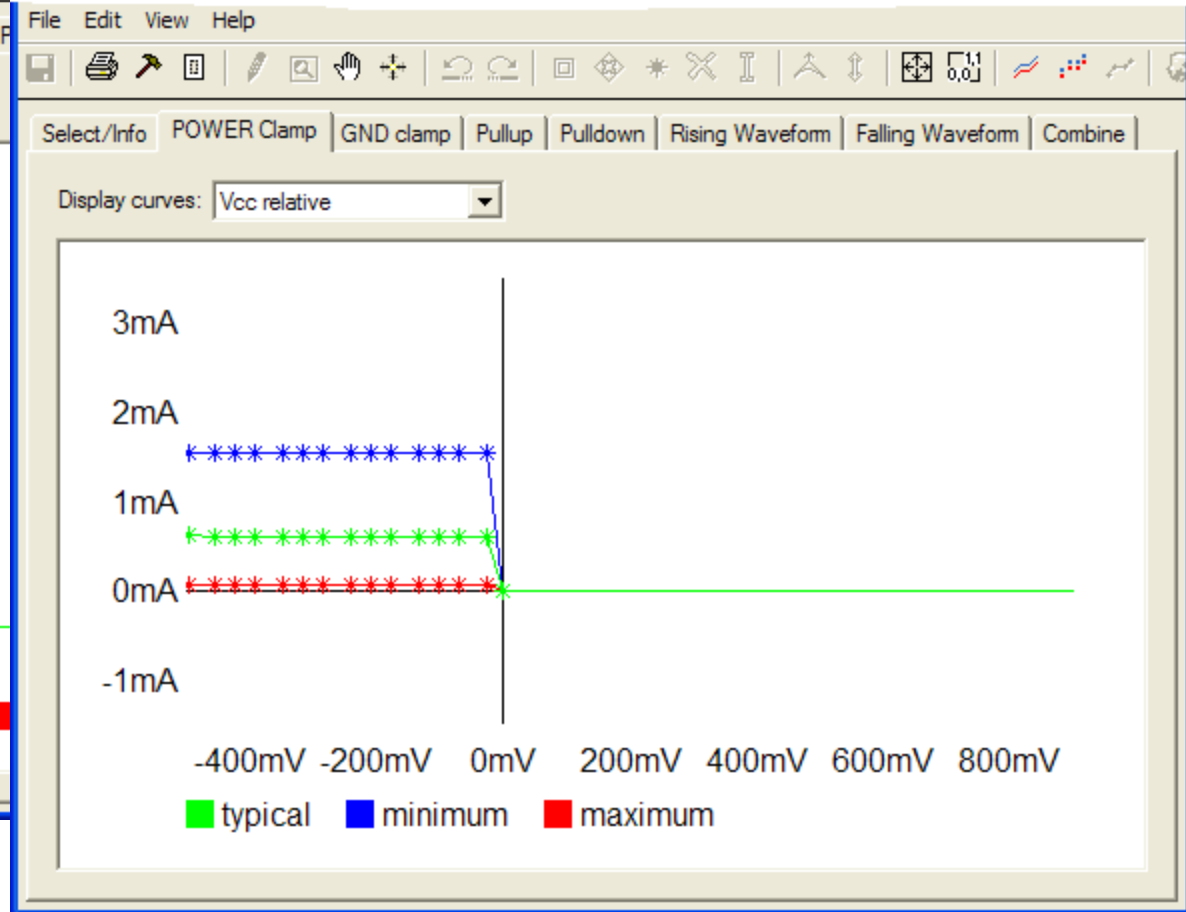
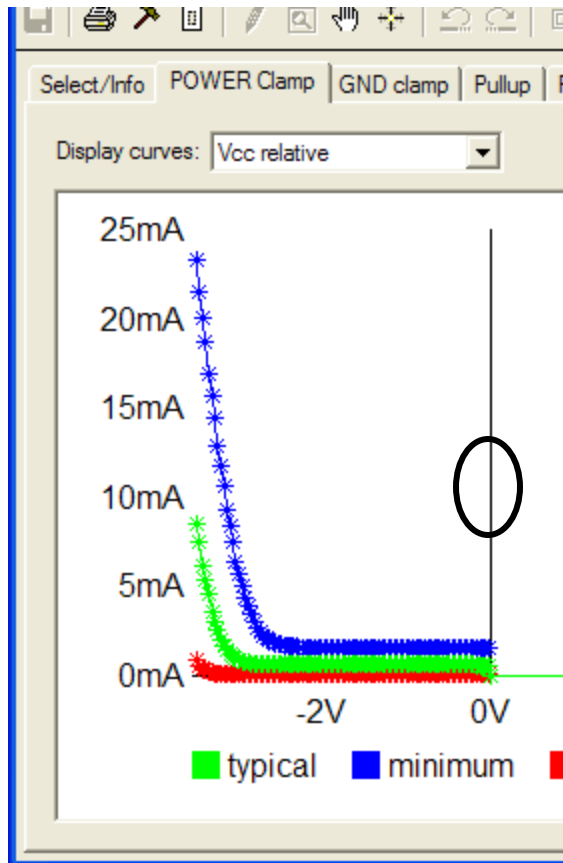
- 6. Clamp tables not covering $-V_{cc}$ to $+2V_{cc}$
- 7. Clamp tables with no points between 0V and $2V_{cc}$
- 9. Waveform tables ending too soon or too late
- 10. Other unexpected data table characteristics

Example of non-monotonicity in TOTAL current



Forcing a table to have 0A at 0V

Derivatives not continuous



The Facts of Life (or at least IBIS)

- More people are using the IBIS Cookbook
- More people are running ibischk5
- Model makers AND their managers need training
- Differential models need more care
- Things are getting noticeably better
- The model review committee is still needed