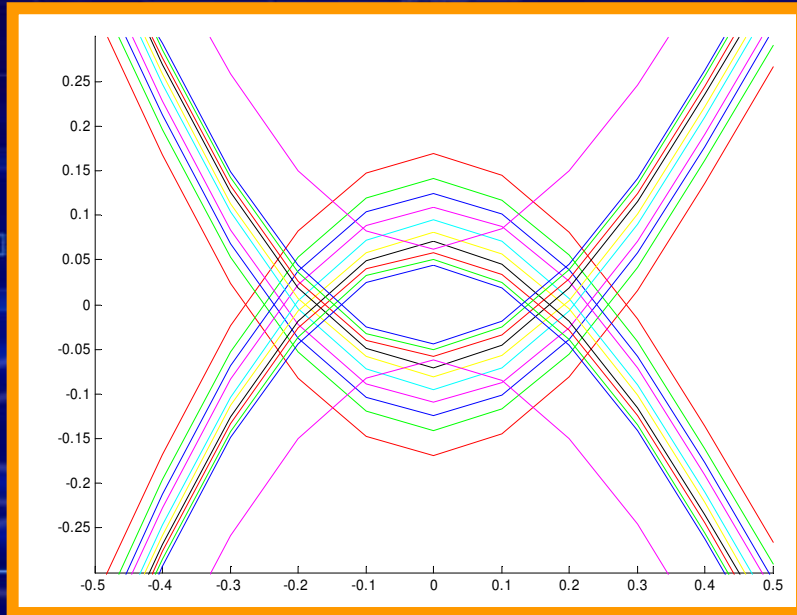


Growing Pains with IBIS-AMI modeling

***IBIS Summit, DesignCon,
February 4, 2010
Santa Clara, CA***



Arpad Muranyi

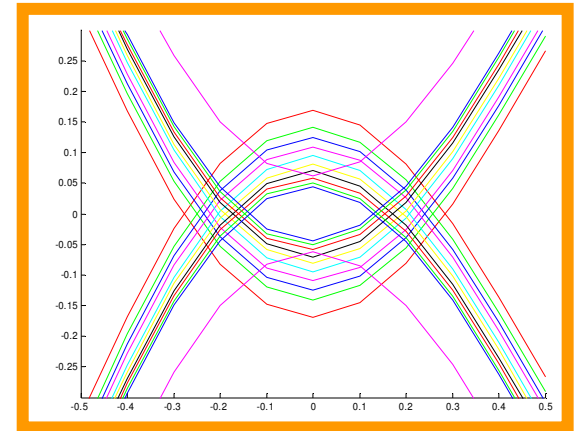


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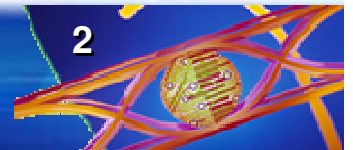
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1. Historical IBIS-AMI overview
2. The condition of the IBIS-AMI specification
3. The condition of the IBIS-AMI parser
4. IBIS-AMI awareness
5. A few words on AMI models
6. The analog IBIS model and AMI
7. Work in progress and not in progress
8. Plea

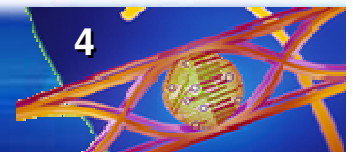


Historical IBIS-AMI overview

- The IBIS v5.0 specification containing the Algorithmic Modeling Interface (AMI) has been ratified on August 29, 2008
- ibischk5 has been released on December 18, 2009
- Several EDA tool vendors have announced support for IBIS-AMI recently
- IC vendors are starting to release IBIS-AMI models for their SERDES products or express interest in making models for upcoming products

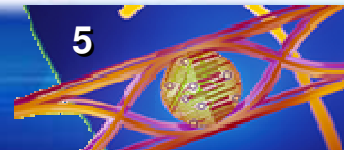
The condition of the IBIS-AMI specification

- A few problems have been discovered with the AMI specification during the development of ibischk5 and during normal, everyday work with it
 - the parser developer reported inconsistencies and ambiguities in the specification
 - fortunately we were able to answer his questions and the parser development was completed
 - EDA tool developers and model makers can't find answers to some questions by reading the specification
 - email discussions helped in finding answers, but the specification must be improved
 - a flaw in the AMI flow was discovered that unintentionally prevented the use of non-LTI algorithmic models
 - the specification must be corrected
- A major revision of the AMI portion of the IBIS specification will address all of these issues, planned for IBIS v5.1
 - the IBIS ATM group is currently working on a BIRD to address these issues



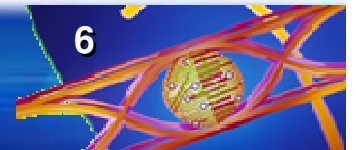
The condition of the AMI parser

- A few problems have been discovered with the AMI parser after its release
 - none of them seemed to be major issues, but they were serious enough to make the parser unusable
 - most (or all?) of these problems have been fixed and new “dot releases” have been issued



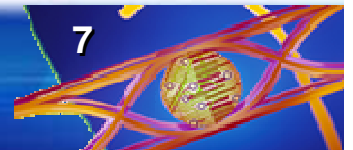
IBIS-AMI awareness

- **AMI is relatively new and lot of education is needed**
 - most “would be model makers” know that IBIS-AMI is useful (and necessary) for GHz SERDES design,
 - but are not familiar with the basic concepts
 - the dividing line between analog “IBIS” models and the “AMI” is blurry
 - the dependence between the above two is not clear
 - the difference between an AMI .dll and an AMI .ami file is not always clear
 - the difference between a time domain channel characterization simulation and the (time domain) signal processing in the algorithmic model (AMI .dll) is not always understood
- **An IBIS-AMI cookbook would probably help a great deal**



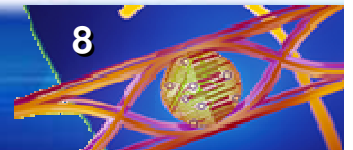
A few words on AMI models

- **A complete AMI modeling solution consists of a minimum of three items:**
 1. **a “conventional” analog IBIS model (using the [Model] keyword) and pointing to an AMI model**
 - including buffer and package models
 - these are needed to generate an impulse response from the channel, which is a fundamental and required input to the AMI models
 2. **one or more AMI .dll executables**
 - this is what most everyone focuses on
 3. **an .ami (parameter) file for each AMI .dll executable**
 - some vendors deliver AMI models without an .ami file, or with a non-compliant .ami file that would fail the IBIS parser
- **Unfortunately not all AMI models are delivered with all of the necessary ingredients**



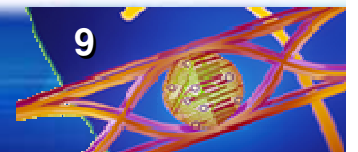
The analog IBIS model and AMI

- The limitations in the “traditional” (analog) IBIS specification makes it hard if not impossible to write an analog IBIS model for GHz buffers associated with AMI modeling
 - C_comp topologies tend to become more complicated
 - differential Cdiff, Rdiff are not available in IBIS
 - current IBIS package model is useless for GHz purposes
- These problems motivate vendors to write IBIS-AMI models that are non IBIS specification compliant
 - we are aware of several such non-compliant IBIS-AMI models
 - these models are non-portable, non-interoperable, and defeat the purpose of the IBIS-AMI specification
- The IBIS Open Forum must put a high priority to solve these issues so that there would be no reason or excuse for distributing proprietary modeling solutions



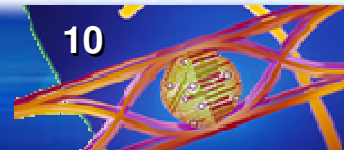
Work in progress

- **A new interconnect specification is almost finished**
 - the IBIS-ATM group prepared a draft for the IBIS Interconnect SPICE Subcircuit (IBIS-ISS) specification
 - this addresses the package and board modeling needs with a standardized SPICE language
 - needs a few finishing touches and approval
- **An Electrical Model Connectivity specification is in the works**
 - this specification would standardize how the various devices (chip, package, connector, etc...) are instantiated and connected in a design project
 - this may supersede the existing EBD specification and the proposed EMD ideas



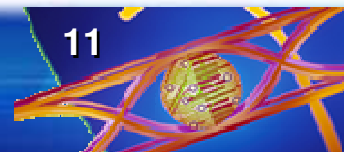
Work not in progress

- **Some (differential) buffer modeling issues are still not addressed**
 - at GHz speeds we need much more than C_comp to the rails
 - pin-to-pin (differential) capacitance and resistance (termination)
 - on die termination (ODT) to a specific voltage (Vtt) source with non-ideal voltage source characteristics
 - I-V curves which are affected by the voltage on the other pin
- **Most (or all) of these could be done with [External ...], but those keywords are not implemented in most EDA tools**
- **IBIS-ISS could theoretically address some of these needs, but currently that specification is not intended to be used for on-die circuit description**
 - [External Circuit] could be used potentially to call IBIS-ISS models but there may be other complications involving [External Circuit] when used for buffer modeling



Plea

- AMI gave new life to IBIS, but we still need to address some serious shortcomings in the “legacy” portions of the IBIS specification to make AMI work without any EDA tool dependent, proprietary modeling solutions
- This situation needs immediate attention, and urgent solutions
- Let's address these problems in a timely manner and provide a complete IBIS-AMI modeling solution in IBIS v5.2



The background is a vibrant blue with a complex pattern of white and light blue lines. These lines form a network of interconnected nodes and paths, reminiscent of a circuit board or a data network. There are also some faint, stylized 3D wireframe shapes scattered throughout, adding a sense of depth and technology.

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