Predicting BER with IBIS-AMI: experiences correlating SerDes simulations and measurement

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IBIS Summit @ DesignCon 2010
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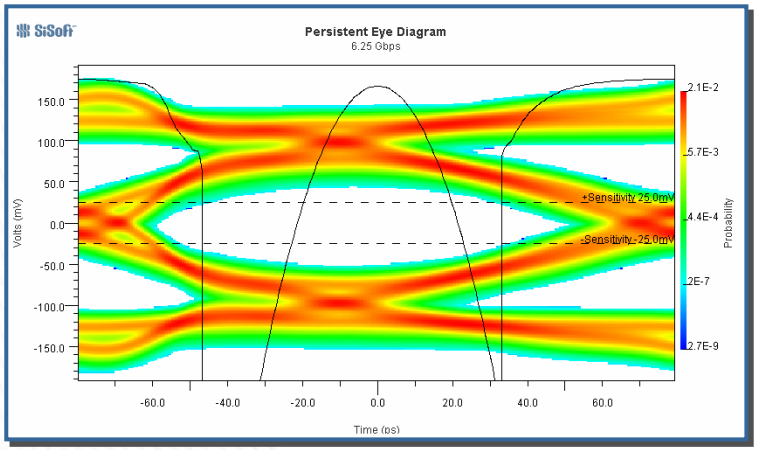
Agenda

- IBIS-AMI Overview
- IBM's IBIS-AMI Models
- Correlation Methodology
- Correlation Results w/o Jitter/Noise
- Jitter / Noise Modeling & Extrapolation
- IBIS-AMI Performance

The SerDes Simulation Problem



- ✓ Model SerDes EQ & CDR
- ✓ Simulate >10M bits
- ✓ Predict BER
- ✓ Models run in multiple tools

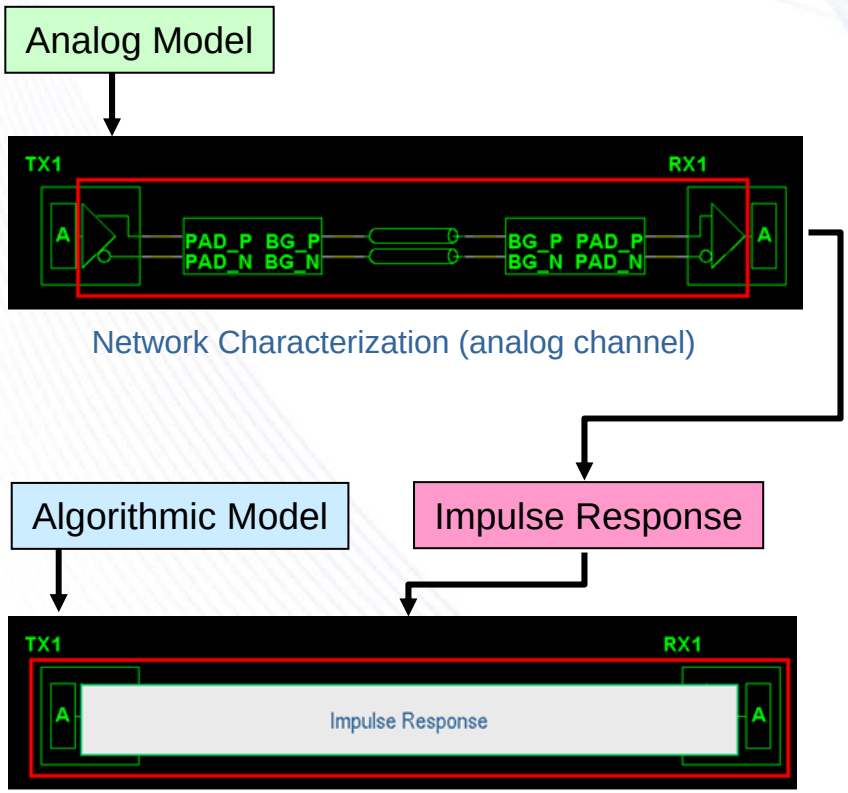
- SPICE
  - Low simulation throughput
- Open-source tools
  - No vendor models
- Vendor tools
  - Limited interoperability
- EDA Tools
  - Proprietary models (Before IBIS-AMI)

Standardizing SerDes Modeling

Goal: create a open modeling standard SerDes for SerDes PHYs that provides:

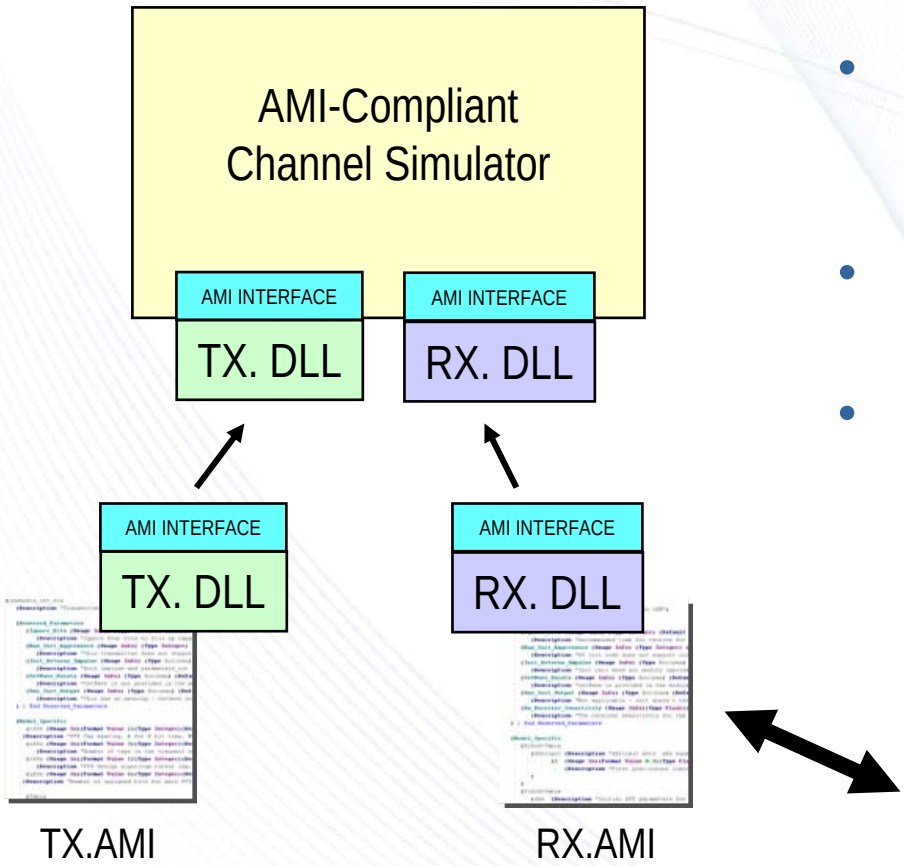
- **Interoperability:** different vendor models work together
- **Transportability:** one model runs in multiple simulators
- **Performance:** comparable to vendor simulators
- **Accuracy:** comparable to vendor simulators
- **IP Protection:** accurate models without divulging internal architectural details

IBIS Algorithmic Modeling Interface (IBIS-AMI)



- Part of IBIS 5.0 specification
- Divides serial link analysis into two steps
  - Network characterization
    - Derives impulse response for unequalized analog network
  - Channel simulation
    - Analyses end-end link
- IBIS-AMI models have two parts
  - Analog model
  - Algorithmic model

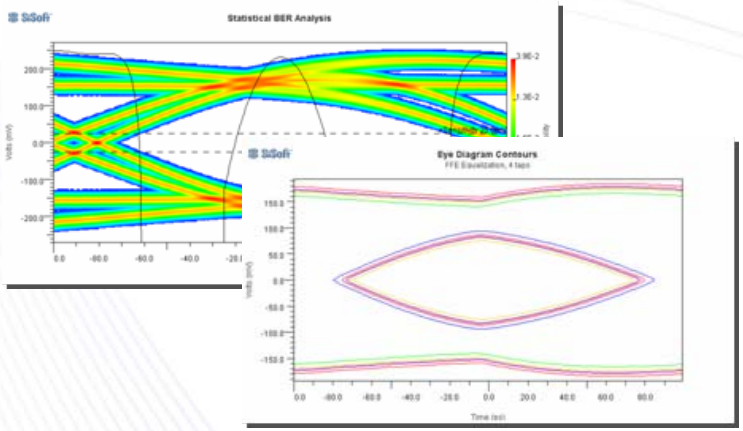
IBIS-AMI Algorithmic Models

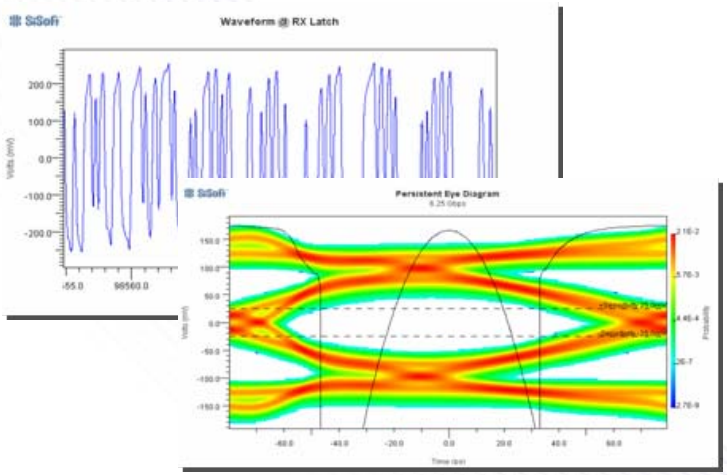


- Supplied as binary code (.DLL) that gets linked into the Channel Simulator at runtime
- Standardized entry points and data passed to/from the model
- Control (.AMI) file lists what features the model supports & what controls the user can set

Variable:	Type:	Value 1:
RX1:Table.dfe.1	Tap	0.0
RX1:agcgain	Float	0.0
RX1:dfeadaptoff	Integer	0
RX1:dfeoff	Integer	0
RX1:freqofs	Float	1.00e-4
RX1:rotlin	String	../../../../../si_lib/spice/io_...
TX1:Tx_Strength	String	Tx Pow Reg 115 = 1.00
TX1:Table.ffe.-1	Tap	.0
TX1:Table.ffe.0	Tap	0.7
TX1:Table.ffe.1	Tap	-0.3

IBIS-AMI Channel Simulation





- Statistical Simulation
  - Computes eye statistics directly (no stimulus/waveform)
  - Models linear equalization
  - 1st order CDR model
- Time-Domain Simulation
  - Specific input stimuli, waveform output
  - Models DFE, adaptive equalization
  - Detailed CDR behavior
  - Simulates ~1,000,000 bits/minute

IBM Modelling Strategy

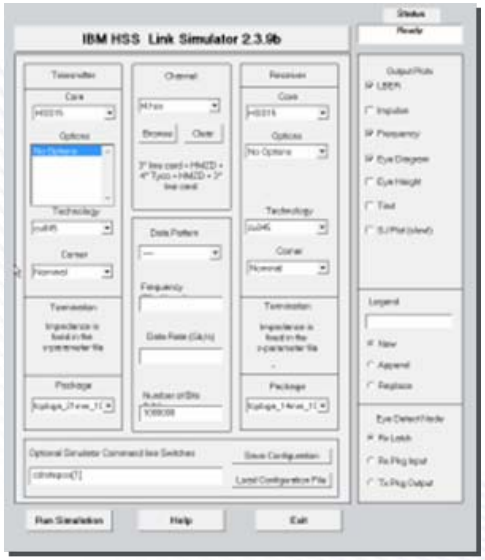
- Create a common set of models that can be configured to support multiple process nodes and technologies
- Use existing broadband characterization data for analog models
- Leverage existing code in HSSCDR where possible
- Models are not made public, but are freely available to customers

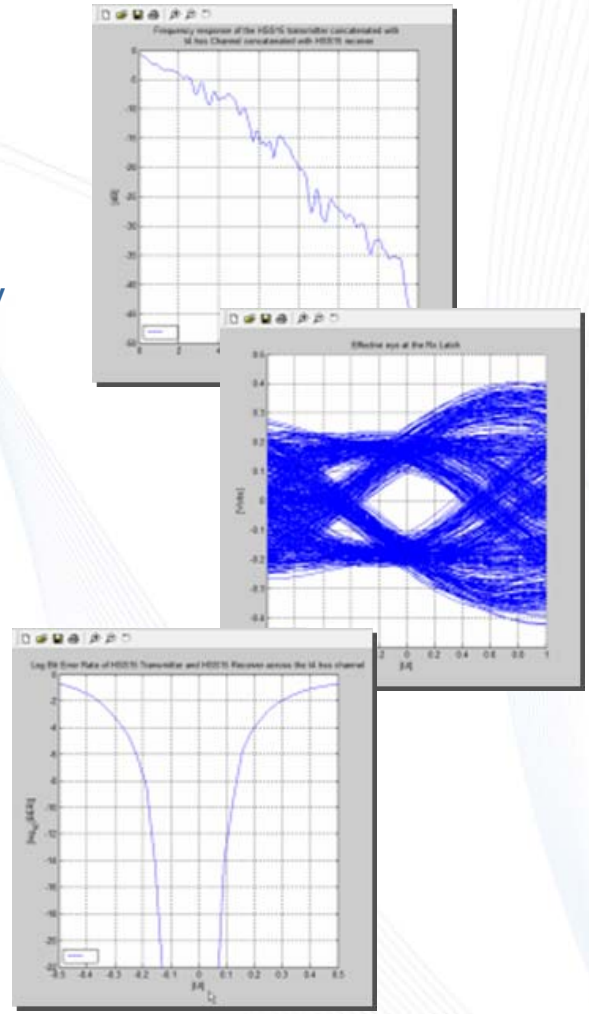
IBM Modelling Strategy (contd.)

- Previous models have included Spice, VHDL, Verilog-AMS, and others
- Present strategy supports IBIS-AMI and in-house HSSCDR proprietary simulator
- Core hardware is correlated in lab to HSSCDR
  - HSSCDR only supports IBM hardware
- HSSCDR and AMI code closely linked

IBM HSSCDR Simulator

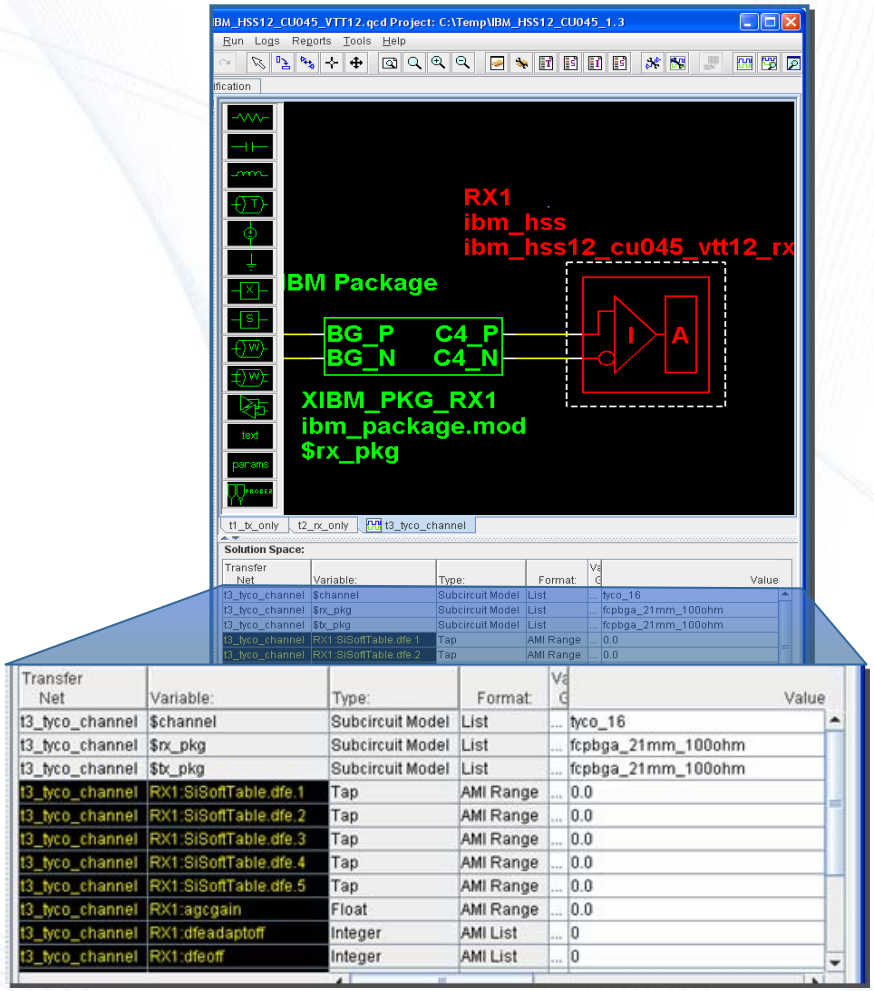
- Standalone channel analyzer and simulator
  - Channel analysis of on-chip parasitics and customer channels
  - Time-domain simulation at approximately 1 million bits/minute
  - Post-processing BER analysis down to 10^{-22} errors



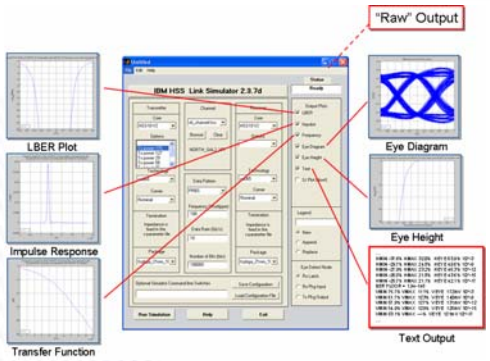


IBIS-AMI Model Parameters

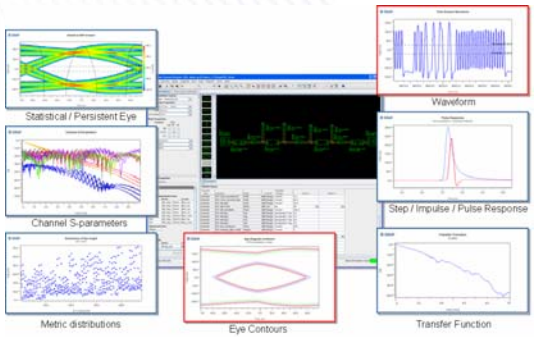
- IBIS-AMI models expose same simulation controls as HSSCDR
- Make comparing results easier & simplified migration process



Correlating Simulation Results



IBM HSSCDR



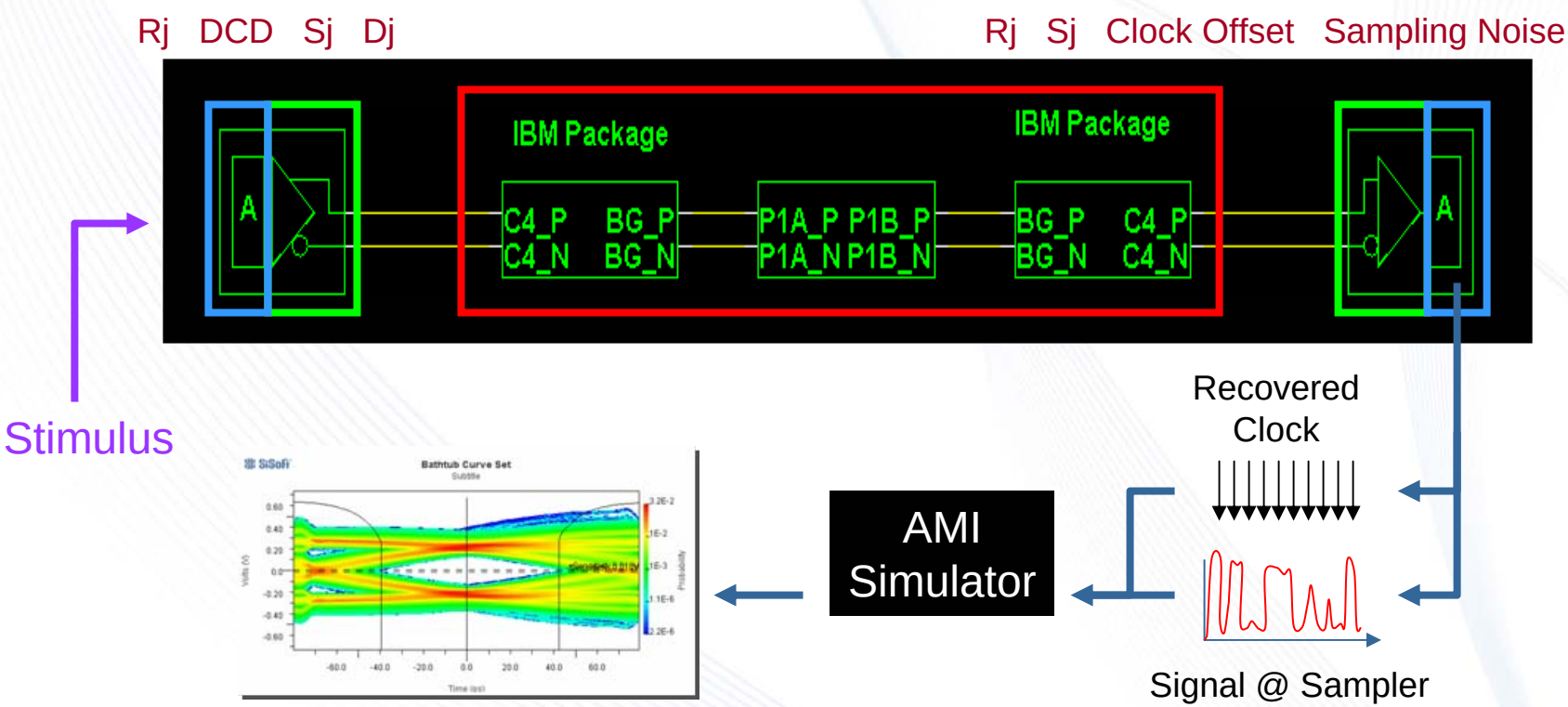
IBIS-AMI Simulator

What Compares with What?

- How to ensure analysis conditions are identical?
- Which outputs can be compared to which?
- What level of correlation is reasonable?
- Which behaviors are simulated?
- Which behaviors are extrapolated?

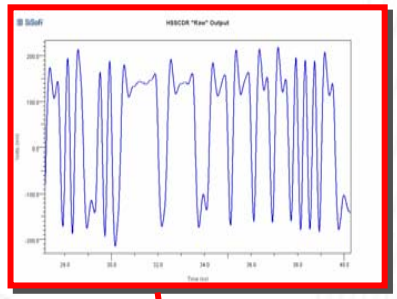
Simulation Elements

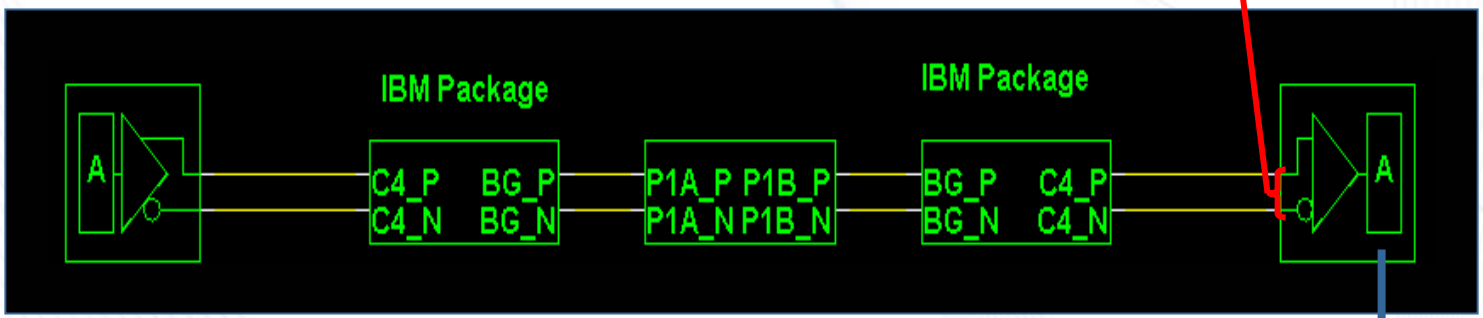
1. Channel Model
2. Analog Model (Impedance, Capacitance)
3. Algorithmic Model (EQ / Clock Recovery)
4. Stimulus
5. Post-processing: data / clock processing and presentation
6. Noise sources, extrapolation, noise processing



HSSCDR Visibility

Waveform @ RX Pad





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VMIN 53.1% VMAX ---% VEYE 121mV 10^-15

Eye Margin @ Sampler

Post-Processing / Extrapolation

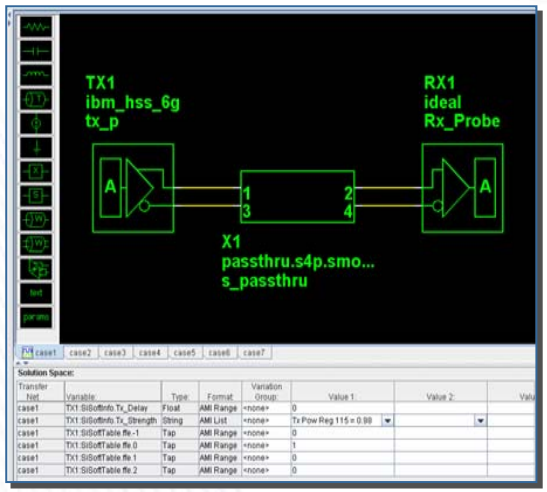
Recovered Clock

Signal @ Sampler

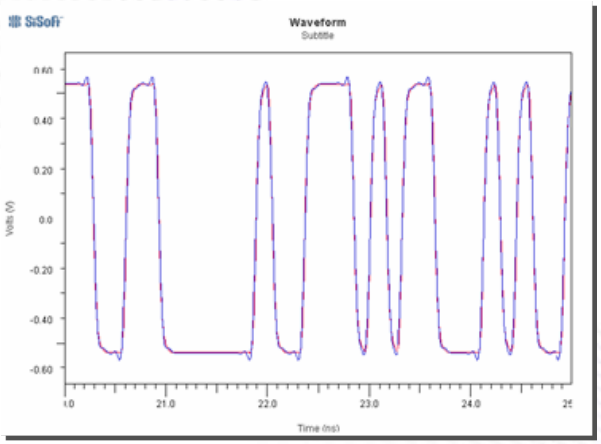
Correlation Strategy

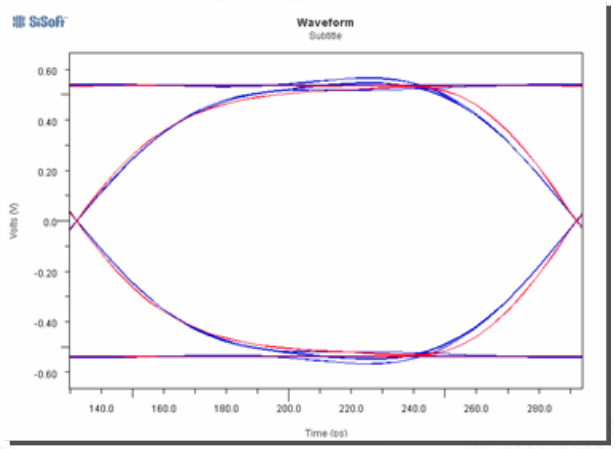
- Correlate everything up to the RX pad by overlaying waveforms
  - TX output impedance, slew rate, voltages
  - TX equalization
  - Channel model
- Correlate RX behavior based on eye height / width at different probability levels
- Include jitter / noise sources once TX / channel / RX behaviors are correlated
- Target correlation was within 5% of margins predicted by HSSCDR

TX Analog Driver Correlation

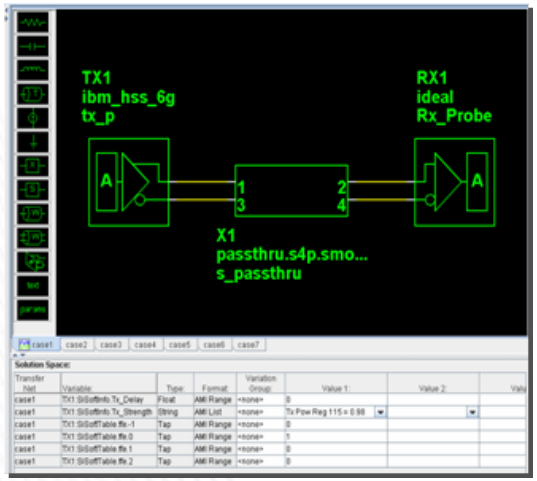


- Correlate analog (unequalized) TX model
  - Slew rate
  - Output impedance
  - Voltage level
- Simulation conditions
  - 6.25 Gb/s
  - TX EQ = Off
  - TXPOW = 115
  - Jitter = 0
  - WC, NC, BC Corners
  - 1000 cycles simulated

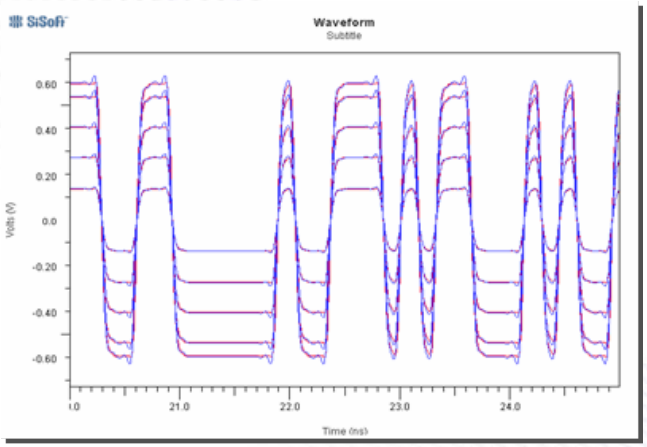


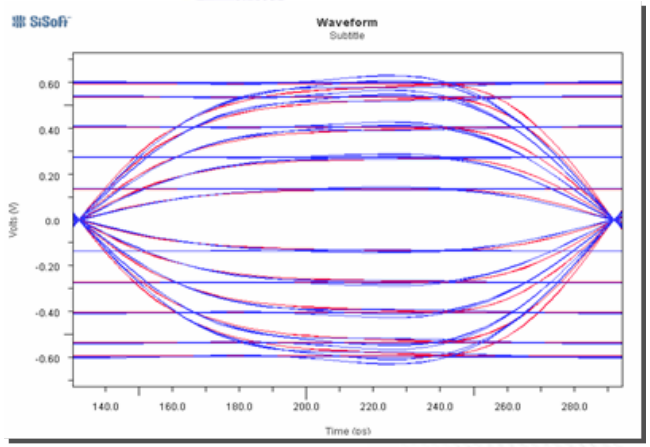


TX Output Swing Correlation

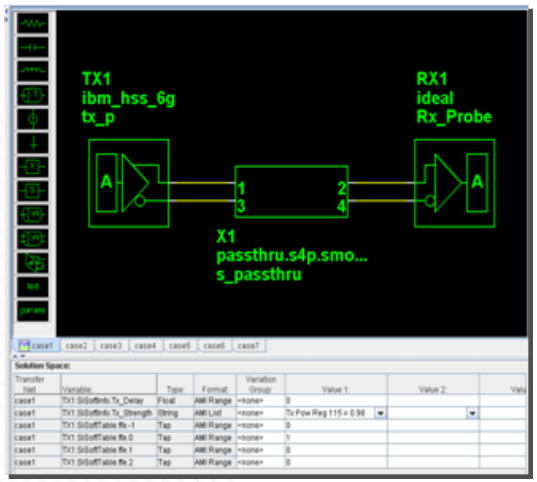


- Correlate TX power settings
- Simulation conditions
  - 6.25 Gb/s
  - TX EQ = Off
  - TXPOW = 29, 58, 86,115, 127
  - Jitter = 0
  - NC Corner
  - 1000 cycles simulated

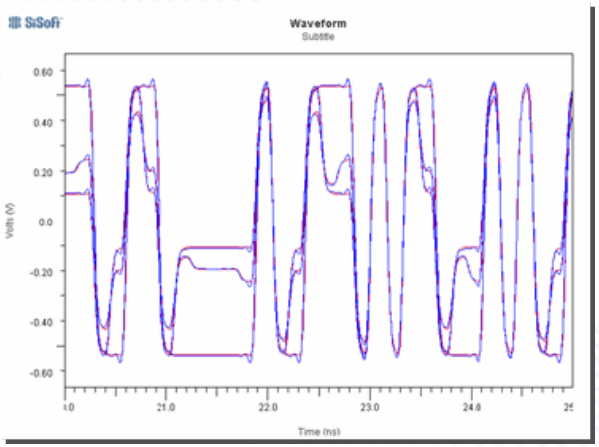


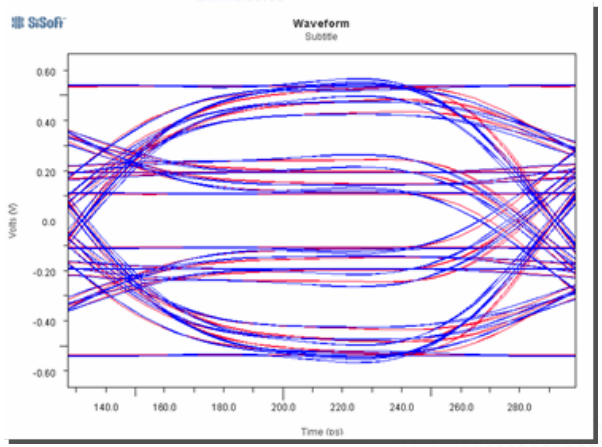


TX Equalization Correlation

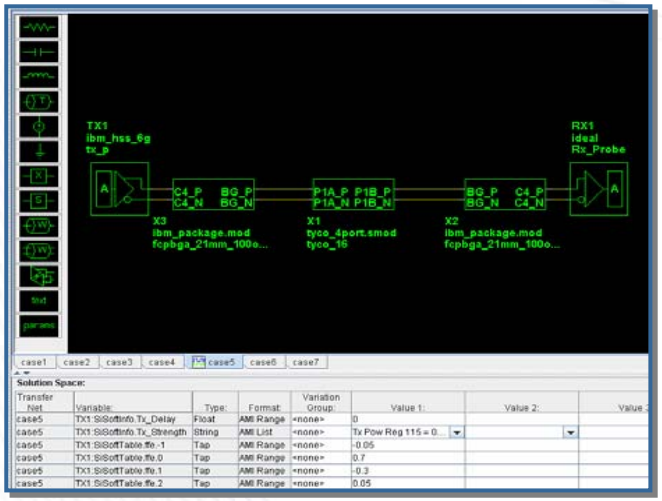


- Correlate TX algorithmic model EQ
  - Slew rate
  - Voltage levels
- Simulation conditions
  - 6.25 Gb/s
  - 4 TX EQ settings
  - TXPOW = 115
  - Jitter = 0
  - NC Corner
  - 1000 cycles simulated

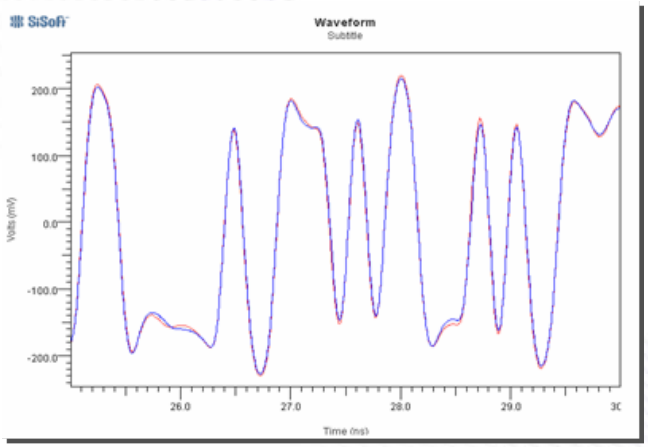


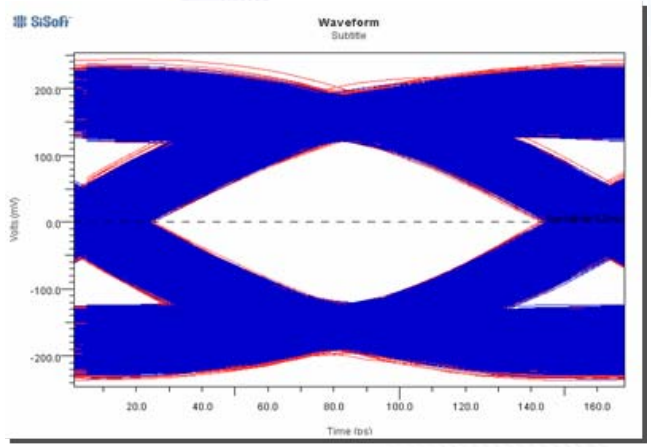


TX / Channel Correlation



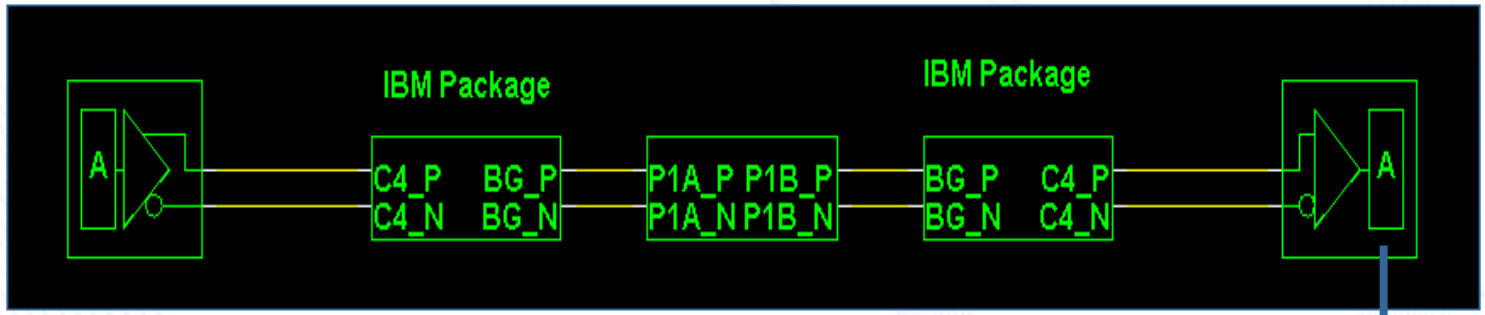
- Correlate full TX with full passive channel
  - TX with equalization
  - Packages + channel
  - Voltages and reflections
- Simulation conditions
  - 6.25 Gb/s
  - TX EQ = -0.05, 0.7, -0.3, 0.05
  - TXPOW = 115
  - Jitter = 0
  - NC Corner
  - 5000 cycles simulated





Correlating RX Eye Height / Width

- Requires combining recovered clock & equalized data behaviors to determine eye margin



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Simulated

Extrapolated

Post-Processing / Extrapolation

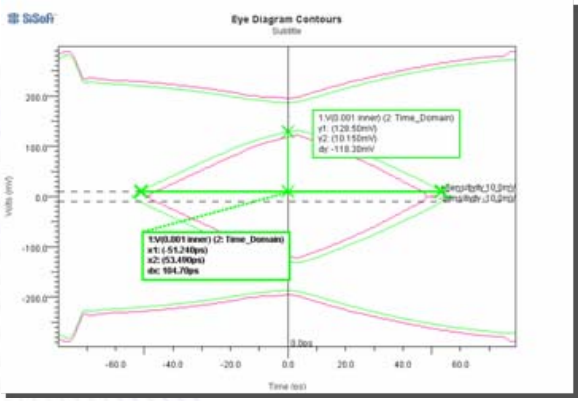
Recovered Clock

Signal @ Sampler

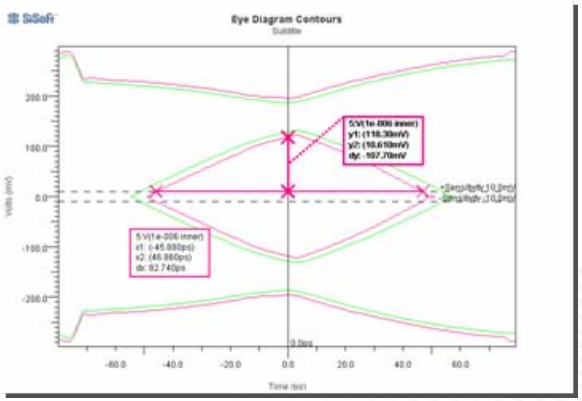
Eye Margin @ Sampler

RX Correlation Results

AMI 1E-3



AMI 1E-6



HSSCDR Output

HMIN -31.0% HMAX 33.5% HEYE 62.0% 10^-3
HMIN -28.6% HMAX 30.9% HEYE 57.1% 10^-6
HMIN -28.0% HMAX 30.3% HEYE 56.0% 10^-9
HMIN -27.8% HMAX 29.7% HEYE 55.5% 10^-12
HMIN -27.5% HMAX 29.1% HEYE 55.1% 10^-15

VMIN 71.9% VMAX 112% VEYE 117mV 10^-3
VMIN 66.0% VMAX 117% VEYE 108mV 10^-6
VMIN 63.2% VMAX 119% VEYE 103mV 10^-9
VMIN 62.1% VMAX 120% VEYE 101mV 10^-12
VMIN 61.2% VMAX 121% VEYE 99.8mV 10^-15

Simulated

Extrapolated

	AMI Eye Width	HSSCDR Eye Width	%	AMI Eye Height	HSSCDR Eye Height	%
1E-3	105ps	103ps	+1.9%	118mV	117mV	+0.9%
1E-6	92.7ps	95ps	-2.4%	107mV	108mV	-0.9%

Jitter and Noise Modeling

HMIN -31.0% HMAX 33.5% HEYE 62.0% 10^-3
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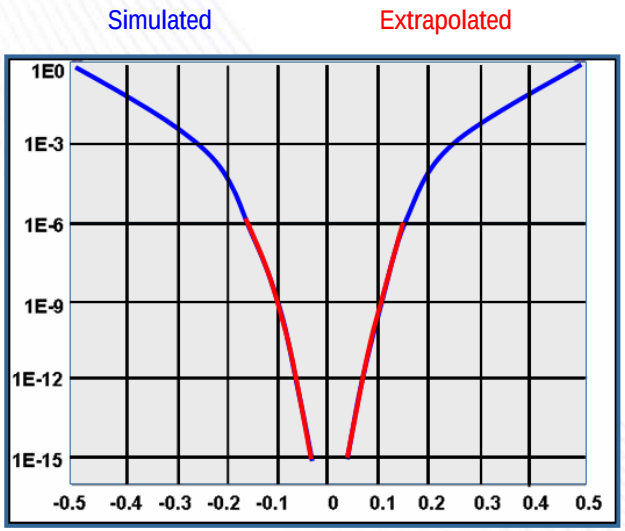
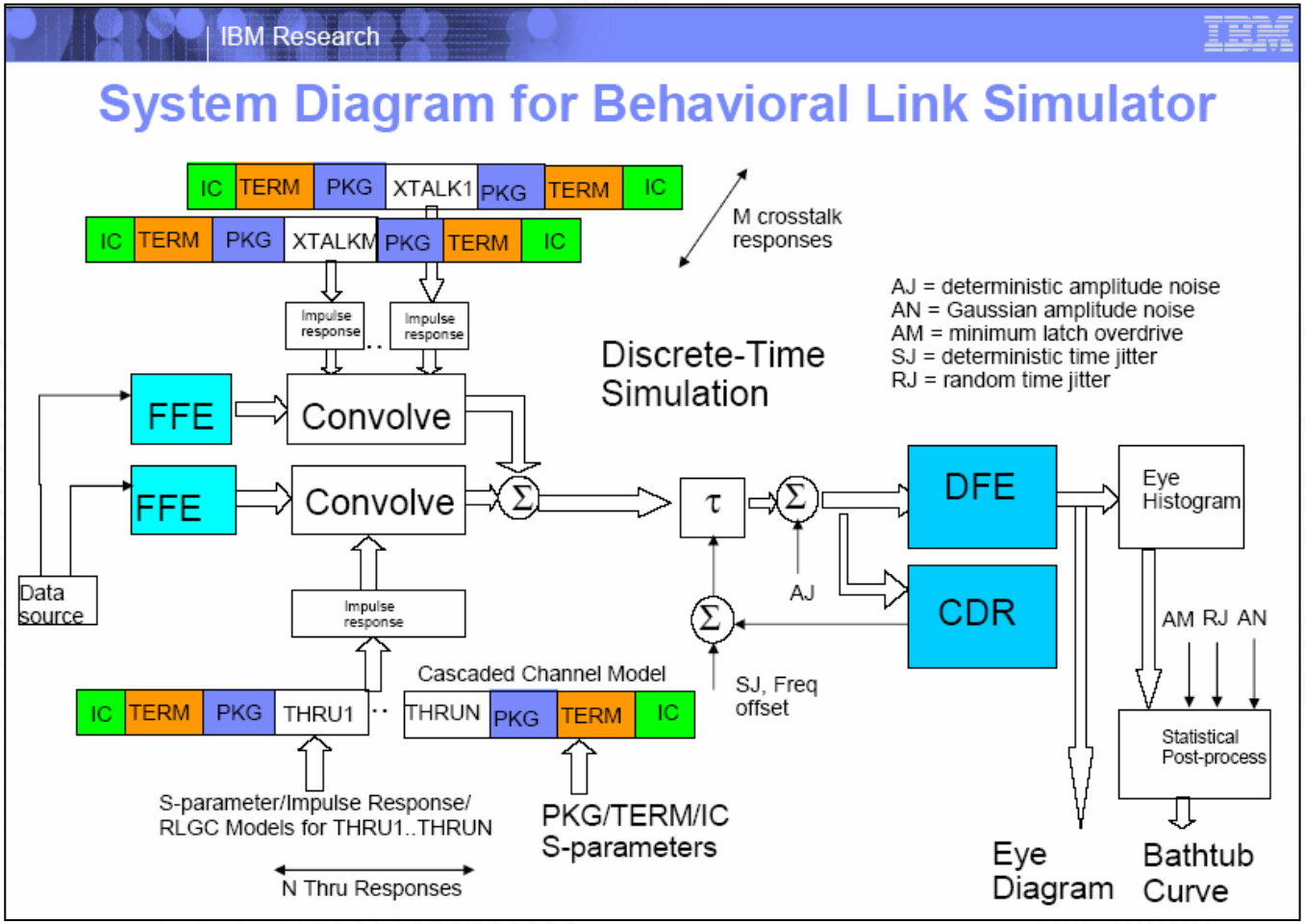


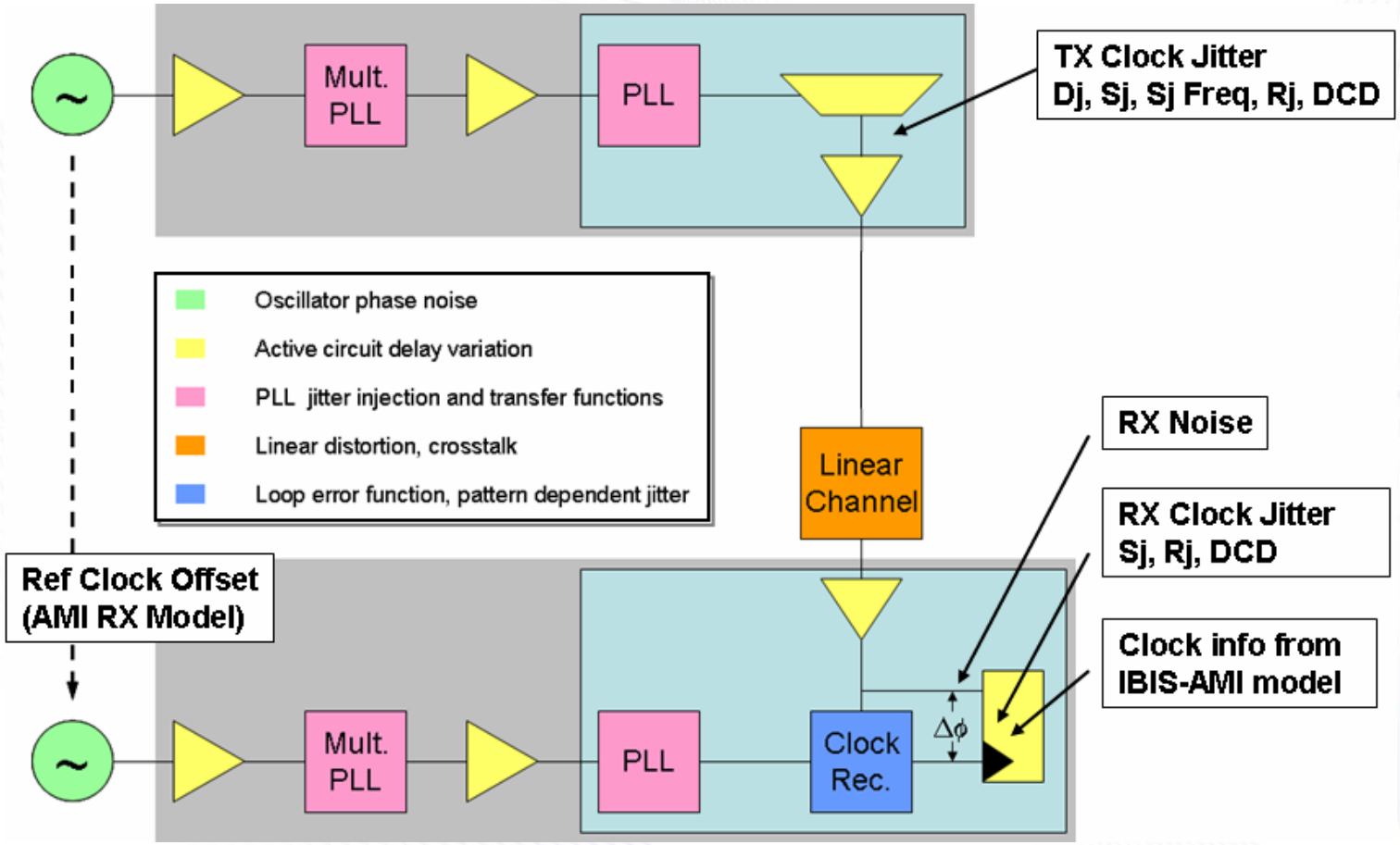
- IBIS-AMI simulations are typically 1M-50M bits long to characterize
  - Intersymbol interference (Dj)
  - TX DCD / channel
  - Crosstalk
- Random (unbounded) behaviors are best handled as budgets
- Channel simulators combine simulated & budgeted data to predict behavior at target design reliability levels

Jitter / Noise Modeling in HSSCDR

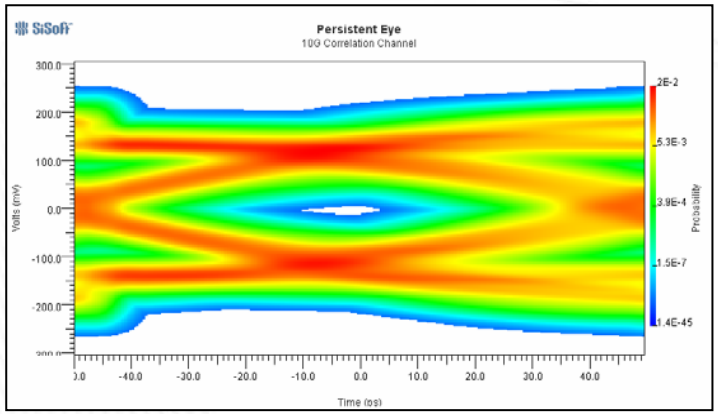


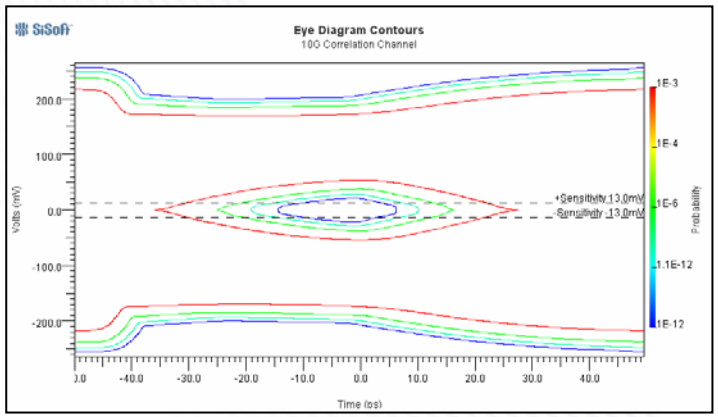
Troy Beukema, "Challenges in Serial Electrical Interconnects at 5 to 10 GB/s and Beyond", IEEE SSCS, 2007

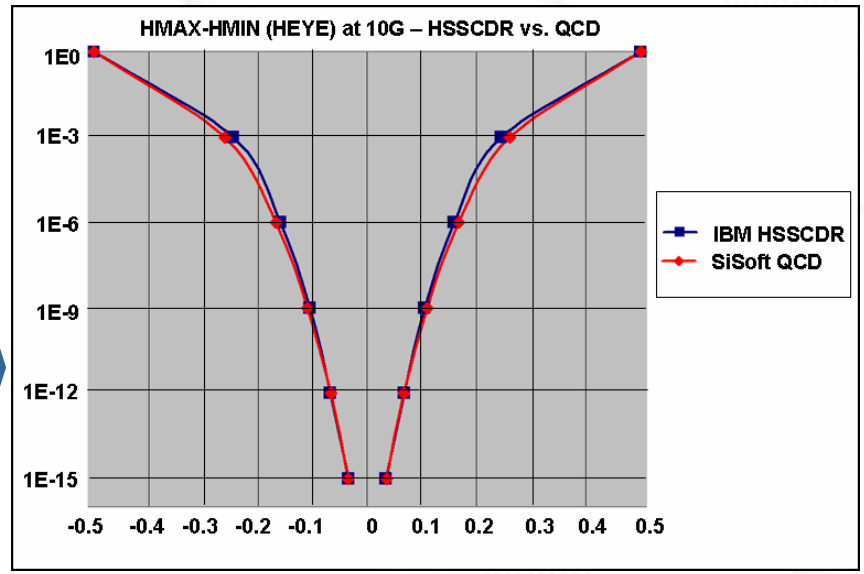
Jitter / Noise Modeling in AMI Simulator



10 Gb/s Correlation Results







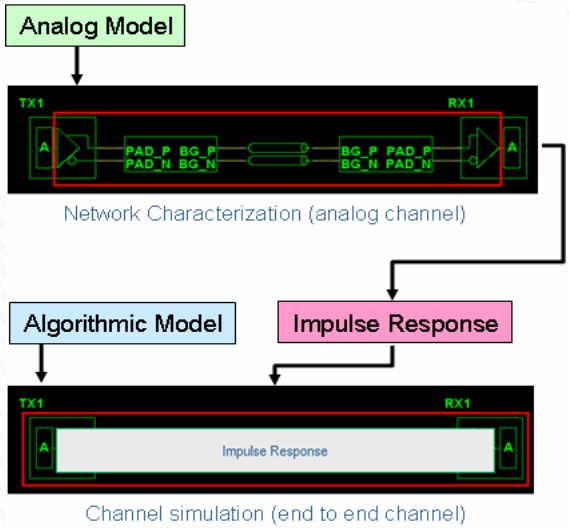
Eye margins match within target tolerances

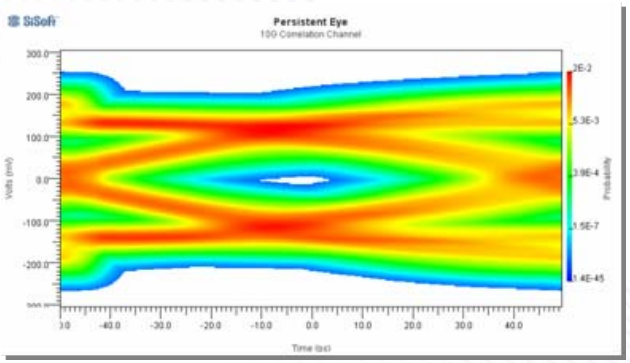
Simulation Performance

	HSSCDR	AMI
100K bits	43 sec	34 sec
1M bit	3 min 48 sec	3 min
10M bits	35 min 4 sec	28 min 50 sec

- IBIS-AMI provides performance on par with vendor simulation tools
- Simulations run on Dell D820 laptop, 2GHz T7200 CPU, 2 GB RAM

Summary





- IBIS-AMI simulation is a two step process
  - Network characterization
  - Channel simulation
- Channel simulation modes
  - Statistical simulation
  - Time-domain simulation
- IBIS-AMI models provide
  - Interoperability
  - Transportability
  - Performance
  - Accuracy