Modeling On-Die Power Supply Decoupling

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Outline

• Elements of an IBIS 5.0 model for Power Integrity simulation
• On-die power supply decoupling models
  ▶ Parasitic vs. non-parasitic
  ▶ Optimization of models
• Simulation results - Transistor-level vs. IBIS 3.2, 5.0
• Conclusions
IBIS 5.0 Power Integrity Modeling

- PI modeling requires [Composite Current], [ISSO PU], [ISSO PD] and a detailed model of decoupling capacitance

* Image from IBIS 5.1 Draft Specification
Power Supply Decoupling Elements

Bond Pad Layout Floorplan

- VDD, VSS, VDDQ, VSSQ
- Cap
- BDL
- ESD
- PU, DQ
- Pre-Driver Circuit powered by VDDQ
- Parasitic Decoupling

Bypass Cap

- I_byp
- C_p+b
- I_pre
- I_cb

Pre-Driver Circuit

- POWER Clamp
- GND Clamp
- L_VDDQ, R_VDDQ

Composite Current

Sig

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Parasitic Decoupling Capacitance

Capacitance

Note:
• Strongly frequency dependant
• Weakly voltage dependant

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Optimization of Parasitic Decoupling

~ 13.4pF - not insignificant

Transistor-level vs. Model
Optimization of All Decoupling

Transistor-level vs. Model

Adds ~450pF!
Simulation Setup

- DDR3 DQ I/O buffer, 1.5V
- PRBS pattern, minimum bit width of 1.25ns
- Typical corner
- Various On-die decoupling capacitance models included as SPICE models
- DQ1 + DQ2 switching (with different PRBS patterns) with fully coupled SPICE package model
No Decoupling Model
No Decoupling Model
Parasitic Decoupling Model Included

Good match to ringing behavior
Parasitic Decoupling Model Included
All Decoupling Modeled

Ringing behavior no longer matches. Why?
All Decoupling Modeled
Conclusions

• A complete model for on-die power supply decoupling must include models for parasitic caps and designed-in caps
• Simple, multi-stage RC circuits accurately model on-die decoupling circuits
• A method is needed for including complex decoupling models along with an IBIS 5.0 model
• More investigation needed to understand circumstances where IBIS 5.0 power-aware models do not match SPICE models