Practical HSIO Link Design and Optimization with Repeater and Retimer

Hsinho Wu, (Intel)
Masashi Shimanouchi, (Intel)
Mike Peng Li, (Intel)
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• Overview of Repeater and Retimer Characteristics
• High-Speed I/O (HSIO) System Design Considerations
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IBIS-AMI has syntax that supports the functionality in this presentation
Serial Data Communications: Data Recovery

• Most serial data transmissions send binary bits/symbols of information as a series of electrical or optical pulses in NRZ (Non Return to Zero) or PAM-n (Pulse Amplitude Modulation) format

• Devices And Transmission channel distort the signal:

• Receiver has to recover both the clock and the data.
3R Regeneration

• What is 3R Regeneration?
  – Reshape, Re-Amplify and Retime

  ➢ 1R: Amplify the signal and re-transmit
    – Amplifier

  ➢ 2R: Reshape and re-amplify
    – Equalizer

  ➢ 3R: Reshape, Re-amplify, and Re-time
    – CDR with/out Equalizer
Equalizers: Only solve part of link issues

- Do NOT Remove effects of **Random Noises**
  - Device Noise → Random Jitter
  - Random jitter accumulates over daisy chained serial links.

- CANNOT Compensate for **Clock Jitter**
  - Reference clock or input clock jitter
  - And clock jitter accumulates as well...

- CANNOT Compensate for **Clock Drift**
  - Reference/input clock frequency drift over time.

- DO NOT Understand **Data/Clock Transitions**
  - In a retimer, CDR uses data transitions to “lock” to the clock.
Repeater Functions and Characteristics

- A repeater performs 1R or 2R
  - Reshape: Channel equalization
  - Amplification: Buffer / Driver

- Three types
  - Linear: The driver stage maintain linear characteristics within majority part of signal amplitude
  - Nonlinear: A high-gain limiting-amplifier sits between the EQ stage and driver stage
  - Passive: Only contain a high-pass filter

- Characteristics
  - Only compensate channel ISI
  - Most of incoming jitter and noise will go through or be shaped by the repeater
    - Noise amplification and/or compressing
    - Non ISI Jitter reshaping
Overview of Retimer Characteristics

• **A retimer performs 3R**
  – Reshape: Channel equalization
  – Amplification: Buffer/Drive
  – Retime: Recover bit time and symbol

• **Handling of jitter and clock-domain noises**
  – Reset incoming random noise/jitter
  – Compensate clock jitter
  – Track/filter clock drift

• **Characteristics**
  – More capable input channel equalization
  – More capable output channel equalization
  – Consume more power and more expensive

• **However**
  – Most retimer won’t detect or recover symbol errors
  – Replace incoming jitter/noise with retimer’s intrinsic/transferred/output jitter/noise
System Design Considerations

• Repeater/retimer are used to boost link margins
• Repeater/retimer are not just band-aids to HSIO systems
  – Strategically deploy repeaters/retimers in part of the links so that the host transceivers can stay simple and low power for most of links
System Design Considerations -- Repeater

• **Use Repeater when**
  - Channel ISI is the only major concern
  - HSIO system with clean clock sources
  - Low crosstalk noise
  - Limited power budget
  - Limited available board footprint
  - Protocol-agnostic
  - Need transparent/linear view between host transceivers

• **Concerns**
  - Jitter/noise amplification by repeater’s CTLE
  - Jitter/noise conversion by repeater’s nonlinear drive stage
    - Convert residual ISI into uncompensable uncorrelated jitter
  - Fixed setting / no EQ adaptation
  - Potentially large PVT and part-to-part variations
System Design Considerations -- Retimer

**Use retimer when**

- More challenging channel characteristics
- Excessive jitter/noise conditions
- Poor reference clock quality
- HSIO links requires multiple-stage signal re-generation

**Concerns**

- Cost
- Power consumption
- Latency
- Data rate range coverage
  - Retimers’ frequency range is not continuous in general
- Protocol dependent
- BER floor with low probability bit errors
- Not transparent between host TX and RX
Repeater/Retimer Placement

• General principles

\[ I_{L_{\text{Channel}}} - (E_{Q_{\text{HostSerDes}}} + E_{Q_{\text{RepeaterRetimer}}}) > 0 \]

• Need to including PVT and part-to-part variations from channel components and devices

\[ I_{L_{\text{Channel}}} - I_{L_{\text{ChannelPVT}}} - (E_{Q_{\text{HostSerDes}}} + E_{Q_{\text{HostSerDesPVT}}} + E_{Q_{\text{RepeaterRetimer}}} + E_{Q_{\text{RepeaterRetimerPVT}}}) > 0 \]
Repeater/Retimer Placement (cont.)

- **Repeater placement**
  - Linear repeater
    - Theoretically, linear repeater can be placed anywhere within the link
    - However, limited linear range will restrict the placement location
  - Nonlinear repeater
    - Uncompensated ISI after a nonlinear repeater will become uncompensable jitter
    - Optimal location will be at the location where the residual jitter is minimal at repeater output
  - Need to simulate and evaluate end-to-end link as a whole to correctly gauge the real performance of a repeater link
• **Retimer placement**
  – Placement solution space is more relaxed than that of repeaters’ due to
    • More capable retimer EQ (both input EQ and output EQ)
    • Jitter cleaning / jitter replacement
  – Place retimer closer to host TX if host TX or reference clock source is noisy
  – Place retimer closer to host RX if host RX has insufficient EQ capability for the link
  – Place retimer in mid-length location for maximum link reach extension

• **Link Performance Evaluation**
  • Can evaluate link performance in segments
  • Need to evaluate link margin at retimer EQ stage output to prevent unexpected BER floor issues

• **Physical constraints**
  – Power supply arrangement for repeaters and retimers
    • Proximity of connectors, where power is delivered, is common
    • Impedance discontinuity caused by the connectors can cause issues
  – Crosstalk caused by signal fan-in/-out at repeater/retimer location
Experiment: HSIO Link with a Linear Repeater

Host Transmitter
Front-end Channel
Repeater Model
Back-end Channel
Host Receiver
Experiment: HSIO Link with a Linear Repeater (cont.)
Experiment: HSIO Link with a Nonlinear Repeater
Experiment: HSIO Link with a Nonlinear Repeater (cont.)
Experiment: HSIO Link with a Retimer
HSIO Link with a Retimer
Stage 1: Front-end Link Optimization

February 3, 2017
DesignCon IBIS Summit
Santa Clara, California
HSIO Link with a Retimer
Stage 1: Back-end Link Optimization

Retimer TX Model

IBIS-AMI Transmitter

Transmission Term bcx4p ID = 3

Transmission Package bcx4p ID = 2

Transmission Trace2 x4p ID = 4

Receiver

TP1

TP2

TP3

TP3 Bathtub
HSIO Link with a Retimer: Stage 2: Retimer Stress Test

- **26 Gbps Front-end Link Stress Test**
- **SJ = 0.4 UI 1 MHz**
- **SJ = 0.4 UI 20 MHz**
- **February 3, 2017**
- **DesignCon IBIS Summit Santa Clara, California**
HSIO Link with a Retimer: Stage 3: End-to-End Link Test

SJ = 0.4 UI
20 MHz

Retimer Model

PDF Eye Diagram

BER Bathtub

BER Floor

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DesignCon IBIS Summit
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Gaps and Future Developments

• **Gaps**
  – Missing repeater/retimer information for accurate performance evaluation
    • Equalizer/Receiver jitter/noise/sensitivity
    • Variations / Corners
  – Boundary of linear behaviors and nonlinear characteristics
    • Especially for repeaters

• **Future Development**
  – More accurate repeater/retimer device models and device characteristics disclosure
  – Include repeater/retimer in standards
    • Retimer support is included in PCI-Express 4.0

*Note: IBIS-AMI supports Repeaters and Retimers*
Thank you!