Effective simulation set up with latest IBIS models

cooporation with IEC 63055 / IEEE 2401

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Mutual Communication
Design Consistency
Shorten Development Time

Enabled by

IBIS and LPB Standard formats
Contents

• Introduction
  • Background of technology matters
  • What is IEC 63055/ IEEE 2401?
  • JEITA delegates & History of discussion IBIS and JEITA

• Technical aspect between IBIS and IEC 63055/ IEEE 2401
  • Issues on IBIS simulation
    • Sample of IEEE 2401, sample of IBIS simulation set up
  • Concerns and required actions.

• Conclusion & Proposal
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• Conclusion & Proposal
  • Joint work for harmonization with latest IBIS and IEEE 2401 (and future)
  • IEEE 2401-2020 update – join P2401 working group if you are IEEE-SA member
Background of technology matters

In Technical, Increasing of connected node causes the long time work,

- Conversion work from someone’s info. To someone’s work environment
- Mistakes may occur in manual connection, but just watching the results, mistake cannot be detected.
- As a results, it takes long time for verification work to correct setup

Engineer's valuable time is lost in such a wasteful work. Engineers have to spend time for innovation.

In Business, delay to put the product in market. Design technology leads to business success.
What is IEC 63055/ IEEE 2401-2015?

Standard format for **LSI Package Board (LPB)** interoperable design.

For effective information exchange in supply chain.

<table>
<thead>
<tr>
<th>Individual</th>
<th>LSI Package</th>
<th>Passive Board</th>
</tr>
</thead>
<tbody>
<tr>
<td>Confidential information</td>
<td>Design detail</td>
<td>Design Detail</td>
</tr>
<tr>
<td>Interoperable information</td>
<td>Behavioral</td>
<td>Behavioral</td>
</tr>
</tbody>
</table>

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1. Project Manage (**M-Format**)  
2. Netlist (**N-Format**)  
3. Component (**C-Format**)  
4. Design Rule (**R-Format**)  
5. Geometry (**G-Format**)  

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**IEC63055/IEEE2401**

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**Models, IBIS, SPICE, etc.**

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6. **Glossary**
What is IEC 63055/IEEE 2401-2015?

In the deployment of electronic products...

Die Size
Pad location
Spice Model correspondence

Die models
IBIS/SPICE
CPM/LPM

Package size
Terminal location
Spice/IBIS/S-para model correspondence

Package models
IBIS
S-para SPICE

Simulation Platform

C-Format

Die mount
Coordinate,
Orientation,
Flip, etc.

C-Format

Package mount
Coordinate,
Orientation,
Flip, etc.

C-Format

Spice Model
correspondence

R-Format

Line/Space
Via pitch/size/hole
Layer Stuck up
Material parameter

G-Format

PWB Routing
/Plane

N-Format

Netlist

R-Format

Connectivity

G-Format

Package Lyout
Wire Bonding
Layer stuck-up
Via, material

M-Format

Combination of C, G, R,
N which constitute the
analysis target
Delegates of JEITA

Japan Electricals and Information Technology Industries Association

Semiconductor Industry Association in Japan

Semiconductor Standardization Committee in Japan

Semiconductor & System Design Technical Committee

Chair: Yoshinori Fukuba (from Toshiba)

LPB (LSI Package board) interoperable design sub-committee

LPB modeling Working Group / IBIS Task Group

Leader: Kazuki Murata (From Ricoh)

- IBIS Summit Japan coordinator

http://jeita-sdtc.com/worldwide/

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History of IBIS & LPB

1. 2013 Asian IBIS Summit Yokohama, Mr. Murata presented on V5.x, AMI’s consideration. After that Fukuba talked with Mr. Michael Mirmak, former chairperson IBIS Open Forum, about the cooperation between IBIS & LPB.

2. Mr. Tanaka introduced LPB concept at 2014 IBIS Summit @ DAC (San Francisco)

3. Fukuba presented LPB concept at 2015 Asian IBIS Summit Yokohama (almost the same content as Mr. Tanaka’s)

4. Mr. Murata presented the chip model at 2017 Asian IBIS Summit Akihabara, Tokyo, after that Fukuba discussed cooperative relationship with Mr. Mike LaBonte.
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Overall Simulation time

- Parameter collection: 2 weeks
- Setup: 1 day
- Calculation: EDA / computer / Academic challenge

Common formats:
- List of information, exchange format, common terms & definitions: 2 days
- Community / e-commerce

Extremely shorten total simulation time
Waste of time – Pin connection

It is complicated to assign IBIS model to component in board layout data. Too many [Pin]s to connect manually!

Example: number of pins.

<table>
<thead>
<tr>
<th>DDR4 64bit</th>
<th>FPGA-A</th>
<th>FPGA-B</th>
<th>SoC-A</th>
<th>SoC-B</th>
</tr>
</thead>
<tbody>
<tr>
<td>114</td>
<td>2892</td>
<td>2912</td>
<td>1760</td>
<td>2597</td>
</tr>
</tbody>
</table>

Some tools can connect them automatically. But, we can’t always get correct result by keyword matching method. Is [Pin] name physical pin name? A1,A2,A3,B1,,,,
LPB - Explicit connection

LPB can contains the correspondence of IBIS [Pin] to chip pin’s physical position.

LPB supports IBIS(.ibs, .pkg, .ebd), SPICE, Spara, Verilog, etc.

Physical position

Link LPB <port> to IBIS [Pin]
SI/PI/EMC designers have to use various tools.
for die tools, for PKG tools, for Board tools, simulators, CAD,,,

Therefore it is necessary to convert the data many times.
Format A -> Format B -> Format C
Are A and C the same layout?
It is complicated to modify the data manually to be the same.
LPB - Seamless design

LPB is mainly XML format, and IEC and IEEE standard. Various tools support LPB. Therefore data conversion is unnecessary.

LPB has module’s physical shape data and layout data. die outline, PKG outline, die pad shape, PKG ball shape, etc. P/G plane shape, transmission line shape, layer stackup, etc. And, these modules are linked to IBIS models or other models. LPB makes it easy to proceed design phase.
Waste of time – Re-setup

Board layout changes may be occurred many times during design phase. SI/PI/EMC designers also have to do simulation many times.

1st design
2nd design
modify cap.
add plane
3rd design
...
Once you setup simulation by using LPB, you can reuse it without re-setup.

1st design

2nd design
modify cap. add plane

3rd design

...
Example of LPB

```xml
<module name="die" type="LSI" shape_id="die_shape">
  <socket name="die_pads">
    <port id="1" name="DQ0" x=100 y=200 />
    <port id="2" name="DQ1" x=100 y=300 />
    ...
  </socket>
</module>

<module name="pkg" type="PKG" shape_id="pkg_shape">
  <socket name="pkg_balls">
    <port id="A1" name="DQ0" x=500 y=1300 />
    ...
  </socket>
</module>

<module name="brd" type="PWB" shape_id="brd_shape">
  <socket name="brd_edge">
    <port id="1" name="sig1" x=800 y=10500 />
    ...
  </socket>
</module>

<component>
  <placement inst="mem1" ref_module="die" x=0 y=0 />
</component>

<component>
  <placement inst="dram_die" ref_module="die" x=0 y=0 />
  <placement inst="mem2" ref_module="pkg" x=700 y=5000 />
</component>
```

Instantiation

Instantiation
Who provides LPB?

For the components, LPB files should be released by component vendors. Some commodity parts are getting ready!
JEITA has released the sample data and tools for either vendor or user to create LPB files.
In case you have to make LPB by yourself, use ‘LPB design kit’ released by JEITA that can export simple LPB files.

http://www.lpb-forum.com/lpb-open-source-project/download/
Sorry, this web site is Japanese.
How to make LPB with IBIS

Example: DRAM

Import IBIS

[Component]

IBIS Viewer

[Pin]

[Component]
How to make LPB with IBIS

Example: DRAM

Export LPB

LPB

with IBIS

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In many cases, **IBIS6.0 doesn’t have die pad information.** Therefore IBIS is linked to LPB PKG module.

If you obtain .pkg file and .ibs file without package model, you can use them for PKG module and DIE module separately. Then PKG module can be stacked with DIE module.
[Interconnect Model] can define die pad. In this case LPB DIE module may be available.

But, there is a possibility that the tool recognizes each model twice – **double counting problem**.
## Concerns and required actions

**Concern:** double count of die and PKG model in case LPB with IBIS7.0  
**Action:** add the optimal function to LPB ?

<table>
<thead>
<tr>
<th>LPB</th>
<th>[Model]</th>
<th>[Package]</th>
<th>[Pin]</th>
<th>[Package Model]</th>
<th>[Interconnect]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Example of modification to correspond to IBIS 7.0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>&lt;ibis:ref_port component=aaa/&gt;</td>
<td>✓</td>
<td>✓</td>
<td>( Depends on simulator )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>&lt;pkg type=short/&gt;</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>&lt;pkg type=package/&gt;</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>&lt;pkg type=pin/&gt;</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>&lt;pkg type=package_model/&gt;</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>&lt;interconnect name=xxx/&gt;</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>&lt;ibis:ref_port component=aaa without_buf=yes/&gt;</td>
<td>✓</td>
<td>✓</td>
<td>( Depends on simulator )</td>
<td></td>
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</tr>
<tr>
<td>&lt;interconnect name=xxx/&gt;</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
</tr>
</tbody>
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<pkg/> and <interconnect/> can be written together.  
More than one <interconnect/> can be written.
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Conclusion & Proposal

Conclusion

• IEC 63055 / IEEE 2401 helps shorten the setup of IBIS simulation and prevent mistakes.

• IBIS 7.0 affects IEC 63055 / IEEE 2401 interface scheme

• IEC 63055/ IEEE 2041 will be updated soon for 2020 version
  • This time, there is possibility to implement the additional option to cooperate with IBIS 7.0. (this will be discussed in JEITA.)

Proposal

• For future, establish Joint work for harmonization with latest IBIS and IEEE 2401.
  • To join the web meeting or to hold the meting with IBIS summit.

• IEEE 2401-2020 revision work – join P2401 working group if you are IEEE-SA member

Thank you!
Reference IEEE P2401

project 2013 http://grouper.ieee.org/groups/2401/

Working Group for Standard Format for LSI-Package-Board Interoperable Design (C/DA/LPB)

This project is sponsored by the IEEE Computer Society/Design Automation (C/DA).

Title: Standard Format for LSI-Package-Board Interoperable Design

Scope: This standard defines a common interoperable format used for the design of (a) Large Scale Integrated (LSI) circuits, (b) Packages for such LSI circuits and (c) Printed Circuit Boards on which the packaged LSI circuits are interconnected. Collectively such designs are referred to as “LSI-Package-Board” designs. The format provides a common way to specify information/data about the project management, net lists, components, design rules, and geometries used in LSI-Package-Board designs.

Purpose: The general purpose of this standard is to develop a common format that LSI-Package-Board design tools can use to exchange information/data seamlessly, as opposed to having to work with multiple different input and output formats.

Need for the Project: Because techniques for the design of LSI circuits, packages and printed circuit boards evolved separately, the software used for such designs typically employ different formats even when accessing identical information and data. The use of these differing formats presents a barrier to the natural flow of information between software tools used for LSI-Package-Board design. The common format to be standardized will eliminate this barrier, and achieve seamless information/data exchange between LSI-Package-Board software tools.

For more information, view the approved PAR.

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IEC 63055/
IEEE 2401-2015

project 2017 → IEEE 2401-2020

Approved PAR, expected IEEE board committee approval by Mar. 2018