Interconnect Task Group Report

with BIRD189.5 Overview

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Agenda

- History
- Principles of the Interconnect Proposal
  - Structure
  - Fundamental Keywords
  - Terminals, Models, Sets, and Groups
- What Has Changed Since DesignCon 2017
- Summary and Next Steps

Status Overview

- The Interconnect Task Group has been developing this proposal since 2014
- BIRD189.4 was submitted to the Open Forum, but is now out-of-date
  - http://www.ibis.org/birds/
- BIRD189.5 is in the final stages of preparation
  - http://www.ibis.org/interconnect_wip/ (as Draft 16)
  - Expected to be submitted to Open Forum in February 2018
- Intended for IBIS Version 7.0

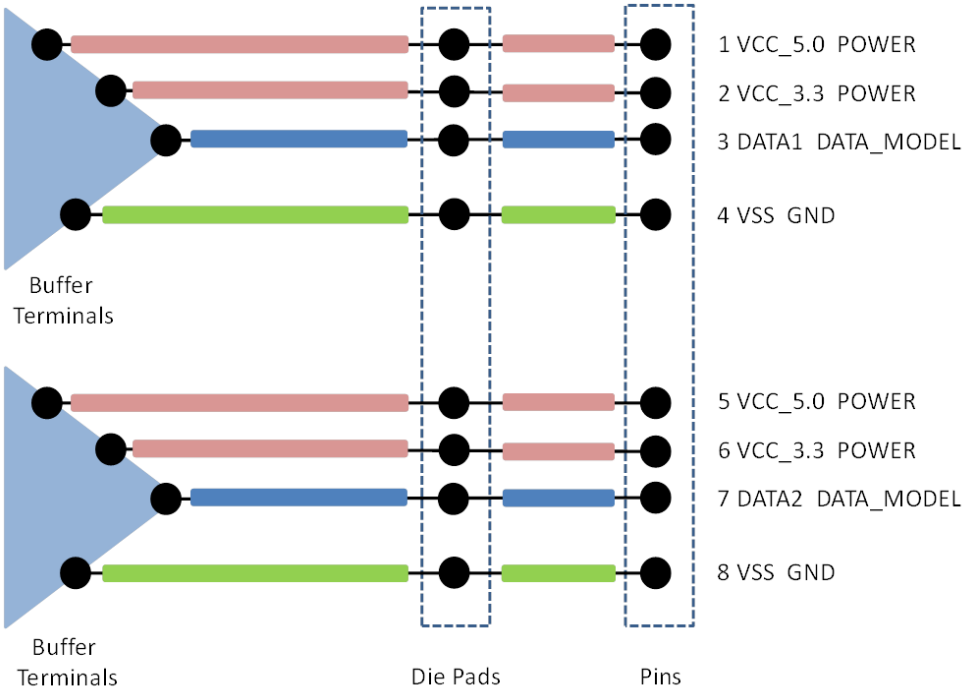
Key changes in draft BIRD189.5 are summarized below

Features of the Interconnect Proposal

- Supports…
  - IBIS-ISS and Touchstone models (common in industry)
  - Both I/O and supply (POWER and GND) connections
  - (New) optional Die pad interface between Pins and Buffers
  - I/O pin_names as terminal qualifiers
    - *May have optional Aggressor_Only designation*
  - POWER and GND terminal qualifiers by pin_name, pad_name, signal_name or [Pin Mapping] bus_label for rail connections with direct or combined terminals
  - Many other features not covered here

This approach links IBIS packages to common industry interconnect modeling data formats

Terminals at Buffer, Die Pad and Pin Interfaces



Original IBIS (4.0 and earlier)

- Pins are explicit
- Buffer terminals implicit in [Model]
- Die pad terminals same as buffer terminals
- Packages defined connections between pins and buffers

Current Proposal

- Die pad terminals are now explicit
- Buffer terminals are now explicit
- [Pin]s are…. still pins
- Separate interconnect definitions can be created between …
  - Pin-to-Die pad terminals,
  - Die pad-to-Buffer terminals,
  - Pin-to-Buffer terminals (still) supported

Keywords and Subparameters (Limited Discussion Here)

- [Bus Labels] | available for most keywords
- [Die Supply Pads] | pad_name, optional bus_label
- [Interconnect Model]/[End Interconnect Model]
  - Unused_port_termination <Open | Ref. | Res.> | Unused port ref. Z
  - Param | parameter passing
  - File_IBIS-ISS | names IBIS-ISS file
  - File_TS | names Tstone file
  - Number_of_terminals=<value> | number of terminals
  - <terminal lines> | described later
- [Interconnect Model Set]/[End Interconnect Model Set]
- [Interconnect Model Set Group]/[End Interconnect Model Set Group]
  - New and changed from “Selector”

[Interconnect Model]

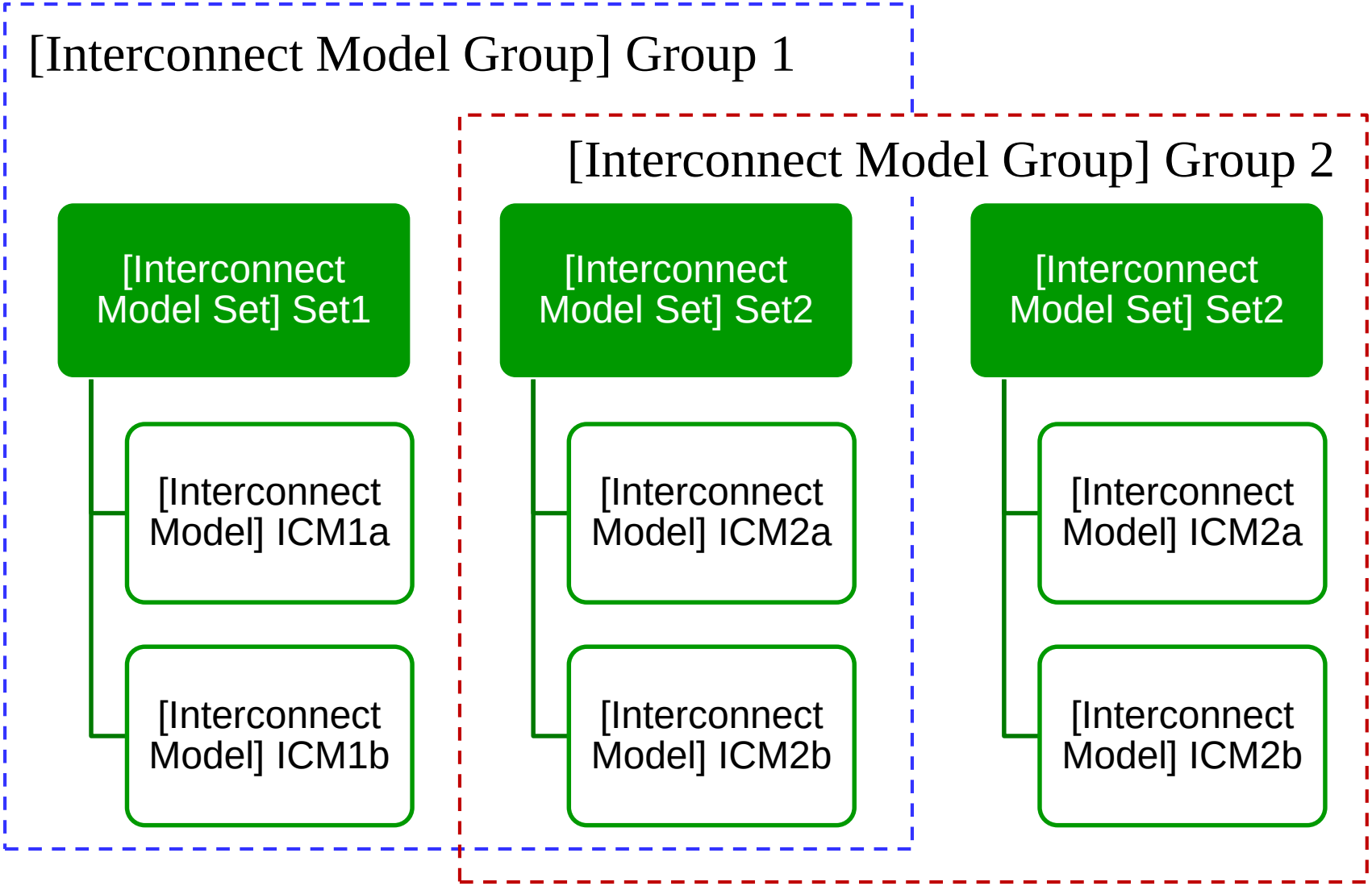
- [Interconnect Model] <interconnect_model_name>
  - Connections between terminals with IBIS-ISS or Touchstone files
  - Terminal connection points at Buffer, Die pad, or Pin interfaces
  - Identifies rail or I/O terminals
  - Allows pin_name, signal_name, pad_name, or bus_label terminal qualifiers for rails (and pin_name for I/O terminals)
  - Identifies whether a coupled signal is only an aggressor or also "experiences" coupling from other sources

How package and on-die electrical information is generated and delivered today

[Interconnect Model Set]s
[Interconnect Model Set Group]s

- [Interconnect Model Set] <set_name>
  - Encapsulates one or more Interconnect Models
- [Interconnect Model Group] <group_name>
  - Names one or more Interconnect Model Sets to be used together
  - Used to establish a complete path for selected buffers
  - <group_name> helps identify buffers selected for simulation
- Some Example Groupings and Applications
  - Separate groups: one per interface (e.g., memory, network)
  - Separate groups for coupled vs. single-line simulations
  - Different sets for different power delivery network complexities
    - *POWER connected at single pin, single buffer terminal*
    - *POWER connected through multiple pins, rails to individual buffer terminals*

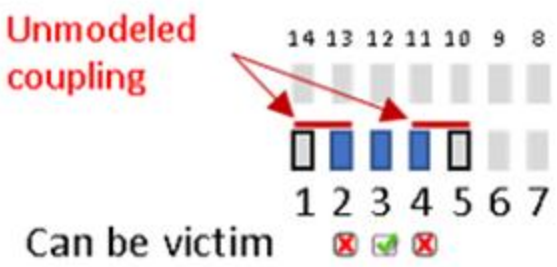
Models Are Grouped Hierarchically



Key Changes in Latest Draft

- Clarification of Aggressor_Only treatment
  - Not all crosstalk in possible the physical design will be represented in the model for terminals labeled “Aggressor_Only”

Terminal_type qualifiers and, here, pin names (e.g., model terminal 1 is associated with pin 2)




```
1  Pin_I/O      pin_name  2  Aggressor_Only
2  Pin_I/O      pin_name  3
3  Pin_I/O      pin_name  4  Aggressor_Only
4  Buffer_I/O   pin_name  2  Aggressor_Only
5  Buffer_I/O   pin_name  3
6  Buffer_I/O   pin_name  4  Aggressor_Only
```

- The model maker is informing the user and tool that all potential crosstalk is included in the model for Pin 3
  - Both what it generates and what it is subject to

A_gnd Added

- A_gnd is an optional declaration available for any terminal
  - This formally adds “ground” to the same hierarchy level as pin, die pad and buffer
- This permits simulator reference (ideal node 0) to be connected to any point
  - A_gnd may be used any number of times with IBIS-ISS files
  - A_gnd may only be used once for Touchstone files, for the N+1th terminal

An A_gnd Example

- An 8-port S-parameter in a 9-terminal structure

```
[Interconnect Model Set]        Full_TS_IO_A_gnd_reference

[Interconnect Model]            Full_TS_IO_A_gnd_reference
File_TS          full_ts_buf_pin_io.s8p
Number_of_terminals = 9
Full_TS_IO_A_gnd_reference
1  Pin_I/O       pin_name       A1     |  DQ1           DQ
2  Pin_I/O       pin_name       A2     |  DQ2           DQ
3  Pin_I/O       pin_name       A3     |  DQ3           DQ
4  Pin_I/O       pin_name       A4     |  DQ4           DQ
5  Buffer_I/O    pin_name       A1     |  DQ1           DQ
6  Buffer_I/O    pin_name       A2     |  DQ2           DQ
7  Buffer_I/O    pin_name       A3     |  DQ3           DQ
8  Buffer_I/O    pin_name       A4     |  DQ4           DQ
9  A_gnd                               |  Reference terminal
[End Interconnect Model]
[End Interconnect Model Set]
```

Other Recent Changes

- Unused_port_termination is back and extended
  - "Resistance" added, with numerical argument
  - Supports tool termination to defined single value of resistance
- Used with Touchstone files
  - Unused_port_termination <Open | Reference | Resistance>
  - Reference: reference impedance reduces the number of Touchstone ports through matrix reduction
  - Open: represents the physically disconnected port
  - EDA tools might still provide an interface to override the choices

Examples:

```
Unused_port_termination       Open

Unused_port_termination       Reference

Unused_port_termination       Resistance  43.5
```

Summary and Next Steps

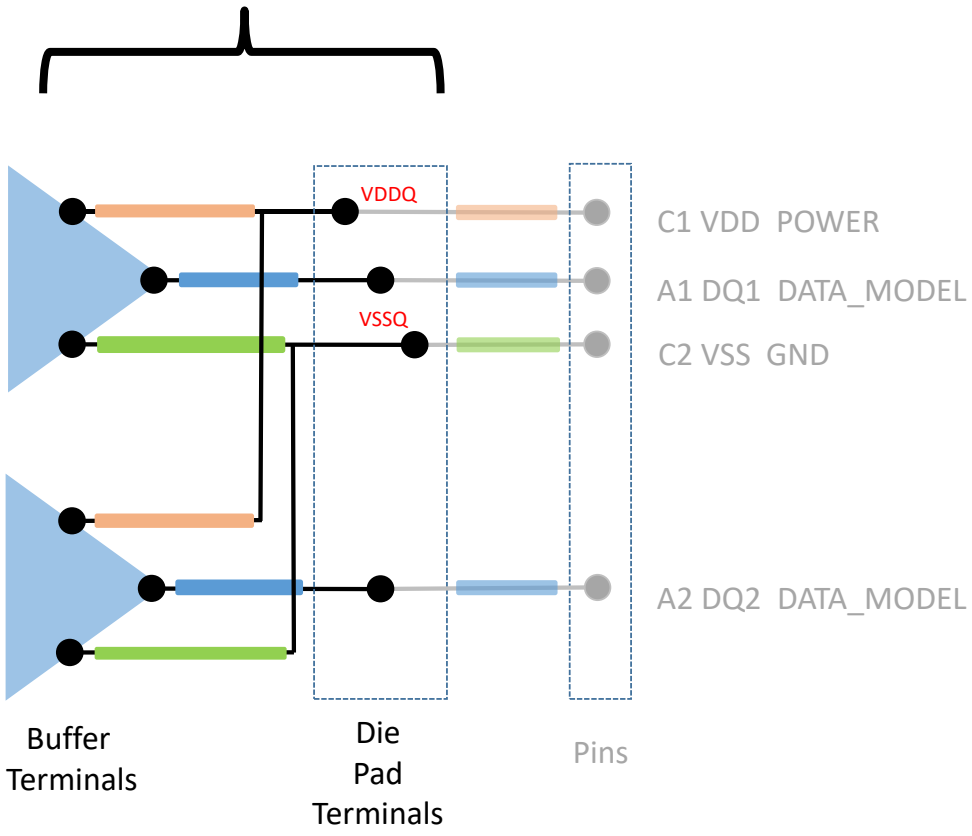
- BIRD189.5 is intended to improve IBIS package modeling
  - Flexibly supports crosstalk, loss, and existing modeling formats
- Formalizes and separates Die pads and Buffers
- Targeted for February 2018 completion by Interconnect Task Group and Open Forum submission

Comments are welcome! Help enable an advanced Interconnect format for IBIS Version 7.0!

BACKUP

[Interconnect Model] for Buffer-to-Die Pad Side

```
[Interconnect Model Set] Full_ISS_PDN
|
[Interconnect Model] Partial_ISS_buf_pad
|
File_IBIS-ISS        buf_pad.iss  buf_pad_2_typ
Number_of_terminals = 10
|
1  Pad_I/O        pin_name     A1 |  DQ1 (DQ signal)
2  Pad_I/O        pin_name     A2 |  DQ2 (DQ signal)
|
| POWER and GND terminals with pad_names and pin_names
3  Pullup_ref     pin_name     A1 |  VDD (POWER connection)
4  Pulldown_ref   pin_name     A1 |  VSS (GND connection)
5  Buffer_I/O     pin_name     A1 |  DQ1 (DQ signal)
6  Pullup_ref     pin_name     A2 |  VDD (POWER connection)
7  Pulldown_ref   pin_name     A2 |  VSS (GND connection)
8  Buffer_I/O     pin_name     A2 |  DQ2 (DQ signal)
|
| POWER and GND terminals with signal_names
9  Pad_Rail       pad_name   VDDQ |  VDD  POWER
10 Pad_Rail       pad_name   VSSQ |  VSS  GND
|
[End Interconnect Model]
```



[Die Supply Pads] for pad_names Shown in Example

The [Die Supply Pads] keyword establishes pad_name <Qualifier_entries> for rails, and associates them with signal_name (and optionally with bus_label entries)

```
[Die Supply Pads] signal_name bus_label
| pad_name
VDDQ                VDD
VSSQ                VSS
```

[Interconnect Model] for Buffer-to-Die Pad Side (Expanded)

```
[Interconnect Model Set] Full_ISS_PDN
|
[Interconnect Model] Partial_ISS_buf_pad
|
File_IBIS-ISS        buf_pad.iss  buf_pad_2_typ
Number_of_terminals = 10
|
1  Pad_I/O        pin_name     A1 |  DQ1 (DQ signal)
2  Pad_I/O        pin_name     A2 |  DQ2 (DQ signal)
|
| POWER and GND terminals with pad_names and pin_names
3  Pullup_ref     pin_name     A1 |  VDD (POWER connection)
4  Pulldown_ref   pin_name     A1 |  VSS (GND connection)
5  Buffer_I/O     pin_name     A1 |  DQ1 (DQ signal)
6  Pullup_ref     pin_name     A2 |  VDD (POWER connection)
7  Pulldown_ref   pin_name     A2 |  VSS (GND connection)
8  Buffer_I/O     pin_name     A2 |  DQ2 (DQ signal)
|
| POWER and GND terminals with signal_names
9  Pad_Rail       pad_name    VDDQ |  VDD  POWER
10 Pad_Rail       pad_name    VSSQ |  VSS  GND
|
[End Interconnect Model]
```

[Interconnect Model]

File and subcircuit

<Terminal lines> for connecting the subcircuit nodes (by position) to the interconnect structure

[Interconnect Model Set Group] for a Selected Group

```
[Interconnect Model Set Group]     A1_A2_PDN
|
| Interconnect Model Set Name      File_reference
Full_ISS_PDN                       NA
|
[End Interconnect Model Set Group]
```

[Interconnect Model Set Group] is at same level as [Package Model] for selected group of Buffer_IO pin(s)

Name should be descriptive for easy selection (e.g., A1-A2_PDN)

Can contain several references to [Interconnect Model Set]s

Sets can be in the .ibs file (NA) or in a separate directories

[Interconnect Model]s within a Group must be connected

Complete [Interconnect Model Set] With Both [Interconnect Model]s

[Interconnect Model Set]

[Interconnect Model]s

```
[Interconnect Model Set] Full_ISS_PDN
|
[Interconnect Model] Partial_ISS_buf_pad
|
File_IBIS-ISS        buf_pad.iss  buf_pad_2_typ
Number_of_terminals = 10
|
1  Pad_I/O        pin_name     A1 |  DQ1 (DQ signal)
2  Pad_I/O        pin_name     A2 |  DQ2 (DQ signal)
|
| POWER and GND terminals with pad_names and pin_names
3  Pullup_ref     pin_name     A1 |  VDD (POWER connection)
4  Pulldown_ref   pin_name     A1 |  VSS (GND connection)
5  Buffer_I/O     pin_name     A1 |  DQ1 (DQ signal)
6  Pullup_ref     pin_name     A2 |  VDD (POWER connection)
7  Pulldown_ref   pin_name     A2 |  VSS (GND connection)
8  Buffer_I/O     pin_name     A2 |  DQ2 (DQ signal)
|
| POWER and GND terminals with signal_names
9  Pad_Rail       pad_name   VDDQ |  VDD  POWER
10 Pad_Rail       pad_name   VSSQ |  VSS  GND
|
[End Interconnect Model]
```

```
[Interconnect Model] Partial_ISS_pad_pin_2
|
File_IBIS-ISS        pad_pin.iss  pad_pin_2_typ
Number_of_terminals = 8
|
1  Pin_I/O    pin_name      A1 | DQ1 (DQ signal)
2  Pin_I/O    pin_name      A2 | DQ2 (DQ signal)
|
| POWER and GND terminals with signal_names
3  Pin_Rail   signal_name  VDD | VDD (POWER connection)
4  Pin_Rail   signal_name  VSS | VSS (GND connection)
5  Pad_I/O    pin_name      A1 | DQ1  (DQ signal)
6  Pad_I/O    pin_name      A2 | DQ2  (DQ signal)
|
| POWER and GND terminals with pad_names
7  Pad_Rail   pad_name    VDDQ | VDD is signal name
8  Pad_Rail   pad_name    VSSQ | VSS is signal name
|
[End Interconnect Model]
|
[End Interconnect Model Set]
```

[End Interconnect Model Set]

<Terminal lines> Syntax

- All column entries on one line:

  <Terminal_number> <Terminal_type>
  <Terminal_type_qualifier> <Qualifier_entry>
  [Aggressor_Only]

- <Terminal_number> is IBIS-ISS node position or Touchstone port number

- Allowable <Terminal_type> names and associations next

Allowable <Terminal_type> Associations

<Terminal_number> <Terminal_type> <Terminal_type_qualifier> <Qualifier_entry> [Aggressor_Only]

Terminal_type	Terminal_type_qualifier				Aggressor_Only
	pin_name	signal_name	bus_label	pad_name	
Pin_I/O	X				A
Pad_I/O	X				A
Buffer_I/O	X				A
Pin_Rail	Y	Y	Y		
Pad_Rail		Y	Y	Z	
Buffer_Rail		Y	Y		
Pullup_ref	X				
Pulldown_ref	X				
Power_clamp_ref	X				
Gnd_clamp_ref	X				
Ext_ref	X				
A_gnd					

<Qualifier_entry>: ”X” I/O pin_name; “Y,” or “Z”: POWER or GND name. Optional “A”: “Aggressor_Only”

Why Update Interconnect Modeling?

- Improve package models with IBIS-ISS (an HSPICE subset) and Touchstone support
- Package modeling in IBIS stable since 2000
  - [Pin], [Package], [Package Model]
  - [Alternate Package Models] selector added
  - Limited support of loss, crosstalk and/or partitioning
- EBD (Electrical Board Description) for boards; No coupling and limited package model application
- IBIS, IBIS-ISS, Touchstone 2.0 and ICM are separate specifications
  - Limited interaction between them for package modeling
  - ICM (Interconnect Model) never adopted by industry