**DesignCon 2019 IBIS Summit**

February 1, 2019
Santa Clara, CA

**Agenda**

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| 8:00 AM | **REFRESHMENTS AND SIGN IN**  |
| 8:30 AM | **OFFICIAL OPENING** - Welcome to Summit - Introductions  |
| 8:45 AM | **IBIS Update** Mike LaBonte (SiSoft, USA)  |
| 9:00 AM | **JEITA EDA Model Specialty Committee Report** Miyo Kawata (ANSYS, Japan)  |
| 9:15 AM | **IBIS-ATM Task Group Report** Arpad Muranyi (Mentor, a Siemens Business, USA)  |
| 9:25 AM | **Introducing IBIS Version 7.0** Michael Mirmak (Intel Corporation, USA)  |
| 9:50 AM | **IBIS Version 7.0 Hierarchy Additions** Bob Ross (Teraspeed Labs, USA)  |
| 10:05 AM | **BREAK AND REFRESHMENTS**  |
| 10:25 AM | **IBIS V7 and IEEE 2401 Harmonization** Genichi Tanaka (Renesas, Japan)  |
| 10:50 AM | **COM & IBIS-AMI - How They Relate & Where They Diverge** Hsinho Wu, Masashi Shimanouchi, Mike Li (Intel Corporation, USA) [Presented by Hsinho Wu (Intel Corporation, USA)  |
| 11:30 AM | **Baseline Wander, Its Time-domain and Statistical Analysis** Vladimir Dmitriev-Zdorov (Mentor, a Siemens Business; USA)  |
| 12:00 PM | **FREE LUNCH** - Pre-registration required  |
| 1:00 PM | **Channel Simulation Using IBIS models with Asymmetric Rising and Falling Edges** Ken Willis, Kumar Keshavan, Ambrish Varma (Cadence Design Systems, USA) [Presented by Ken Willis (Cadence Design Systems, USA)]  |
| 1:20 PM | **Methods to Reduce Effects of DDR5 Rise/Fall Asymmetry in IBIS-AMI Simulations** Walter Katz (SiSoft, USA)  |
| 1:50 PM | **Study on Potential Feature Additions for Bit-by-bit Simulation Technique to Address DDR5 Requirements** Ted Mido (Synopsys, Japan)  |
| 2:20 PM | **Study of DDR Asymmetric Rt/Ft in Existing IBIS-AMI Flow** Wei-hsing Huang# and Wei-kai Shih## (SPISim, #USA, ##Japan) [Presented by Wei-hsing Huang (SPISim, USA)  |
| 2:50 PM | **BREAK AND REFRESHMENTS**  |
| 3:10 PM | **Modeling Forwarded Clock Interfaces with IBIS-AMI** Justin Butterfield (Micron Technology, USA)  |
| 3:30 PM | **Rx Clock Forwarding Investigation** Stephen Slater (Keysight Technologies, USA)  |
| 3:50 PM | **Impact of True Strobe Timing on DDR Channel** Simulation with IBIS-AMI Models Ken Willis, Kumar Keshavan, Ambrish Varma (Cadence Design Systems, USA) [Presented by Ambrish Varma (Cadence Design Systems, USA)]  |
| 4:10 PM | **On Die De-cap Modeling Proposal** Kazuki Murata\*, Megumi Ono\*\* (Ricoh\*, Socionext\*\*, Japan) [Presented by Megumi Ono (Scionext, Japan)]  |
| 4:40 PM | **IBIS Based Modeling for System-Level Power Delivery** Zhiping Yang\*, Songping Wu\*, Kinger Cai\*\*, Joshua Luo\*\*\*, Yingxin Sun\*\*\* (Google\*, Intel Corporation\*\*, Cadence Design Systems\*\*\*; USA) [Presented by Zhiping Yang (Google, USA)]  |
| 4:55 PM | **OPEN DISCUSSION AND CONCLUDING ITEMS** - Next Open Forum Meeting: February 22, 2019  |
| 5:00 PM | **END OF MEETING ROOM AVAILABILITY**  |

