IBIS Update

Mike LaBonte

SiSoft

Chair, IBIS Open Forum

2019 DesignCon IBIS Summit

Santa Clara, CA

February 1, 2019

http://www.ibis.org/

26 IBIS Members

Our Members

ANSYS · APPLIED SIMULATION TECHNOLOGY · BROADCOM · cadence · CISCO

CST · Ericsson · GLOBALFOUNDRIES · HUAWEI · IBM

infineon · intel · IOMeth · KEYSIGHT TECHNOLOGIES · MAXIM INNOVATION DELIVERED

Mentor A Siemens Business · NXP · Micron · Raytheon · SiSoft

SPISIM · synopsys · Teraspeed Labs · XILINX · ZTE

ZUKEN

Number of Members by Year

| Year	Members
1995	20
1996	23
1997	22
1998	27
1999	33
2000	35
2001	34
2002	31
2003	28
2004	23
2005	32
2006	34
2007	32
2008	32
2009	30
2010	31
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2012	29
2013	22
2014	22
2015	24
2016	22
2017	26
2018	26
2019	26
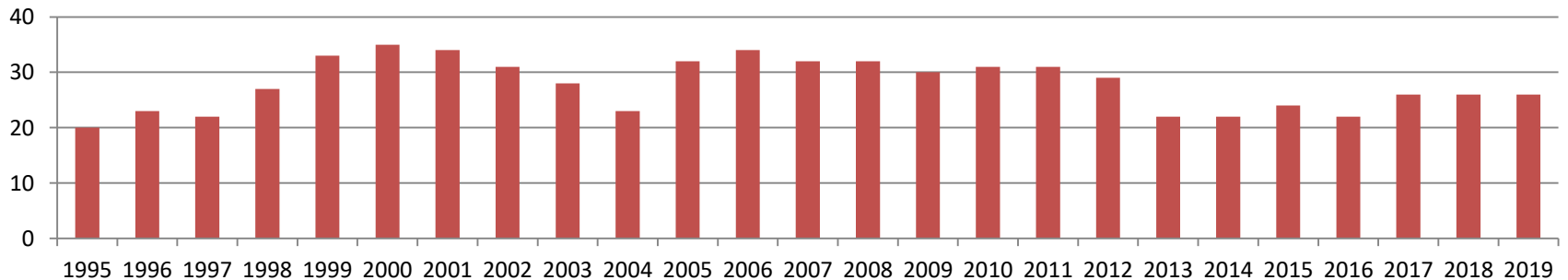
IBIS Officers 2018-2019

Chair: *Mike LaBonte, SiSoft*

Vice-Chair: *Lance Wang, IO Methodology Inc.*

Secretary: *Randy Wolff, Micron Technology*

Treasurer: *Bob Ross, Teraspeed Labs*

Librarian: *Anders Ekholm, Ericsson*

Postmaster: *Curtis Clark, ANSYS*

Webmaster: *Mike LaBonte, SiSoft*
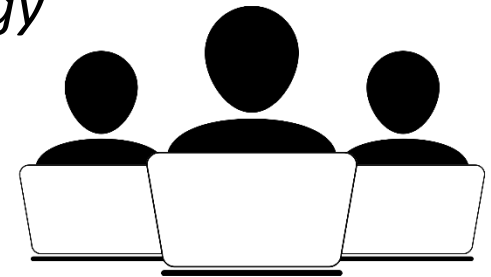
IBIS Meetings
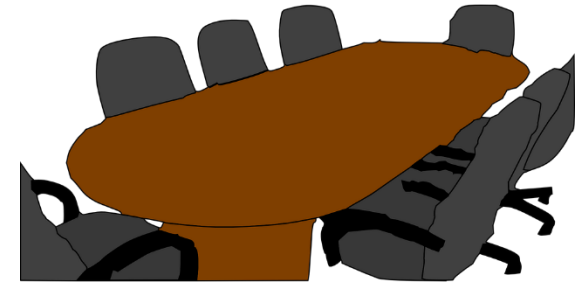
- Weekly teleconferences
  - Quality Task Group (Tuesdays)
  - Advanced Technology Modeling Task Group (Tuesdays)
  - Interconnect Task Group (Wednesdays)
  - Editorial Task Group (some Fridays)
- IBIS Open Forum teleconference every 3 weeks
  - 488 meetings so far
- IBIS Summit meetings: DesignCon, IEEE SPI, EDICON USA, EPEPS, Shanghai, Taipei, Tokyo

IBIS Summit Meetings

Taipei

Europe

Tokyo

Santa Clara

Shanghai

SAE ITC

- SAE Industry Technologies Consortia is the parent organization of the IBIS Open Forum

- IBIS is assisted by SAE employees José Godoy, Phyllis Gross, Dorothy Lloyd

- SAE ITC provides financial, legal, and other services

- http://www.sae-itc.org/

Task Groups

- Interconnect Task Group
    - Chair: Michael Mirmak
    - http://ibis.org/interconn_wip/
    - Develop on-die/package/module/connector interconnect modeling BIRDs

- Advanced Technology Modeling Task Group
    - Chair: Arpad Muranyi
    - http://ibis.org/atm_wip/
    - Develop most other technical BIRDs

- Quality Task Group
    - Chair: Mike LaBonte
    - http://ibis.org/quality_wip/
    - Oversee IBISCHK parser testing and development

- Editorial Task Group
    - Chair: Michael Mirmak
    - http://ibis.org/editorial_wip/
    - Produce IBIS Specification documents

BIRD = Buffer Issue Resolution Document

IBIS Milestones

I/O Buffer Information Specification

- 1993-1994 **IBIS 1.0-2.1**:
  - Behavioral buffer model (fast simulation)
  - Component pin map (easy EDA import)
- 1997-1999 **IBIS 3.0-3.2**:
  - Package models
  - Electrical Board Description (EBD)
  - Dynamic buffers
- 2002-2006 **IBIS 4.0-4.2**:
  - Receiver models
  - AMS languages
- 2007-2012 **IBIS 5.0-5.1**:
  - IBIS-AMI SerDes models
  - Power aware
- 2013-2015 **IBIS 6.0-6.1**:
  - PAM4 multi-level signaling
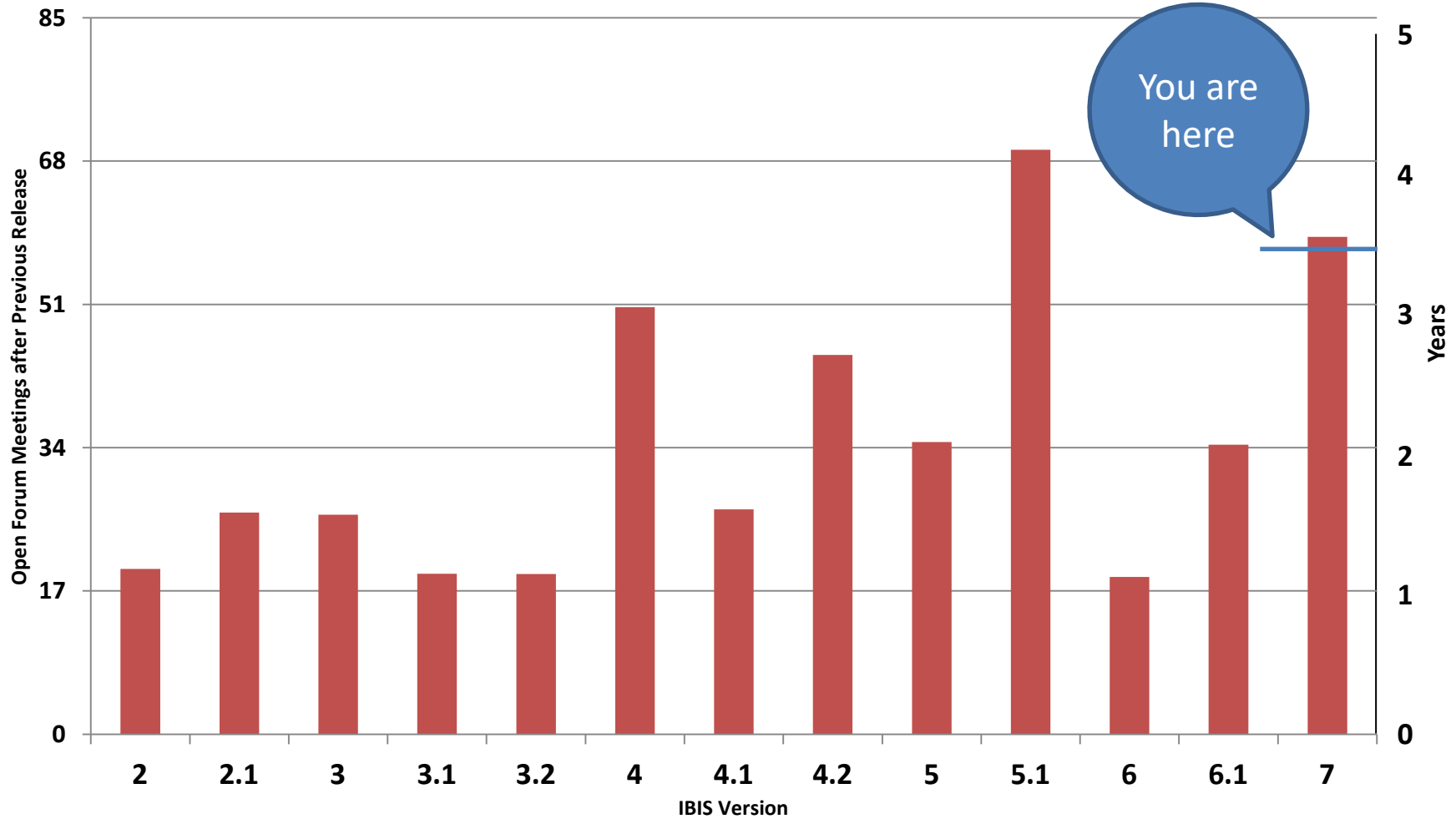 - Power delivery package models
- **2019? IBIS 7.0**

Current development

Other Work

- 1995: **ANSI/EIA-656**
  - IBIS 2.1
- 1999: **ANSI/EIA-656-A**
  - IBIS 3.2
- 2001: **IEC 62014-1**
  - IBIS 3.2
- 2003: **ICM 1.0**
  - Interconnect Model Specification
- 2006: **ANSI/EIA-656-B**
  - IBIS 4.2
- 2009: **Touchstone 2.0**[*]
- 2011: **IBIS-ISS 1.0**
  - Interconnect SPICE Subcircuit specification

IBIS Version Development

As of 15-Mar-2019

Beyond IBIS 7.0

- Currently 4 BIRDs in discussion
  - 2 about redriver flow
  - 1 editorial
  - 1 to support single-ended IBIS-AMI
- IBIS-ISS module syntax soon
- What else should IBIS tackle?
- Time to put on our thinking caps

IBIS Models Are Widely Available

- The IBIS Models page lists 80 suppliers

IBIS Model Suppliers - Click first letter of company name to jump

A B C D E F G H I J K L M N O P Q R S T U V W X Y Z

A   Go to top

get link

Actel

IBIS Models

Models for Actel's product families: IGLOO, IGLOO PLUS, Axcellerator, ProASIC3, ProAsic3L, Fusion, SX-A/eX, MX, ProASIC plus, etc. Like other programmable part families, these models come with device models and general package parasitic's only. The actual packaged models must be created by the user.

Showing **1029** results.

IBIS ✕   **Clear all**

162-Ball 4GB/8GB e•MMC v4.51 MLC and 8Gb

🔒 **IBIS** - 11.23.2012

162-Ball 4GB/8GB MLC e•MMC v4.51 (PS8210) and 8Gb LPDDR2 MT29PZZZ8D4WKFMW-18 W ES.6D4

Download

Think of IBIS as a distribution channel

What Else Could the IBIS "Distribution Channel" Be Used For?

- IBIS is nominally about I/O buffers, used to:
  - Solve signal quality problems like loss, inter-symbol interference (ISI) and crosstalk
  - Generate waveforms used in timing analysis
- But engineers also:
  - Insure proper timing between pins
  - Insure sufficient power distribution
  - Include optical links in analyses
  - Analyze channel operating margin (COM), forward error correction (FEC), etc.
  - Comply with any other new requirements posed by JEDEC, etc.

- What other data might IBIS formats convey?

The Most Common Engineering Data Format

- There is still much data found in PDF files, needed to complete the work of high speed digital design.

- Can IBIS formalize the presentation of some of that data to support EDA?

New Directions for IBIS?

- IBIS VRM models
- IBIS chip power models
- IBIS timing models
- IBIS waveform analysis language
- Data probability distributions
  (or at least more than 3 corners)
- IBIS-ISS [Test Load], external [Test Data]
- Optical Model_type(s) for
  Vertical Cavity Surface Emitting Laser (VCSEL), etc.
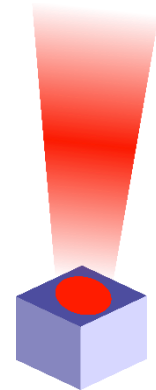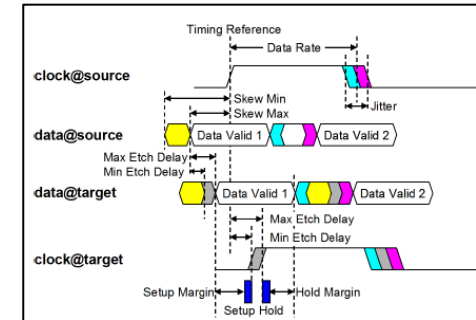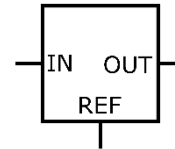
Before We Start Adding New Features

- Can we make IBIS support new types of model data without waiting for the next IBIS version?

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Future-Proofing IBIS

- More executable APIs?

- Programming languages for post-processing?

- Other uses for IBIS-ISS?

- Syntax to bundle other model file formats that make reference to the same pins, etc.

- Example:

```
[Associated Data] Pin_ref
MFMT_LPB_example.xml
[End Associated Data]
```

[Thank You]

IBIS Open Forum:
Web: http://www.ibis.org
Email: info@ibis.org

We welcome participation by all IBIS model makers, EDA tool vendors, IBIS model users, and interested parties.