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# On Die De-cap Modeling Proposal

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JEITA

Semiconductor & System Design Technical Committee

LPB Interoperable Design Sub-Committee

Modeling Working Group

# Contents

- Background
- Proposal for On die De-cap model
- Measurement of On die De-cap
- Conclusion

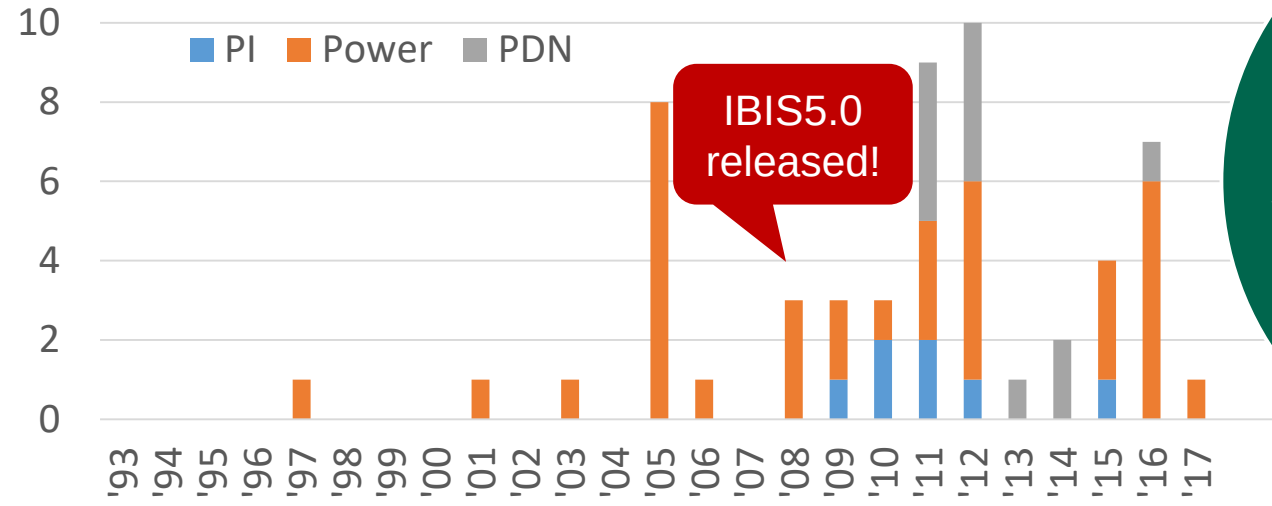
# Contents

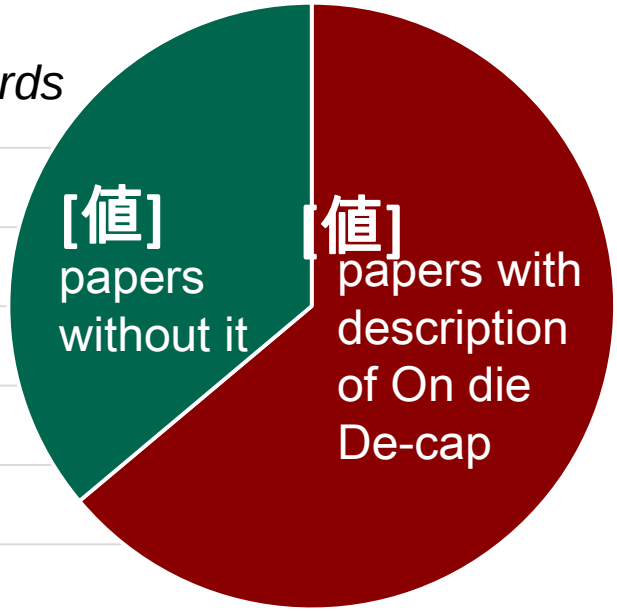
# Chip PDN characteristic

- Chip PDN characteristic
  - On die Resistance affects IR-Drop and Q factor
  - On die De-cap affects High frequency power-supply noise

Many papers reported in IBIS Summit describe importance of On die De-cap, because it is one of the few solution that reduce high frequency power-supply noise

*IBIS Summit papers, the title of which have the below words*



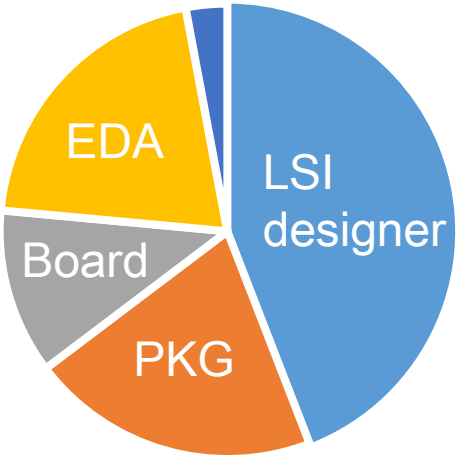



# A Survey of On die De-cap model

- However, board and system designers can hardly obtain On die De-cap model

*A Survey by JEITA LPB-SC MDL-WG @LPB developers workshop 2017.9.2*

*Respondents*

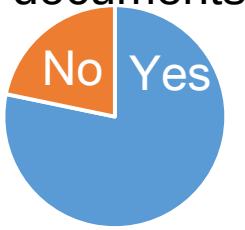



*Q1. to All*

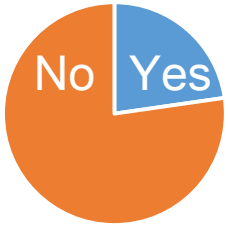
*"Can you obtain information about Chip PDN?"*

*Answer*

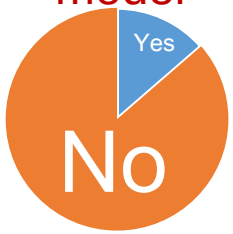
Guideline documents



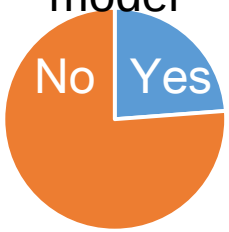

Target Z




On die De-cap model




PKG PDN model




*Q2. to LSI designer*

*"What are you concerned about when you offer PDN model"*

Answer

*"Which model format is suitable for our customer?"*

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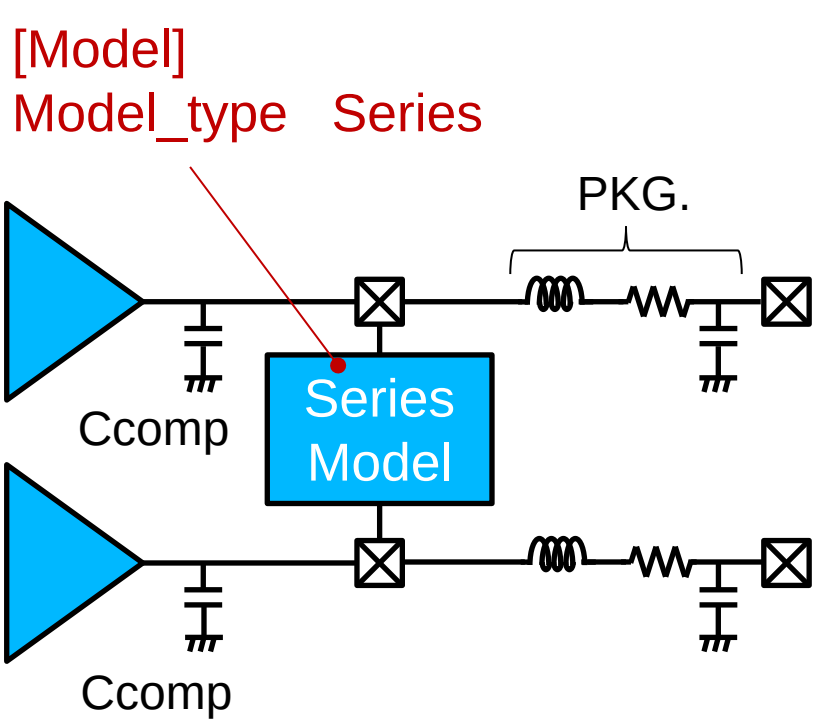
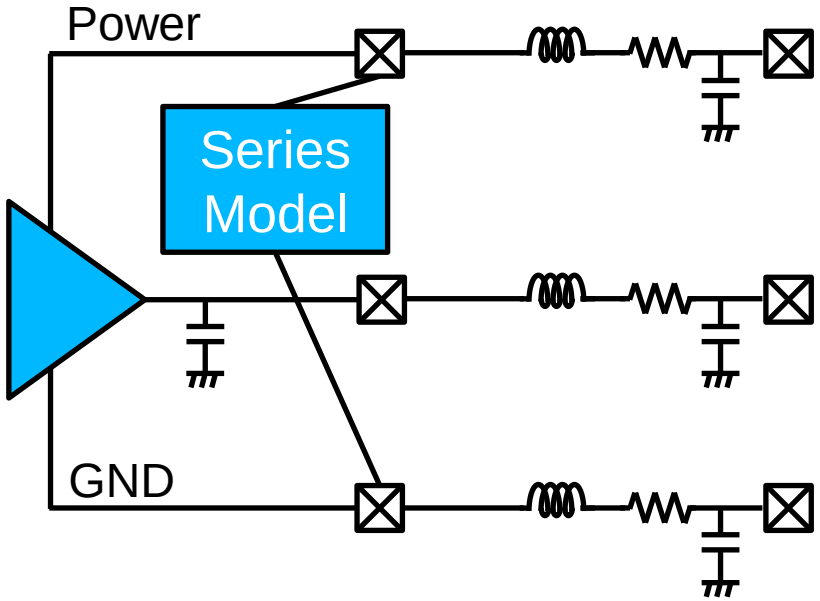
# On die De-cap model in IBIS

- It's time to add new IBIS keywords about On die De-cap!




*'Modeling the On-die De-cap of IBIS5.0 PDN-aware Buffers'*
*Lance Wang, and Randy Wolff Nov 2011*




(Another method: Support for De-caps using IBIS Version 7.0 will also be investigated.)

# On die De-cap model format proposal

## Present Series Model

```
[Pin]
A1  VCC  POWER
B2  SigA  BufferA
C3  VSS  GND
|
[Pin Mapping]
A1  NC       VBUS1
A2  NC       VBUS1
B2  GBUS1  VBUS1
C3  GBUS1  NC
C4  NC       VBUS2
|
[Series Pin Mapping]
C3  A1  OnChipDecap
|
[Model]  OnChipDecap
Model_type  Series
[C series]   3n  2.9n  3.1n
…
```

The word "Series" doesn't make me imagine PDN model

## Proposal

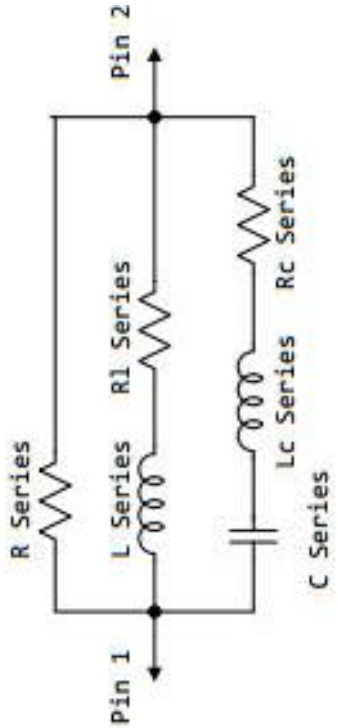
```
[Pin]
A1  VCC  POWER
B2  SigA  BufferA
C3  VSS  GND
|
[Pin Mapping]
A1  NC       VBUS1
A2  NC       VBUS1
B2  GBUS1  VBUS1
C3  GBUS1  NC
C4  NC       VBUS2
|
[PDN Model Mapping]
C3  A1  OnChipDecap
|
[Model]  OnChipDecap
Model_type    PDN
[C pdn]   3n  2.9n  3.1n
…
```

Proposal
Only for PDN model
Function is the same

# Topology of On die De-cap model

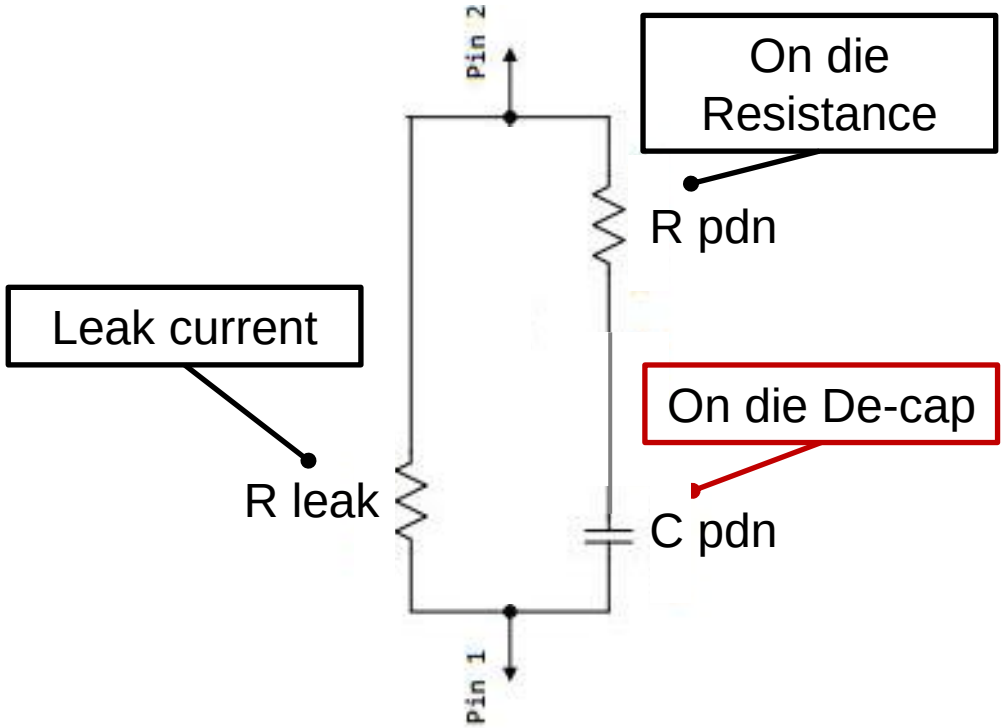
- Model_type Series

IBIS maker can choose which element to enable
There are 30 circuit topologies



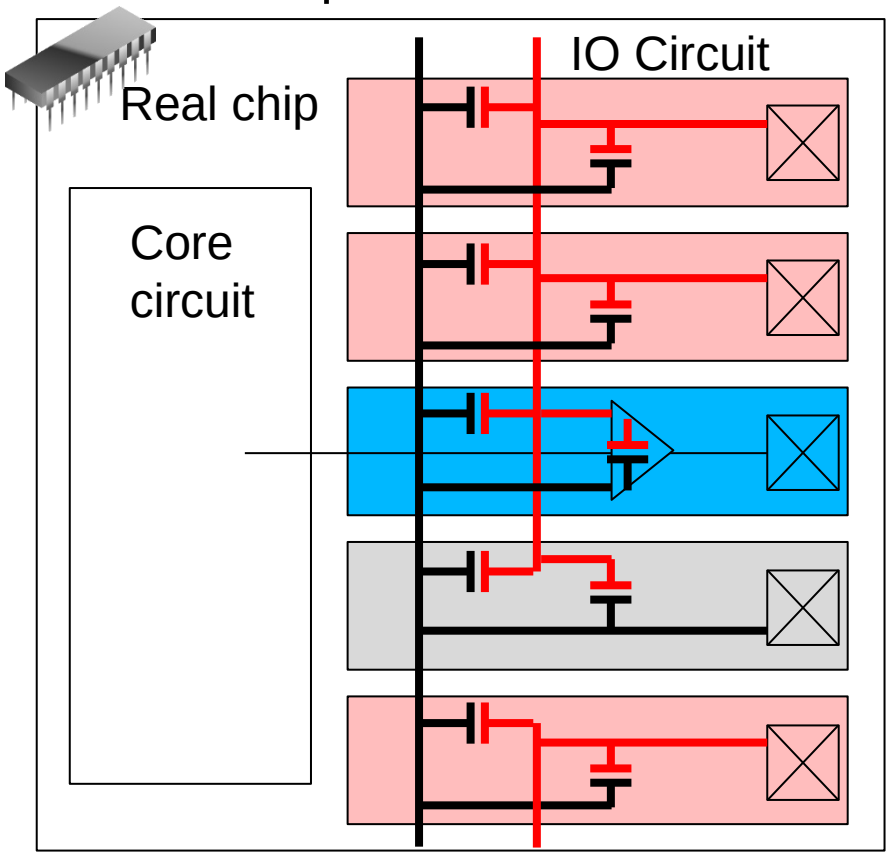

- Proposal: Model_type PDN

Only one topology available
On die De-cap, Resistance and Leak current can be represented

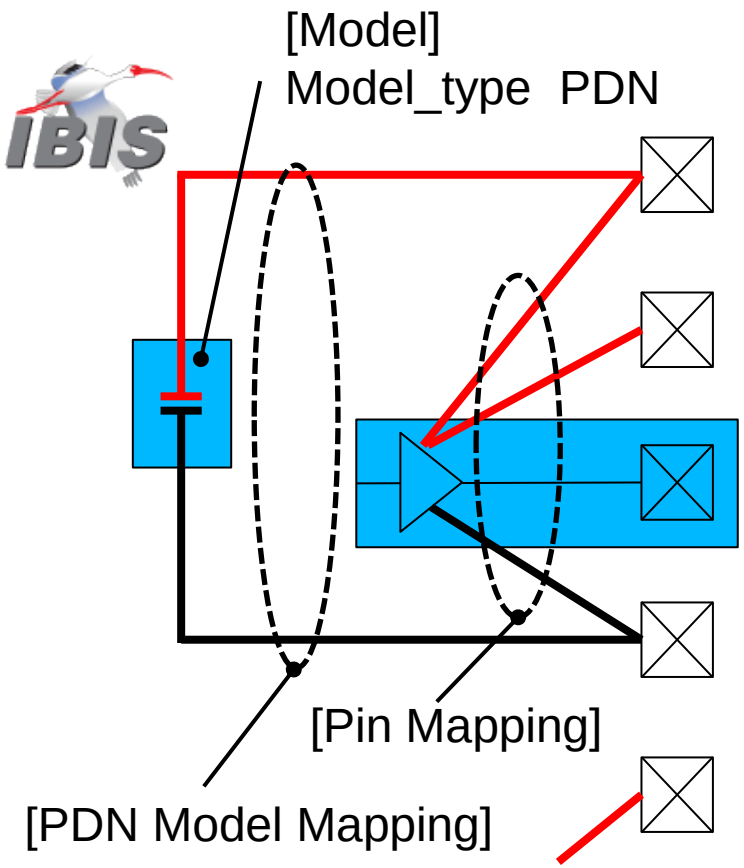


# On die De-cap model and real circuit

- There are De-cap cell, parasitic capacitance between VCC and GND metal, and MOS capacitance in IO circuit




- It is better to be represented by only one capacitor for the purpose of simplicity



# Modeling On die De-cap

- I hope that chip vendor can easily provide On die De-cap model by this proposal
- However, even if this proposal is adopted, it takes some time to spread this model

"I want to know this chip's PDN model right now!"
-> Try measuring

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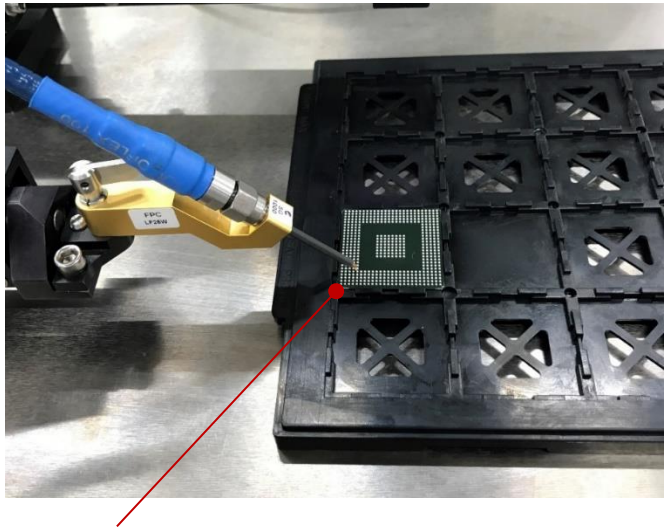
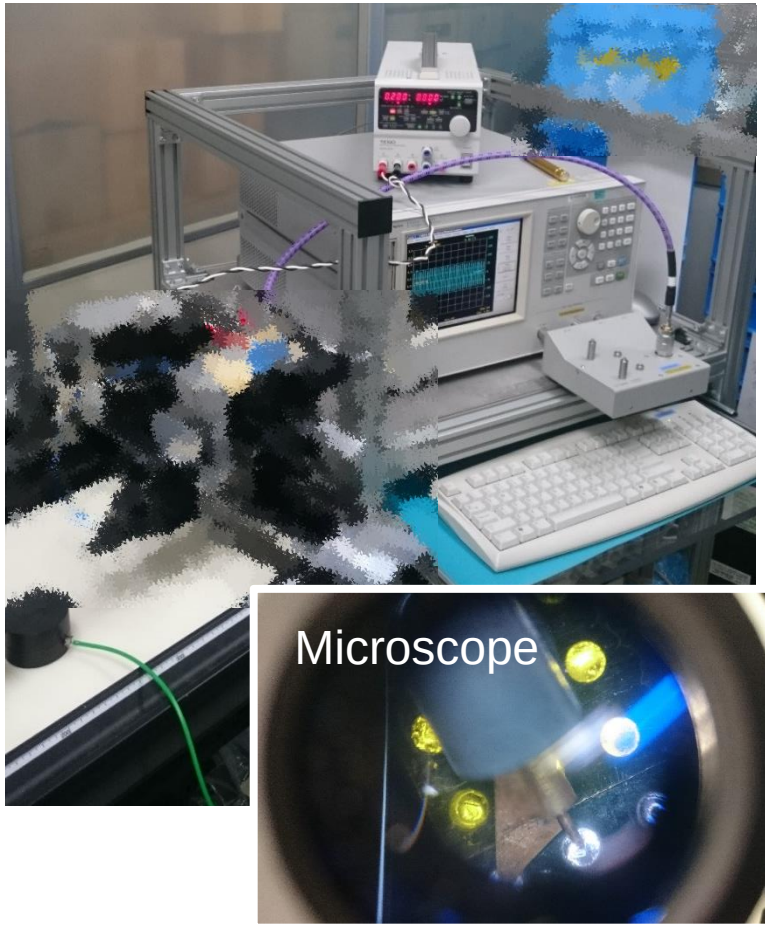
# Measuring On die De-cap

- Method

We measured impedance between VCC pin and GND pin by Impedance analyzer (or Network analyzer)
Supply voltage was applied these pins also

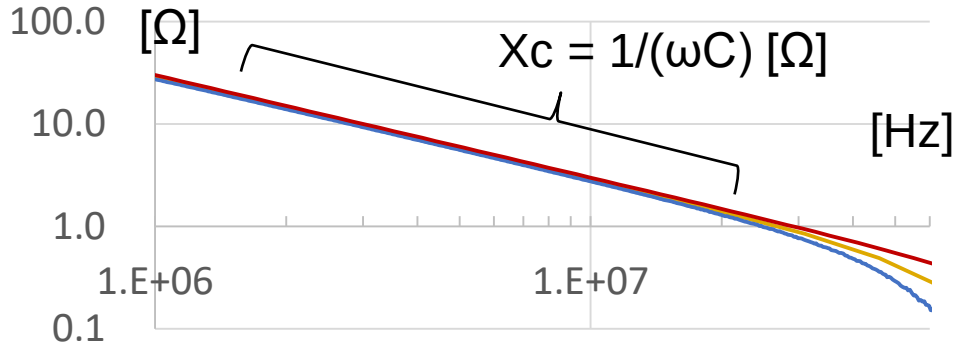


JEITA member company's chip



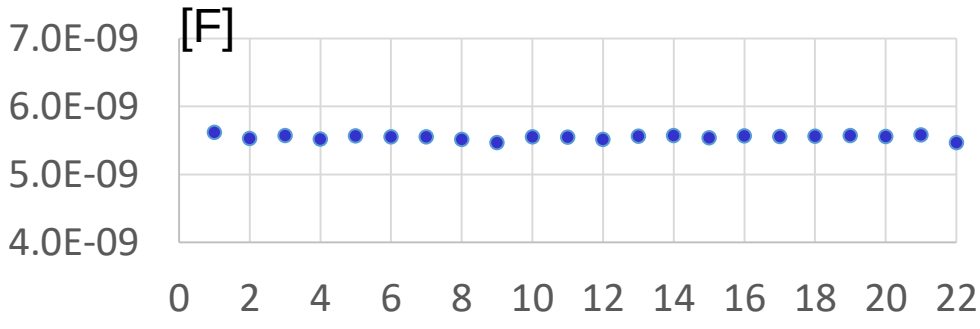
# Measurement Result

- Measured capacitance values are almost the same as the design value
- Even if each company measures the same chip in different measurement environments, the capacitance values are almost the same




| | |
|---|---|
| design value | 5.294nF |
| At company A | 5.691nF |
| At company B | 5.617nF |

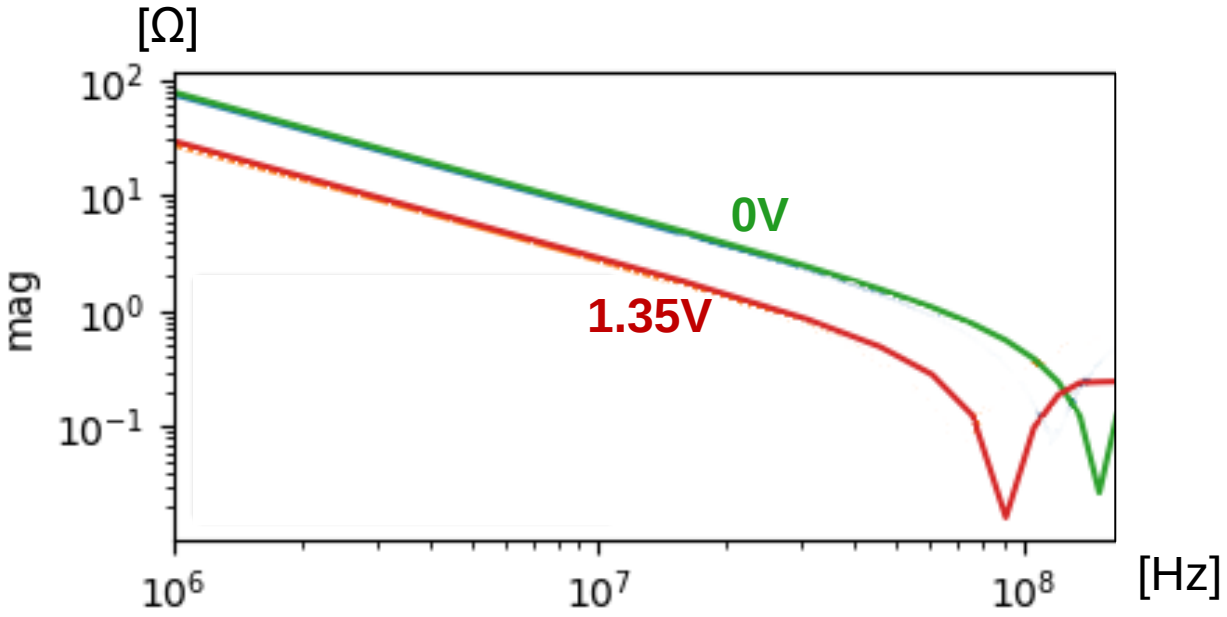
- There are few individual differences




Min=5.466nF
Max=5.617nF
σ=34pF

# Voltage dependence

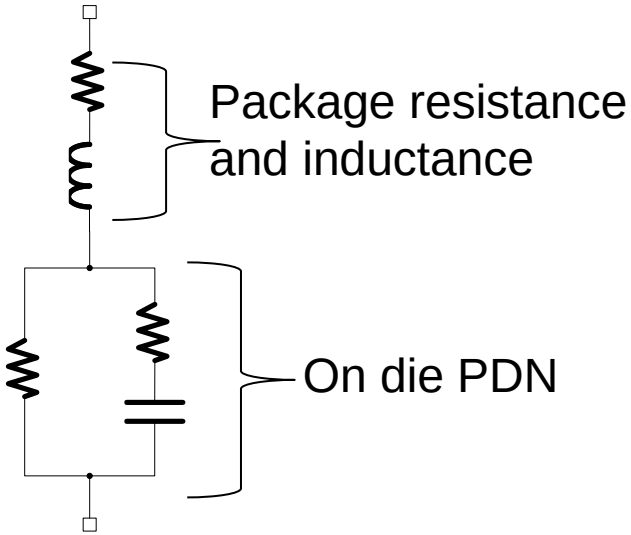
- Due to the voltage dependence, it is necessary to measure with the appropriate voltage applied

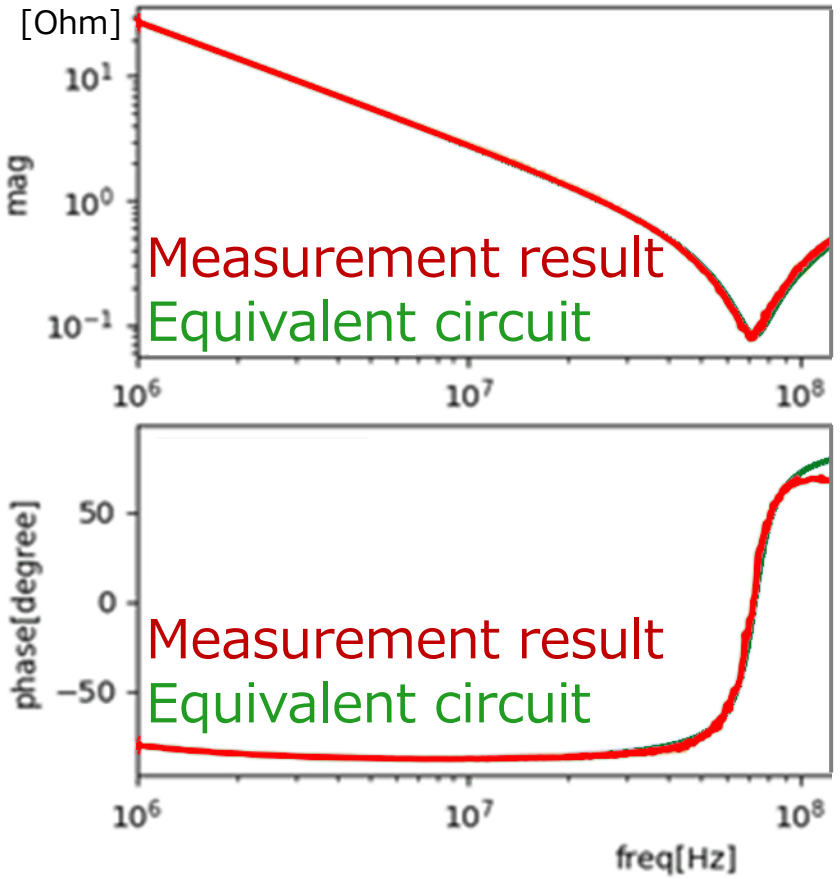


# Equivalent circuit

- Measuring result can be represented in the following equivalent circuit

Equivalent circuit

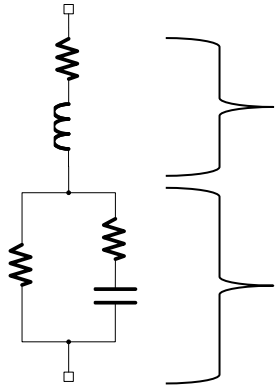


# Convert to IBIS

- This equivalent circuit can be represented in proposed PDN model

## Present Series Model

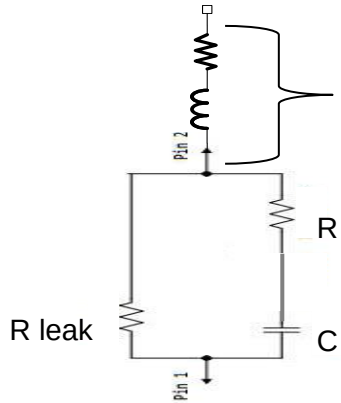


Package resistance and inductance

On die PDN = Series Model

```
[Model]      OnChipDecap
Model_type   Series
C_comp              0 0 0
|
|Variable            typ      min      max
[Voltage range]      1.35     1.283    1.425
|
[Temperature Range]  25       125      -40
[C series]           0.1n     0.09n    1.1n
[Rc series]          0.1      0.1      0.1
[R series]           200      200      200
```

## Proposed PDN model




Package resistance and inductance

On die PDN = Proposed PDN model

```
[Model]      OnChipDecap
Model_type   PDN
C_comp              0 0 0
|
|Variable            typ      min      max
[Voltage range]      1.35     1.283    1.425
|
[Temperature Range]  25       125      -40
[C pdn]              0.1n     0.09n    1.1n
[R pdn]              0.1      0.1      0.1
[R leak]             200      200      200
```

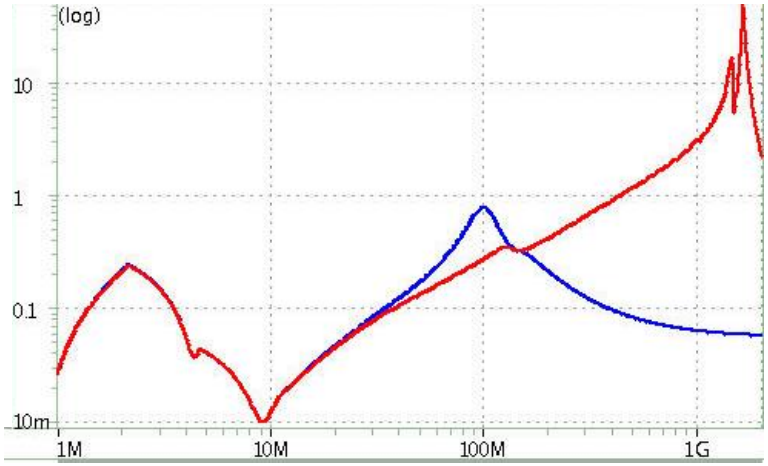
# Trial simulation

- Simulation using the IBIS model shown in the previous page

AC analysis result
= PDN input impedance

IBIS w/ PDN model
IBIS w/o PDN model

[Ω]

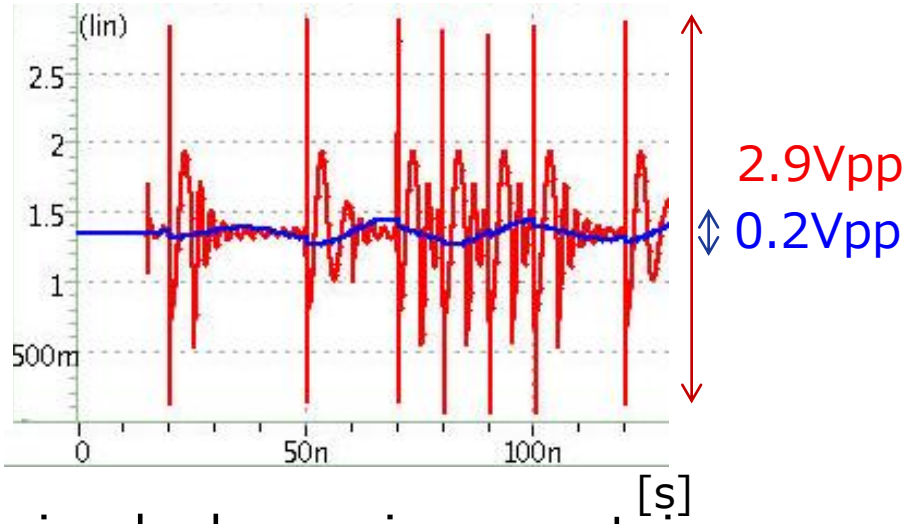



[Hz]

Transient analysis result
= IO switching VDD noise @DIE

IBIS w/ PDN model
IBIS w/o PDN model

[V]




[s]

- The expected result was obtained when using a certain simulator

**➔Please support our proposal in IBIS Model**

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# Conclusion

Chip PDN model is still not widespread. Therefore, we proposed to add an explicit keyword of chip PDN to IBIS.

And we introduced On die De-cap measuring method. Equivalent circuit made from measurement result can be represented in the new keyword.

We will submit a BIRD by March 14th. Please consider our proposal. And then, we hope that EDA tools will support it.

Thank you!