On Die De-cap Modeling Proposal

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JEITA
Semiconductor & System Design Technical Committee
LPB Interoperable Design Sub-Committee
Modeling Working Group
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- Background
- Proposal for On die De-cap model
- Measurement of On die De-cap
- Conclusion
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Chip PDN characteristic

- Chip PDN characteristic
  - On die Resistance affects IR-Drop and Q factor
  - On die De-cap affects High frequency power-supply noise

Many papers reported in IBIS Summit describe importance of On die De-cap, because it is one of the few solution that reduce high frequency power-supply noise

*IBIS Summit papers, the title of which have the below words*

IBIS Summit papers with description of On die De-cap: [36 papers]
IBIS Summit papers without it: [36 papers]

IBIS5.0 released!
A Survey of On die De-cap model

- However, board and system designers can hardly obtain On die De-cap model

A Survey by JEITA LPB-SC MDL-WG @LPB developers workshop 2017.9.2

Q1. to All
“Can you obtain information about Chip PDN?”
Answer
Guideline documents
Target Z
On die De-cap model
PKG PDN model

Q2. to LSI designer
“What are you concerned about when you offer PDN model”
Answer
“Which model format is suitable for our customer?”
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On die De-cap model in IBIS

- It’s time to add new IBIS keywords about On die De-cap!

(Another method: Support for De-caps using IBIS Version 7.0 will also be investigated.)
On die De-cap model format proposal

Present Series Model

[Pin]
A1  VCC  POWER  
B2  SigA  BufferA
C3  VSS  GND

| [Pin Mapping]
A1  NC  VBUS1
A2  NC  VBUS1
B2  GBUS1  VBUS1
C3  GBUS1  NC
C4  NC  VBUS2

| [Series Pin Mapping]
C3  A1  OnChipDecap

| [Model] OnChipDecap
Model_type  Series
[C series]  3n  2.9n  3.1n
...

Proposal

[Pin]
A1  VCC  POWER
B2  SigA  BufferA
C3  VSS  GND

| [Pin Mapping]
A1  NC  VBUS1
A2  NC  VBUS1
B2  GBUS1  VBUS1
C3  GBUS1  NC
C4  NC  VBUS2

| [Model] OnChipDecap
Model_type  PDN
[C pdn]  3n  2.9n  3.1n
...

The word “Series” doesn’t make me imagine PDN model
Proposal Only for PDN model
Function is the same
Topology of On die De-cap model

- Model_type Series

IBIS maker can choose which element to enable
There are 30 circuit topologies

- Proposal: Model_type PDN

Only one topology available
On die De-cap, Resistance and Leak current can be represented

![Diagram of On die De-cap model]
On die De-cap model and real circuit

- There are De-cap cell, parasitic capacitance between VCC and GND metal, and MOS capacitance in IO circuit.

- It is better to be represented by only one capacitor for the purpose of simplicity.

Real chip

Core circuit

IO Circuit

De-cap model

[Pin Mapping]

[Model]

Model_type PDN

[PDN Model Mapping]
Modeling On die De-cap

- I hope that chip vendor can easily provide On die De-cap model by this proposal

- However, even if this proposal is adopted, it takes some time to spread this model

“I want to know this chip’s PDN model right now!”
-> Try measuring
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Measuring On die De-cap

- **Method**
  We measured impedance between VCC pin and GND pin by Impedance analyzer (or Network analyzer)
  Supply voltage was applied these pins also

JEITA member company’s chip
Measurement Result

- Measured capacitance values are almost the same as the design value.
- Even if each company measures the same chip in different measurement environments, the capacitance values are almost the same.

![Graph showing Xc = 1/(ωC) [Ω] relationship between frequency [Hz] and resistance [Ω].]

- Design value: 5.294 nF
- At company A: 5.691 nF
- At company B: 5.617 nF

- There are few individual differences:
- Min = 5.466 nF
- Max = 5.617 nF
- σ = 34 pF

![Graph showing capacitance values over chip IDs.]
Voltage dependence

- Due to the voltage dependence, it is necessary to measure with the appropriate voltage applied.
Equivalent circuit

- Measuring result can be represented in the following equivalent circuit.
This equivalent circuit can be represented in proposed PDN model.

**Present Series Model**

- Package resistance and inductance
- On die PDN = Series Model

**Proposed PDN model**

- Package resistance and inductance
- On die PDN = Proposed PDN model

![Diagram of Proposed PDN model](image)

**Table Examples**

<table>
<thead>
<tr>
<th>Model</th>
<th>OnChipDecap</th>
</tr>
</thead>
<tbody>
<tr>
<td>Model_type</td>
<td>series</td>
</tr>
<tr>
<td>C_comp</td>
<td>0 0 0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Variable</th>
<th>typ</th>
<th>min</th>
<th>max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage range</td>
<td>1.35</td>
<td>1.283</td>
<td>1.425</td>
</tr>
</tbody>
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</tr>
</thead>
<tbody>
<tr>
<td>C series</td>
<td>0.1n</td>
<td>0.09n</td>
<td>1.1n</td>
</tr>
<tr>
<td>Rc_series</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td>R series</td>
<td>200</td>
<td>200</td>
<td>200</td>
</tr>
</tbody>
</table>
Simulation using the IBIS model shown in the previous page

- AC analysis result
  - = PDN input impedance
  - IBIS w/ PDN model
  - IBIS w/o PDN model

- Transient analysis result
  - = IO switching VDD noise @DIE
  - IBIS w/ PDN model
  - IBIS w/o PDN model

![Graph showing AC analysis results with and without PDN model](image1)

![Graph showing transient analysis results with and without PDN model](image2)

- The expected result was obtained when using a certain simulator

⇒ Please support our proposal in IBIS Model
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Conclusion
Conclusion

Chip PDN model is still not widespread. Therefore, we proposed to add an explicit keyword of chip PDN to IBIS.

And we introduced On die De-cap measuring method. Equivalent circuit made from measurement result can be represented in the new keyword.

We will submit a BIRD by March 14th. Please consider our proposal. And then, we hope that EDA tools will support it.

Thank you!