IBIS Version 7.0 Hierarchy Additions

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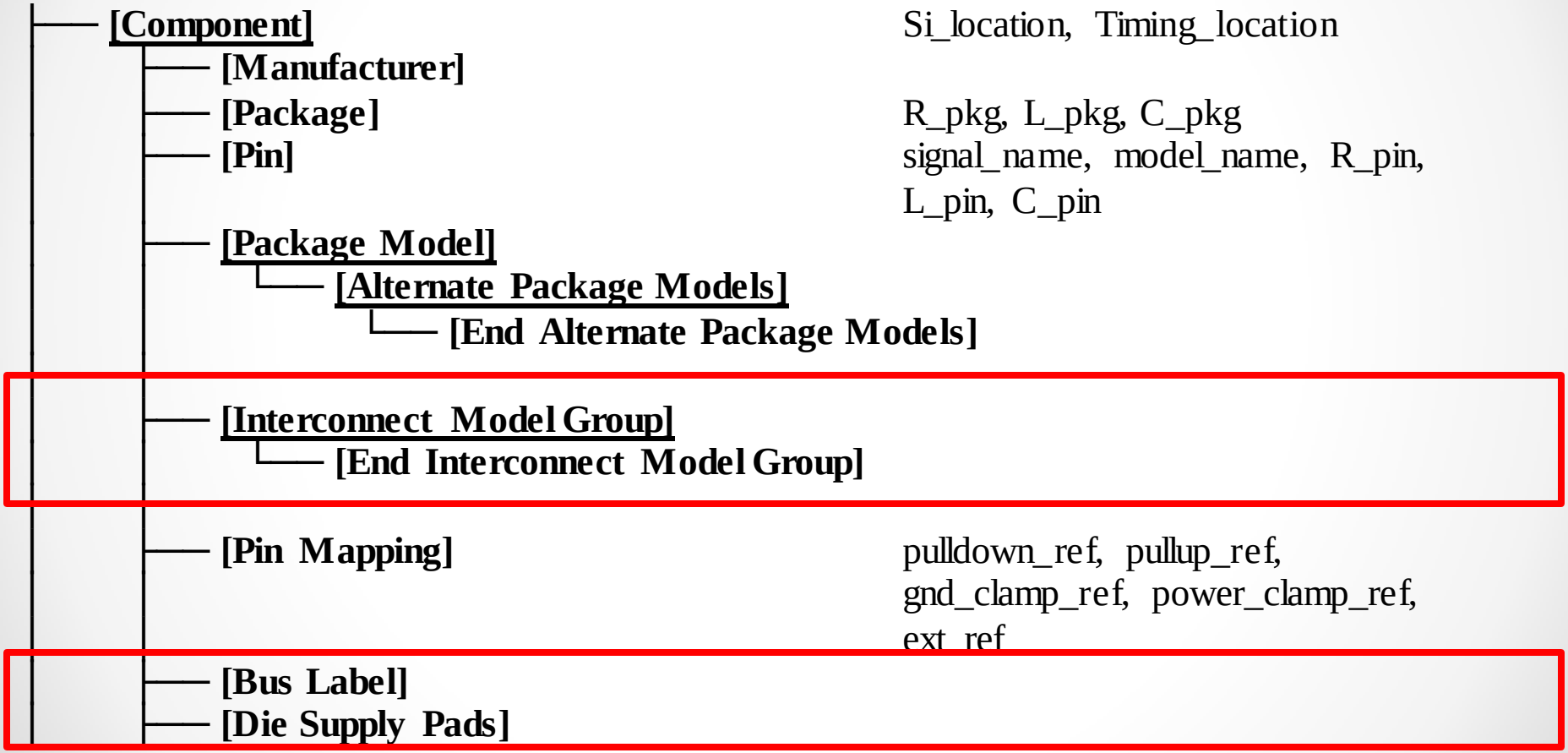
Overview – A Quick Reference

- Section 3.3 in IBIS Version 7.0 contains a hierarchy (tree) diagram for all file formats, keywords and subparameters
  - .ibs files
  - .pkg files
  - .ebd files
  - Not included - .ami files
  - New - .ims files
- Interconnect Modeling related additions is focus here
  - (Unofficial expanded hierarchy (tree) diagram and IBIS evolution table with more details uploaded under http://www.ibis.org/ver7.0_wip/)

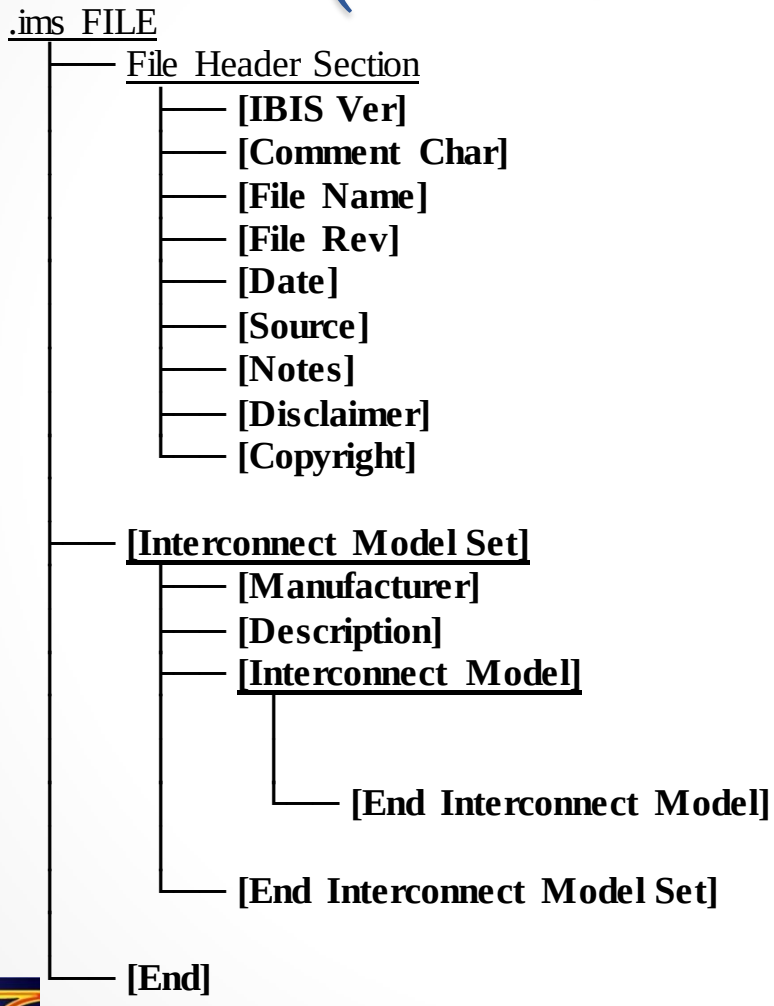
Existing Package Options Under [Component] (Section 3.3)

- **[Component]** — Si_location, Timing_location
  - **[Manufacturer]**
  - **[Package]** — R_pkg, L_pkg, C_pkg
  - **[Pin]** — signal_name, model_name, R_pin, L_pin, C_pin
  - **[Package Model]**
    - **[Alternate Package Models]**
      - **[End Alternate Package Models]**
  - **[Interconnect Model Group]**
    - **[End Interconnect Model Group]**
  - **[Pin Mapping]** — pulldown_ref, pullup_ref, gnd_clamp_ref, power_clamp_ref, ext_ref
  - **[Bus Label]**
  - **[Die Supply Pads]**

New Interconnect and Terminal Definitions

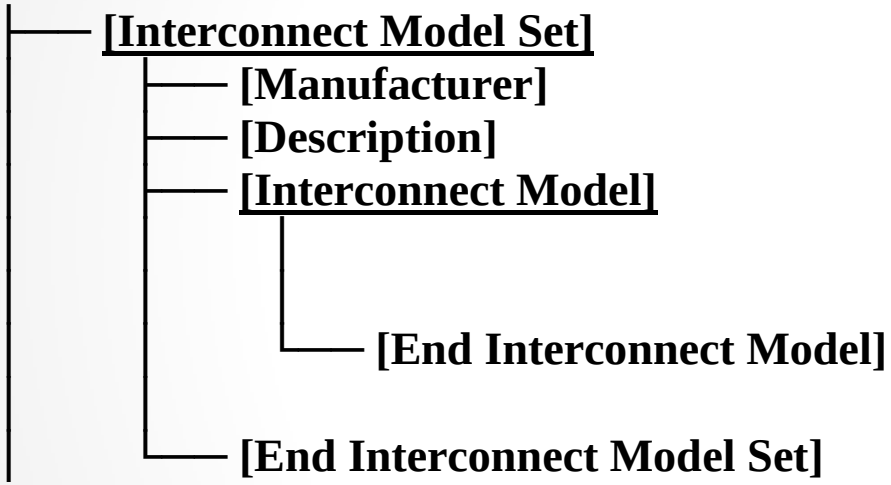


[Interconnect Model Set] (In New File)



Param, File_TS, File_IBIS-ISS, Unused_port_termination, Number_of_terminals

[Interconnect Model Set] (In .ibs File at Top-level)



Param, File_TS, File_IBIS-ISS, Unused_port_termination, Number_of_terminals

(Same level as [Component])

[Interconnect Model Group] Additions (Section 5)

- **[Interconnect Model Group] columns**
  - **<ims_name> links to an [Interconnect Model Set] <ims_name> keyword**
  - **<file_reference> gives the [Interconnect Model Set] location**
  - **E.g.,**
    - **<ims_name1> <file_reference1>**
    - **<ims_name2> <file_reference2>**
    - **…**
  - **<file_reference> column:**
    - **NA: in same .ibs file**
    - **<{directory_path}/ims_file_name>: in a .ims file**

[Interconnect Model Group] Section 5; Examples 2, 3

```
| Example 2
|
[Interconnect Model Group] Full_ISS_PDN_sn_2
| Interconnect Model Set    file_reference
Full_ISS_PDN_sn_2           NA                  | The [Interconnect Model Set] is
                                                | present in the .ibs file for
                                                | all I/O pins and PDN described
                                                | by signal_names (sn)
[End Interconnect Model Group]
|

| Example 3
|
[Interconnect Model Group] A1_TS
| Interconnect Model Set    file_reference
A1_TS                       touchstone/ts_sets.ims | [Interconnect Model Set] is
                                                   | in ts_sets.ims under the
                                                   | touchstone directory for A1
[End Interconnect Model Group]
|
```

[Interconnect Model Set] Section 11, Example 2

```
| Example 2: Same as Example 1 except the PDN networks are simplified with
|   signal_name qualifiers to create a pair of POWER terminals and a pair
|   of GND terminals

[Interconnect Model Set]          Full_ISS_PDN_sn_2
|-----
[Interconnect Model]              Full_ISS_buf_pin_2
File_IBIS-ISS   full_buf_pin.iss                full_buf_pin_2_typ
Number_of_terminals = 14

1  Pin_I/O      pin_name      A1    |  DQ1          DQ
2  Pin_I/O      pin_name      A2    |  DQ2          DQ
3  Pin_I/O      pin_name      A3    |  DQ3          DQ
4  Pin_I/O      pin_name      D1    |  DQS+         DQS
5  Pin_I/O      pin_name      D2    |  DQS-         DQS
|
| POWER and GND terminals with signal_names
|
6  Pin_Rail     signal_name   VDD   |  VDD          POWER
7  Pin_Rail     signal_name   VSS   |  VSS          GND
|
8  Buffer_I/O   pin_name      A1    |  DQ1          DQ
9  Buffer_I/O   pin_name      A2    |  DQ2          DQ
10 Buffer_I/O   pin_name      A3    |  DQ3          DQ
11 Buffer_I/O   pin_name      D1    |  DQS+         DQS
12 Buffer_I/O   pin_name      D2    |  DQS-         DQS
|
| POWER and GND terminals with signal_names
|
13 Buffer_Rail  signal_name   VDD   |  VDD          POWER
14 Buffer_Rail  signal_name   VSS   |  VSS          GND
|
[End Interconnect Model]
[End Interconnect Model Set]
```

[Interconnect Model Set] Section 11, Example 3

```
|*****************************************************************************
|
| Example 3: Single I/O Touchstone connection with one extra terminal for the
|   N+1 .s2p reference connection terminal

[Interconnect Model Set]      A1_TS
|-----
[Interconnect Model]          A1_TS_buf_pin
File_TS          dq_ts_buf_pin.s2p
Number_of_terminals = 3
1  Pin_I/O       pin_name      A1
2  Buffer_I/O    pin_name      A1
3  Pulldown_ref  pin_name      A1   | VSS reference for .s2p file
                                   | Rail connections to Buffer_I/O through
                                   | [Pin Mapping] or a [Model] reference
                                   | voltage used if no external rails
[End Interconnect Model]
[End Interconnect Model Set]

|*****************************************************************************
|
```

Terminal Name Entries Under [Component] keyword (Section 5)

- **POWER/GND rail terminal names**
  - **[Pin]: pin_name AND signal_name, (default) bus_label**
  - **[Pin Mapping]: pin_name AND bus_label**
  - **[Bus Label]: bus_label AND signal_name**
  - **[Die Supply Pads]: pad_name AND signal_name (and optional bus_label)**
- **I/O buffer terminal names**
  - **[Pin]: pin_name**
  - **[Pin Mapping]: pin_name**

- **See www.ibis.org/summits/oct17/ross.pdf for details**

Summary

- **Section 3.3 – Keyword Hierarchy for keyword context and scoping – a quick reference guide**
- **Section 5 - [Interconnect Model Group] keyword for linking to [Interconnect Model Set]s by <ims_name>**
- **Section 5 - Terminal name descriptions with [Pin], [Pin Mapping], [Bus Label], [Die Supply Pads] for [Interconnect Model] terminal lines**
- **Section 11 - Interconnect Modeling descriptions**
  - **.ims file**
  - **[Interconnect Model Set] <ims_name>**
  - **[Interconnect Model]**