Impact of True Strobe Timing on DDR Channel Simulation with IBIS-AMI Models

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Overview

• As channel simulation and IBIS-AMI modeling methods are adapted from serial link to DDR interface analysis, serial link CDR algorithms are often used for analysis
• But actual DDR interfaces use strobe signals as the timing reference for data buses
• What is the impact?
Agenda

• Current CDR-based method
• True strobe timing
• Comparison of results
• Summary
Current CDR-Based Method

• Centers the eye for each individual signal
  – With real strobe, this is done for entire byte lane
  – Some controllers have some individual bit de-skewing
Current Channel Simulation Flow

- Standard (Current) channel simulation flow for serial link channels that is also used for parallel bus

- Ideal clock ticks are generated internally by the eye sampler
- Clock ticks can also be generated by AMI models and sent to the eye sampler
True Strobe Timing (TST)

- Clock ticks are collected from the strobe channel instead of the data channel
- Strobe channel is only fed with 0101 data
- Clock ticks are collected in the same way as data channel
New Channel Simulation Flow for Source Synchronous Channel

EDA Platform

BIT PATTERN

Continuous waveform

Eye Sampler
(EDA Platform)

Eye Sampler
(EDA Platform)

CLOCK PATTERN

Continuous waveform

Strobe Clock ticks

Strobe Path

Data Path
Comparison of Results

• CDR vs. TST
• CDR vs. TST with jitter impairments

• Test Setup
  – 1 data line is used for simulations
  – 6 Gbps
  – Rx CTLE
  – Rx 4 tap DFE
CDR vs. TST
Strobe Results with Dj Applied at Tx
CDR Results with Dj Applied at Tx
CDR vs. TST

• After delaying by 0.2 UI
CDR vs. TST

• After delaying by 0.2 UI
Summary

- Using default CDR instead of actual strobe to get clock risks missing important impairments/jitter for parallel bus topology
- Analysis results show false optimism using CDR approach as compared to true strobe timing methodology
- Need to model delay accurately