IBIS Based Modeling for System-Level Power Delivery

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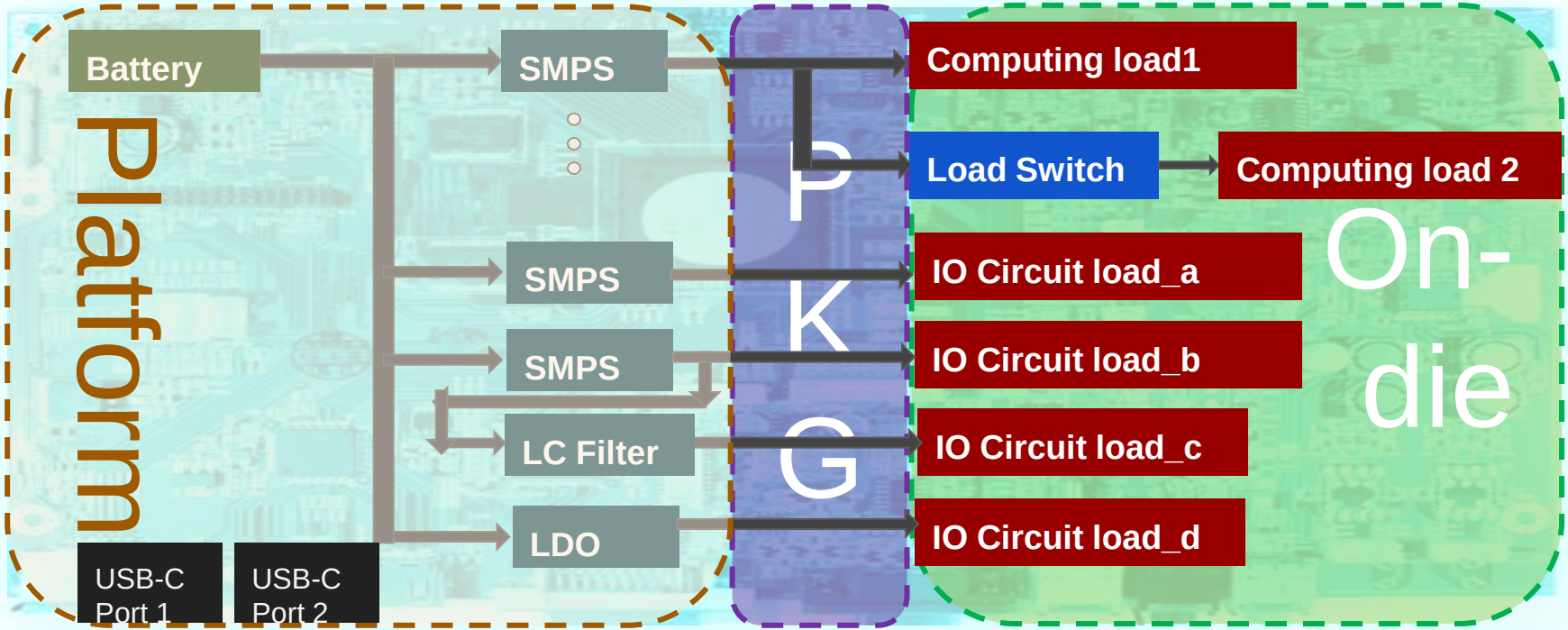
System Power Delivery Architect



*SMPS=switching mode power supply

Sys PD Architect:

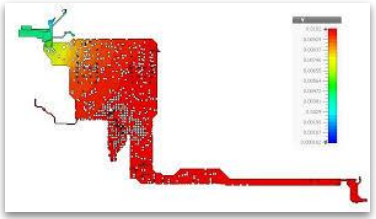
1, SMPS to computing load 2, SMPS to IO circuit load

3, LDO to IO circuit load 4, SMPS to IO circuit load_b, and also to IO circuit load_c through LC filter to IO

System-Level Power Simulation Coverage

Propose to use IBIS format models to do the following simulations:

- System level DC simulations, including IR drop, DCR.
- AC simulations, i.e. PDN impedance
- Transient load response, i.e. transient power noise
- System power consumption and efficiency
- Power/thermal co-simulation



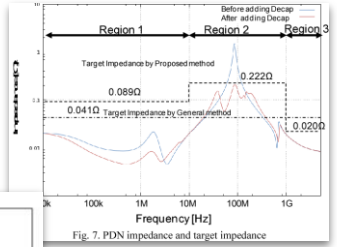
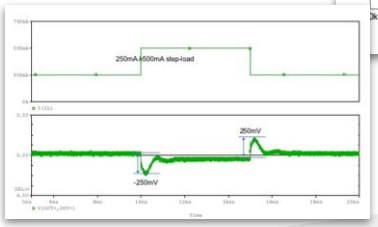
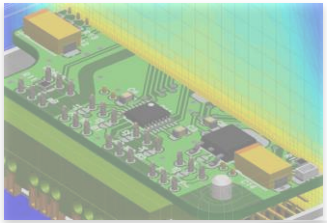
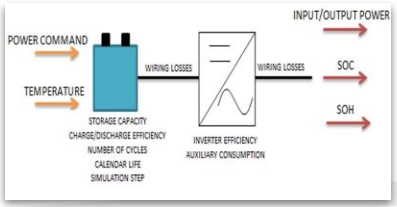


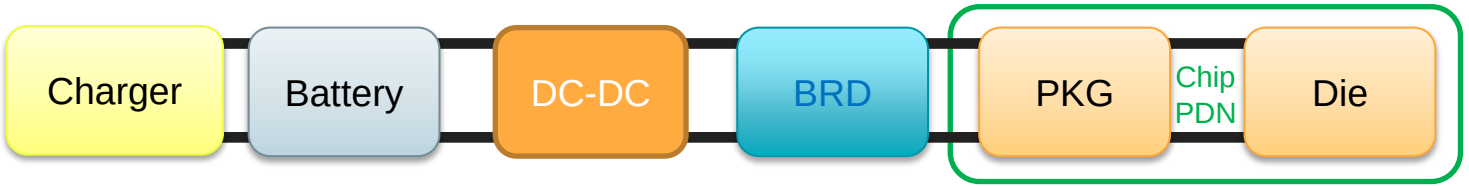
Fig. 7. PDN impedance and target impedance



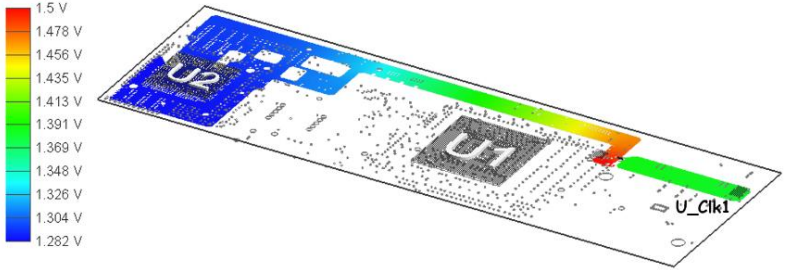




DC Simulation Common Methodology



- Charger & Battery not modeled. Model from DC-DC to Die IR drop.
- DC-DC model as current source
- BRD & all the passive components on board as a resistance network
- PKG resistance network
- Die as current sink/load



Shortcomings and Proposals

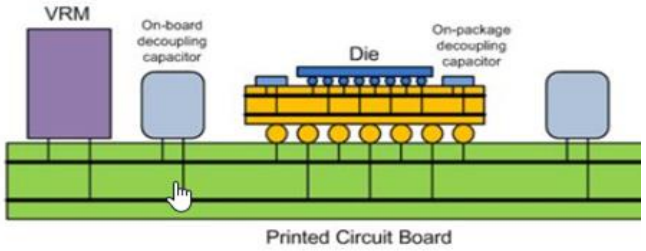
- Shortcomings:
  - Have to readout and key in current load and voltage source values for all the rails manually. Easy to make a fault.
  - No VRM loadline information included.
- Proposals:
  - Device chip vendor to provide IBIS format power model that includes current information.
  - VRM vendor to provide IBIS format model including voltage source information.

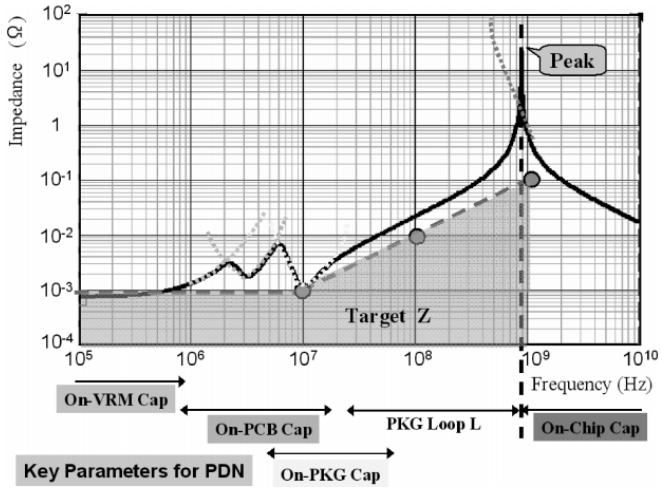
AC Simulation Common Methodology

Die Models:
- CPM model (passive)
- Simple Rdie, Cdie netlist
- PKG PDN (level –a)
  - S parameter from bump to pin/BGA
  - pin awareness, for automatically merging with BRD
  - Impedance target at Observation port in PKG
- On-die PDN (level –b)
  - S parameter of power grid
  - Impedance target at Observation port in PKG

BRD Models:
- Passive extraction using EM EDA tools

VRM Models:
- 1st order 2-element model
- 2nd order 4-element model





Shortcomings and Proposals

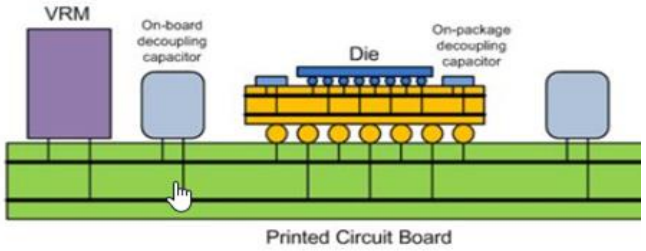
- Shortcomings:
  - Hard to get die model either in CPM or Rdie/Cdie from chip vendor
  - Hard to get package model from vendors
- Proposals:
  - Device chip vendor to provide IBIS format power model that can (optionally) provide die model as well as package model.

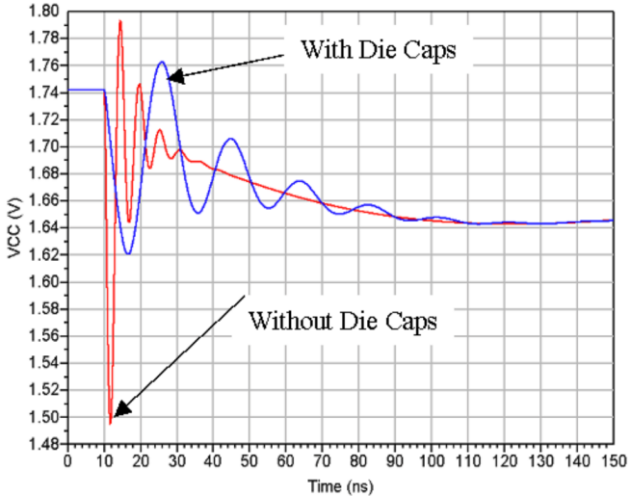
Transient Simulation Common Methodology

Die Models:
- CPM model (active)
- Worst case icct profile

BRD Models:
- PDN including power routings, caps extraction using EM EDA tools

VRM Models:
- Simplis model
- Behavioral HSPICE model
- Transistor level model





Similarly . . .

- We propose to include current consumption and CMOS circuits netlist in the IBIS format model to simulate power consumption of each device.
- We propose to include detailed chip model in IBIS format to model switching and conduction loss of a device so as to get power/thermal co-simulation.

Approved IBIS BIRDs related to Power - 1

BIRD #	Title	Status	Statement	Value for this proposal
28.3	Enhancement To The Package Model (.pak file) Specification	Accepted	“The current package model specification describes each pin on a package using lumped L/R/C parameters. Coupling between pins also assumes lumped electrical parameters. However, these description are inadequate when the electrical length of the package elements are greater than ~1/6 of the I/O buffers' rise time. This bird enhances the package description by allowing package elements to be described in terms of length and L, R and C per unit length; i.e. a transmission line representation.”	Can be used for package model format.
38	Maximum Voltage	Rejected	“IBIS can be extended to allow a component supplier specify maximum positive and negative voltages (or currents) that can safely be applied to an I/O buffer”.	Can be extended to all power device current profile format.

Approved IBIS BIRDs related to Power - 2

BIRD #	Title	Status	Statement	Value for this proposal
42.3	Modeling Current Waveforms	Rejected	“Current into the power and ground rails are needed to give a more accurate analysis for ground and power bounce analysis associated with simultaneous switching”.	A similar format can be used to give current profile.
95.6	Power Integrity Analysis using IBIS	Accepted	“Power Integrity Analysis which includes Current switching profile of the Core as well as Simultaneous Switching Noise (SSN) of states of a buffer is to be analyzed through IBIS.”	Can be extended to core power rails too.
125.1	Make IBIS-ISS Available for IBIS Package Modeling	Rejected	“Package modeling in IBIS has numerous serious limitations which make it practically useless for simulations involving modern devices and signaling technologies. However, the IBIS-ISS specification defines useful and much-needed features through a standardized SPICE language. These features would enhance the current package modeling capabilities of IBIS significantly with minimal changes in the specification and little implementation effort in EDA tools.”	Can use IBIS-ISS format for package modeling

Approved IBIS BIRDs related to Power - 3

BIRD #	Title	Status	Statement	Value for this proposal
176	Power Pin Package Modeling	Accepted	“This BIRD enhances IBIS with interconnect modeling features to support broadband, coupled package, and on-die interconnect using IBIS-ISS and Touchstone data. The BIRD also adds a keyword for buffer rail mapping, to link to new terminal definitions defined for buffers”.	Similar interconnect model idea can be applied to system-level modeling.
189.7	Interconnect Modeling Using IBIS-ISS and Touchstone	Accepted	“Under the [Package] keyword, the IBIS specification defines a set of rules on the hierarchy of the various package modeling options. It is clearly stated that when present, the package information under the [Pin] keyword will override the package information in the [Package] keyword, and if present, the information in the [Package Model] and [Define Package Model] keywords will override the information in the [Pin] and [Package] keywords. The Usage Rules of the [Pin Numbers] keyword in the [Define Package Model] keyword section do not prohibit a “partial package model”, i.e., a model which only describes a subset of a Component’s pins. The problem is that there are no rules under the [Pin Numbers] keyword to describe what the EDA tool should do when the keyword doesn't contain the name of a pin that is listed in the component's [Pin] keyword. In the absence of rules, model makers and EDA tool vendors may make different assumptions which may lead to incorrect simulation results. For example, when a pin name is missing under the [Pin Numbers] keyword one EDA tool might make use of the RLC values in the [Pin] or [Package] keyword, while others might implement an open or short instead.”.	Same pin rule can be used as well.

The END