ALPHAWAVE SEMI

Rigorous Correlation Methodology for PCIe Gen5 & Gen6 DSP Based IBIS-AMI Models

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Outline

- Motivation
- DSP based IBIS-AMI
  - Modeling strategy
  - Model data path
  - Figure of Merit
- Correlation challenge
- Proposal
- Lab/simulation environment calibration
  - Stress methodology
  - Reference models
- Correlation regression
  - Simulation calibration 32GT/s
  - Model regression 32GT/s
  - Simulation calibration 64GT/s
  - Model regression 64GT/s
- Conclusion

Motivation

- IBIS-AMI model are powerful link performance prediction tools for SI engineers, “when they are correlated”
- Correlation setup for a given symbol rate / channel reach is not guaranteed to work at a different operation frequency of the SerDes and care must be taken to validate the models electrically across different standard/protocol around their intended operating point (loss, noise, jitter)
- For DSP receiver correlation requires capturing error statistics out of the DUT in the lab

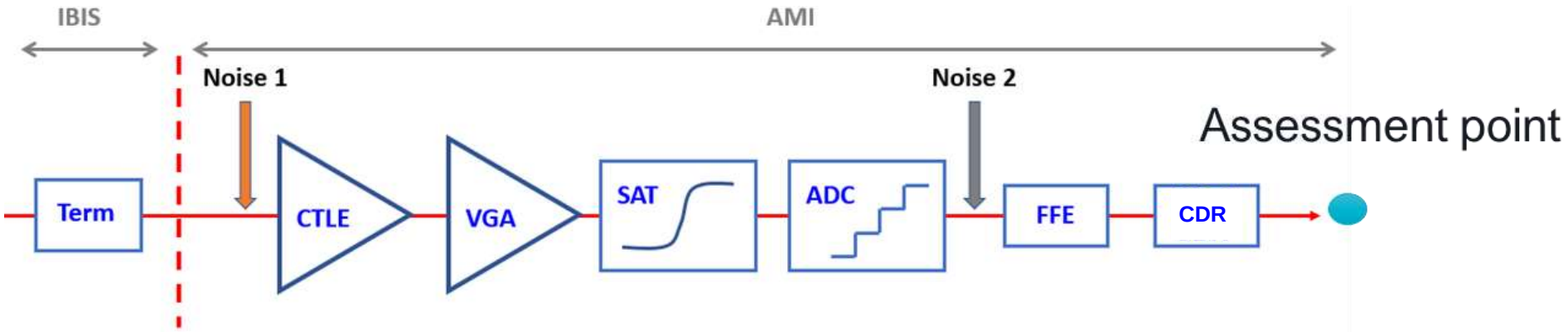
DSP based IBIS-AMI

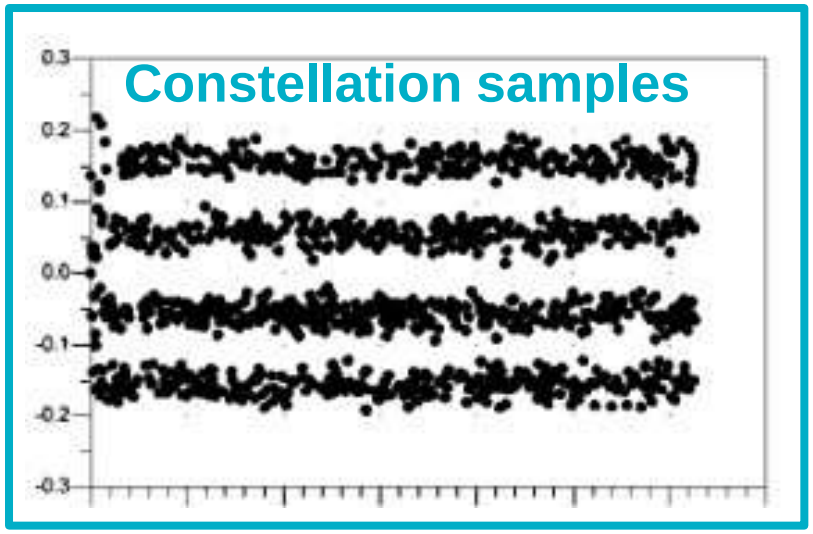
Modeling strategy

- The strategy proposed for the IBIS-AMI model is to use a layer of abstraction between the real architecture implementation and the model signal processing:
  - Longer life (can re-use across IP for several generation until large architecture change occur)
  - Less complex and easier to maintain
    - Some IP changes can be incorporated through re-correlation
  - Similar modeling as reference receiver from standard bodies, IEEE (COM), PCIe
    - Can re-use and compare parameters
  - Better thruput than an architecturally accurate representation
- With this abstraction, more attention need to be put on correlation
- Model internal tuning parameters need to be used for fine performance match with the actual silicon

DSP based IBIS-AMI

Model data path

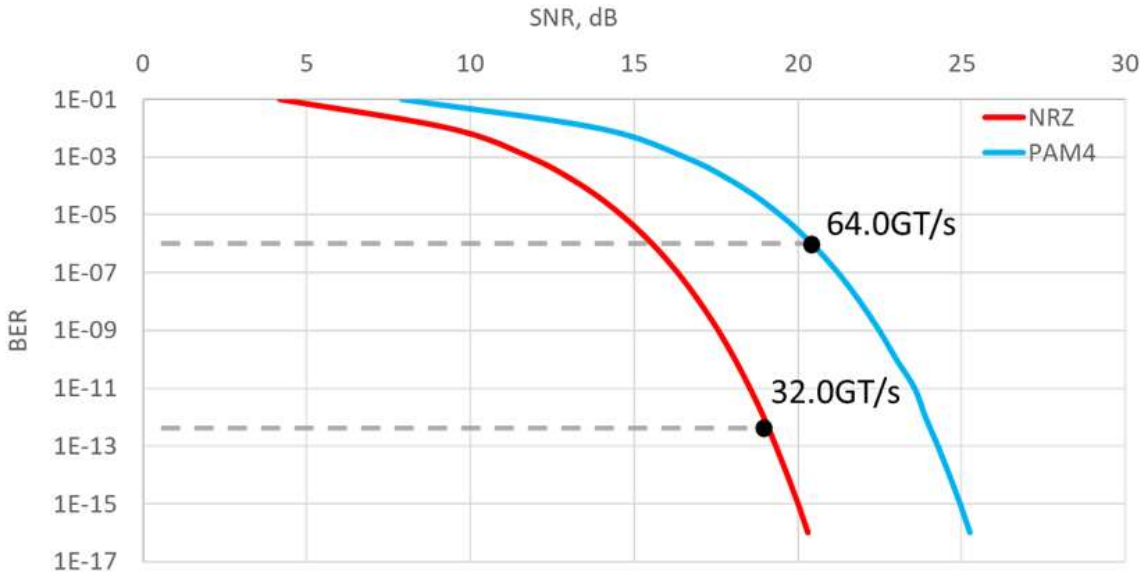




- Behavioral modeling of the data-path block, CTLE, VGA, Sat Amp, FFE
- Baudrate CDR to keep constant lock and provide sampling point for samples and calculating the constellation SNR
- All data-path signal conditioning is optimized in Statistical domain (AMI_Init function) for model thruput performance and fixed in transient domain
- Sample constellation is the only quantitative quantity that can be used for performance assessment

DSP based IBIS-AMI

Figure of Merit



- Errors are counted from the symbols sent/decoded by the IP
- Raw error counts/BER is used as a direct correlation metric
- Model BER will be calculated from its output sample's constellation SNR as error calculation is unpractical in simulation

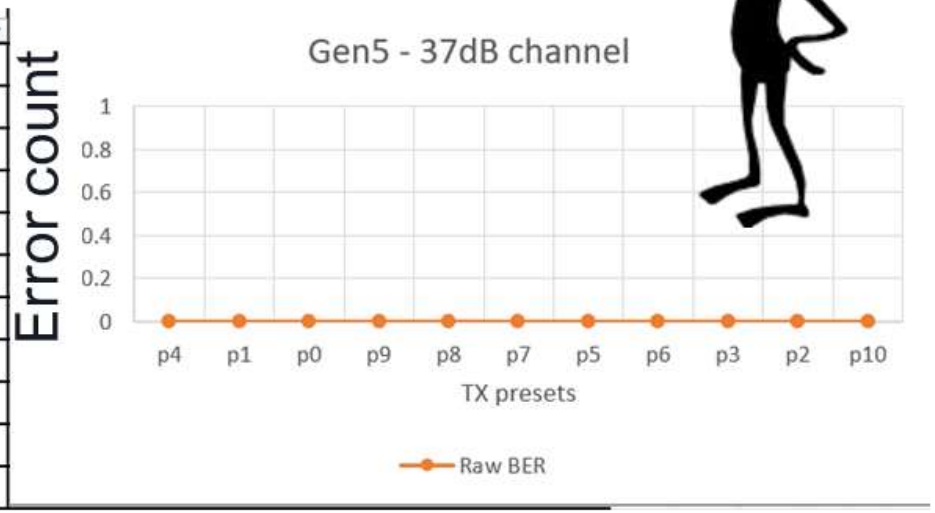
$$BER_{NRZ} = \left(\frac{1}{2}\right) erfc\left(\sqrt{\frac{10^{\frac{SNR}{10}}}{2}}\right)$$

$$BER_{PAM4} = \left(\frac{3}{8}\right) erfc\left(\sqrt{\frac{10^{\frac{SNR}{10}}}{10}}\right)$$

Correlation challenge

Loopback Test Setup

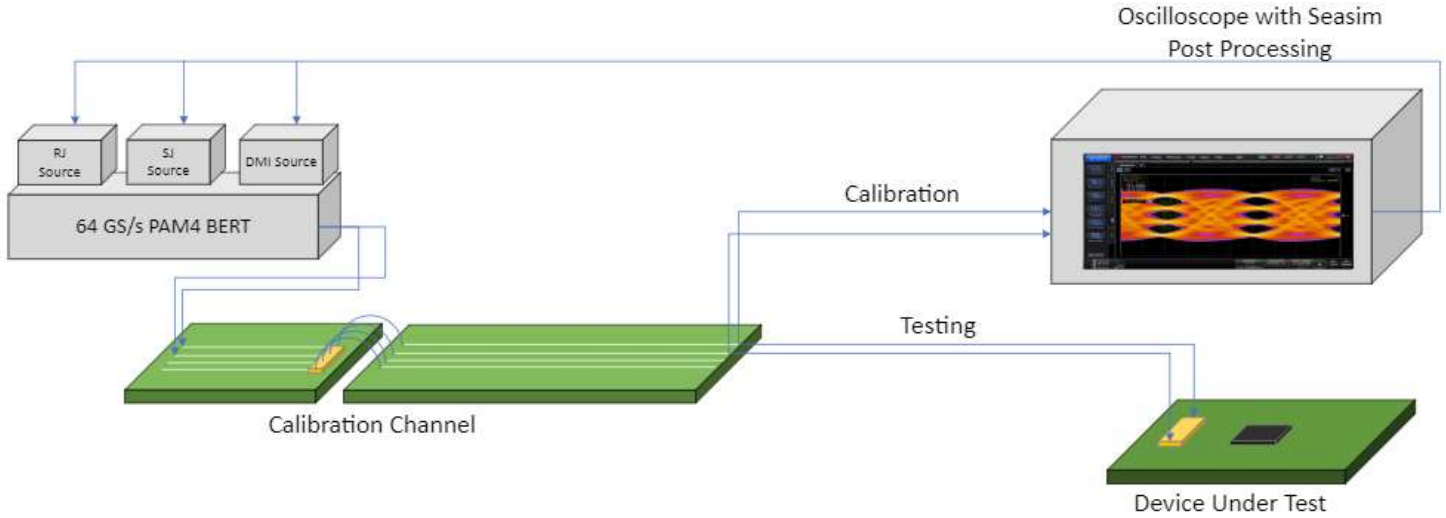
rx_bist_errors	rxbist_ber	txprese
0	0	p4
0	0	p1
0	0	p0
0	0	p9
0	0	p8
0	0	p7
0	0	p5
0	0	p6
0	0	p3
0	0	p2
0	0	p10



- 37dB loopback testing at 32GT/s does not provide error statistic for correlation purpose, baseline BER too low
- further increasing the loss will deviate from the intended operation point of the PCIe PHY and not a meaningful correlation point
- Indirect BER through constellation extrapolation not desired

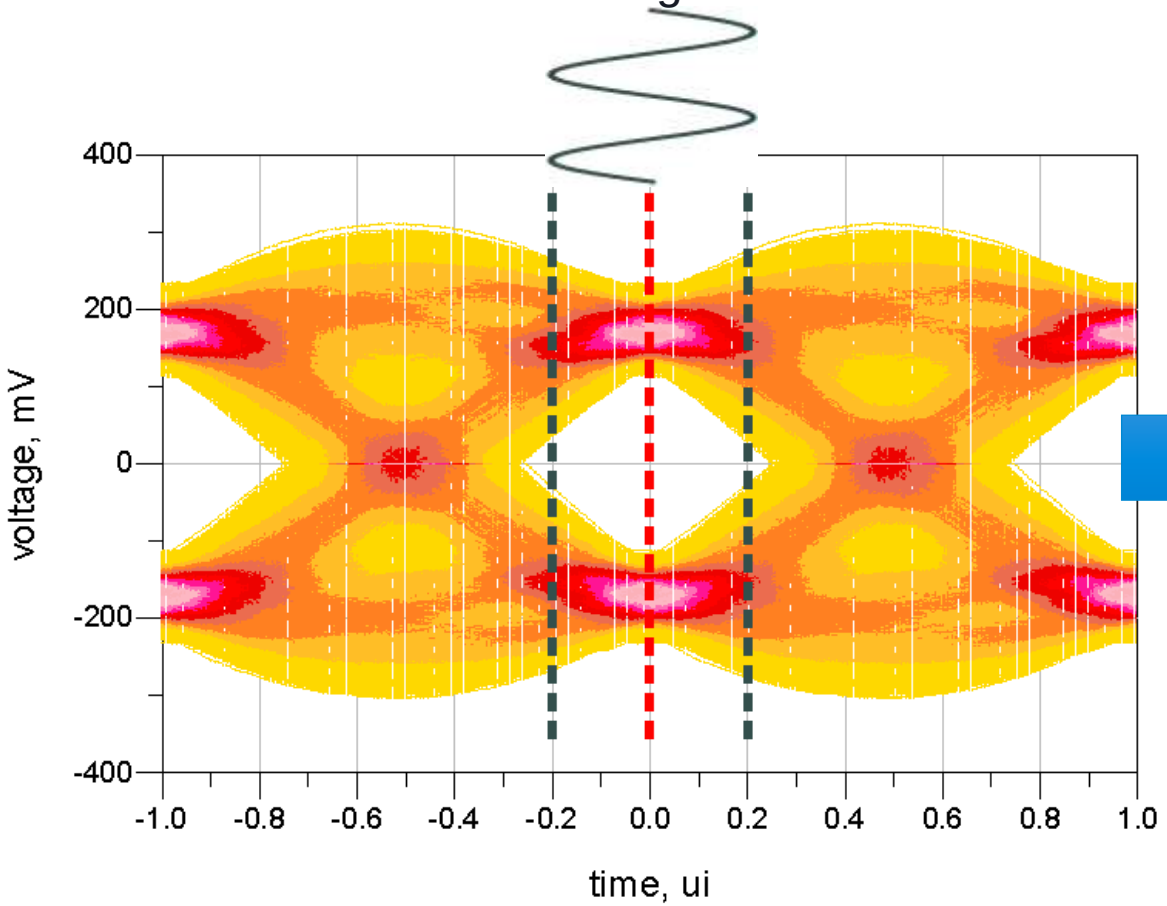
Proposal

- Stressing the channel with additional impairment required to guarantee measurable error statistics
- Use PCIe stress eye calibration methodology, why?
  - post-processing available in lab equipment
  - can be reproduced with generic IBIS-AMI models and used in EDA
- After stress calibration: correlate the lab and models with 100MHz single tone jitter tolerance

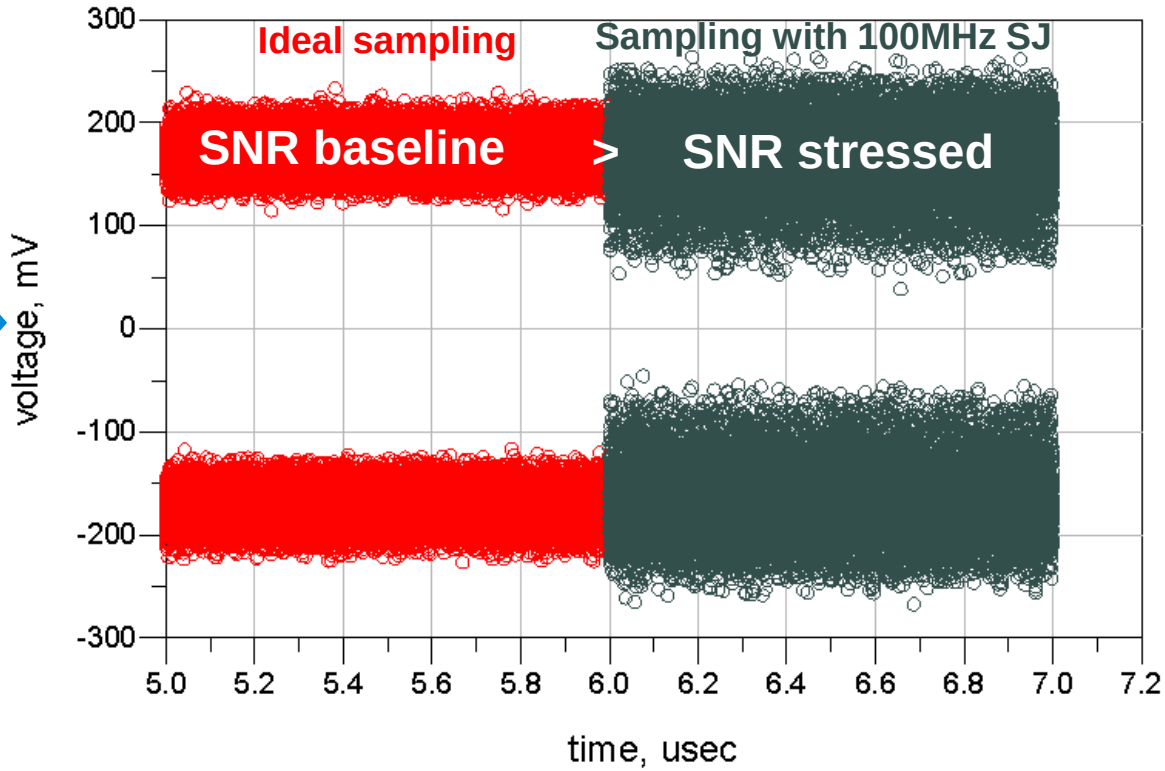


Proposal

100MHz single Tone SJ

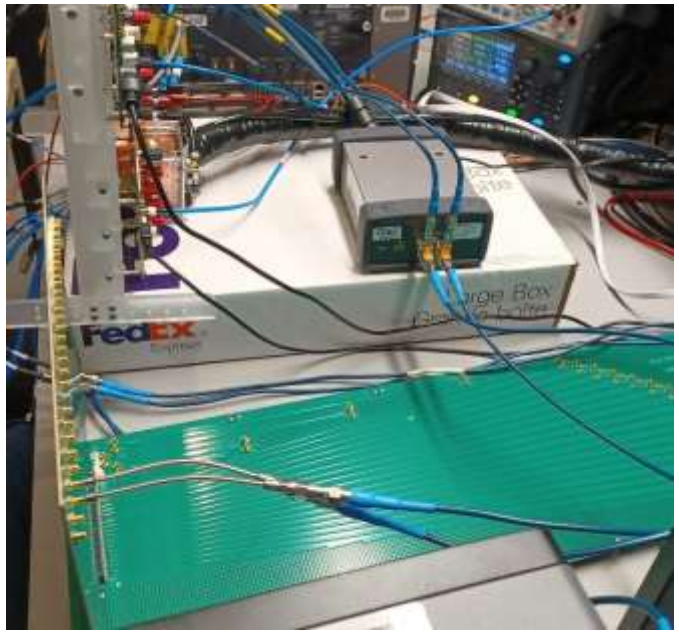


100MHz jitter not tracked by CDR
SNR is reduced

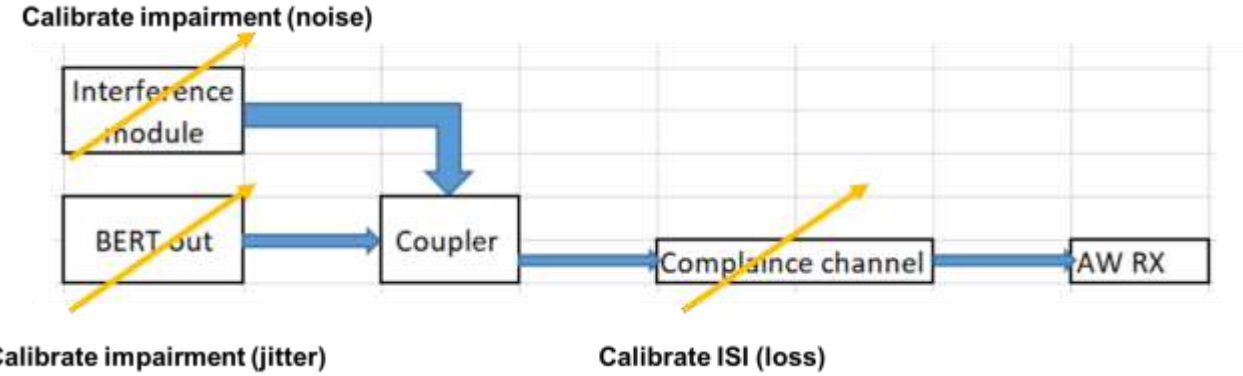


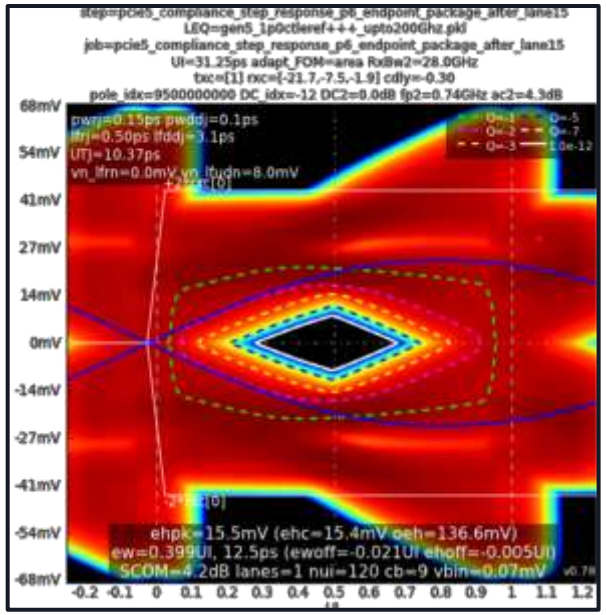
Lab/simulation environment calibration

Stress methodology



BERT impairment (jitter) and Interference module (noise coupling) are added injected the signal

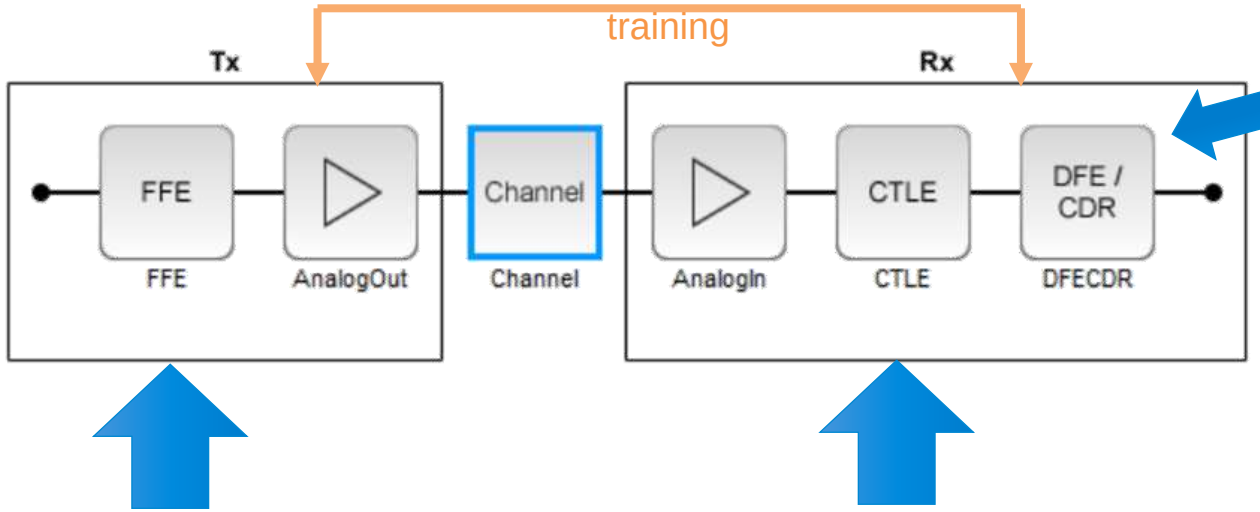




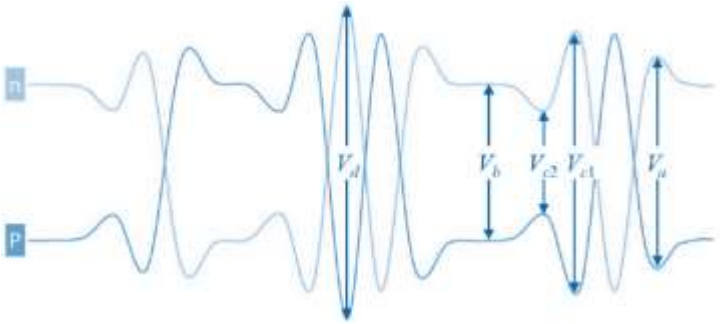
- Scope equipment provide necessary electrical post-processing (reference receiver model) to perform calibration to the desired eye opening metric.
- Same reference will be implemented and used in simulation EDA environment

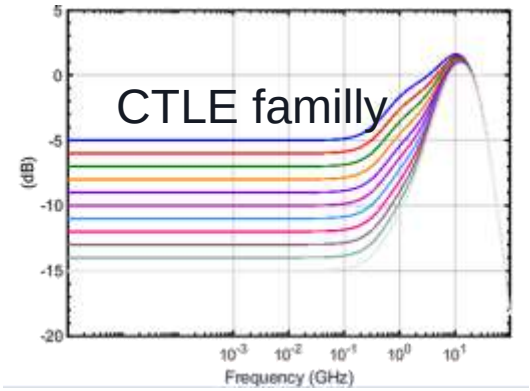
Lab/simulation environment calibration

Reference model



FIR preset





DFE tap number and constraint

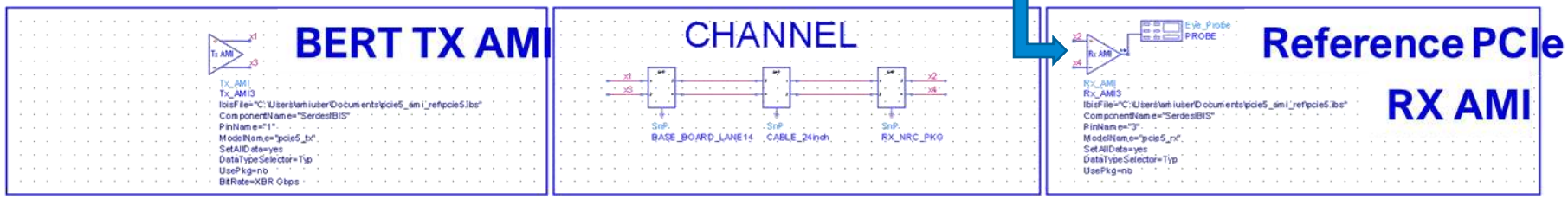
$$\frac{|d_1|}{h_0} < 0.8 \text{ and } \frac{|d_{2,3}|}{h_0} < 20\text{mV}$$

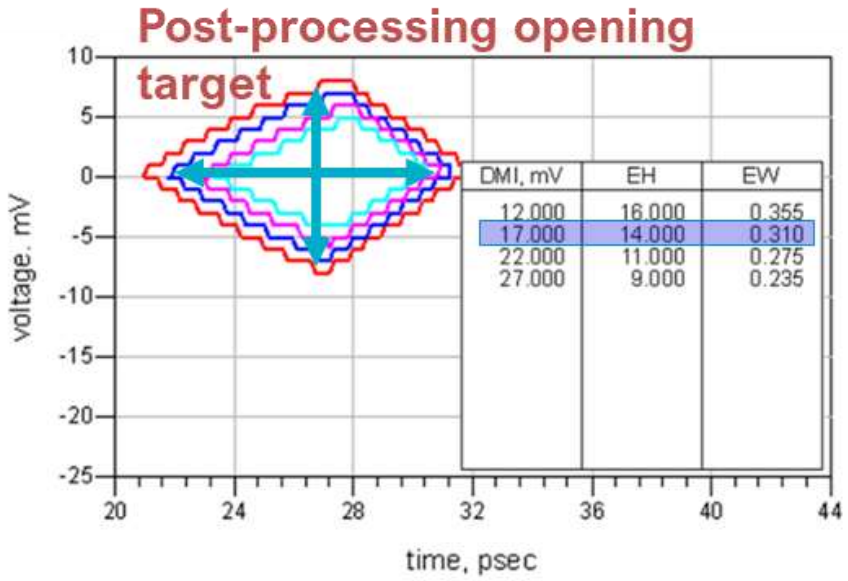
- A reference transceiver model is used to calibrate the signal that is applied to the DUT
- Calibration model should apply same EQ signal conditioning as in the lab
- Calibration will be done to a certain post-processed eye diagram opening
- Transmitter model implements FIR and preset training and is also used to inject noise, jitter
- The model definition will be wrapped into AMI to calibrate the simulation environment

Correlation regression

Simulation calibration 32GT/s

17mV DMI, Rj=16mUIrms

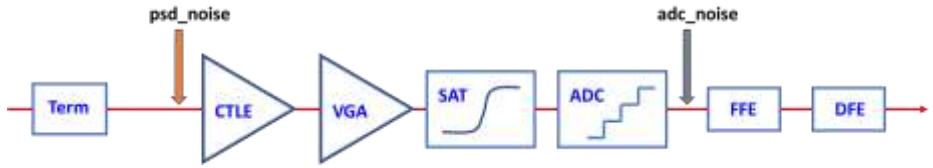




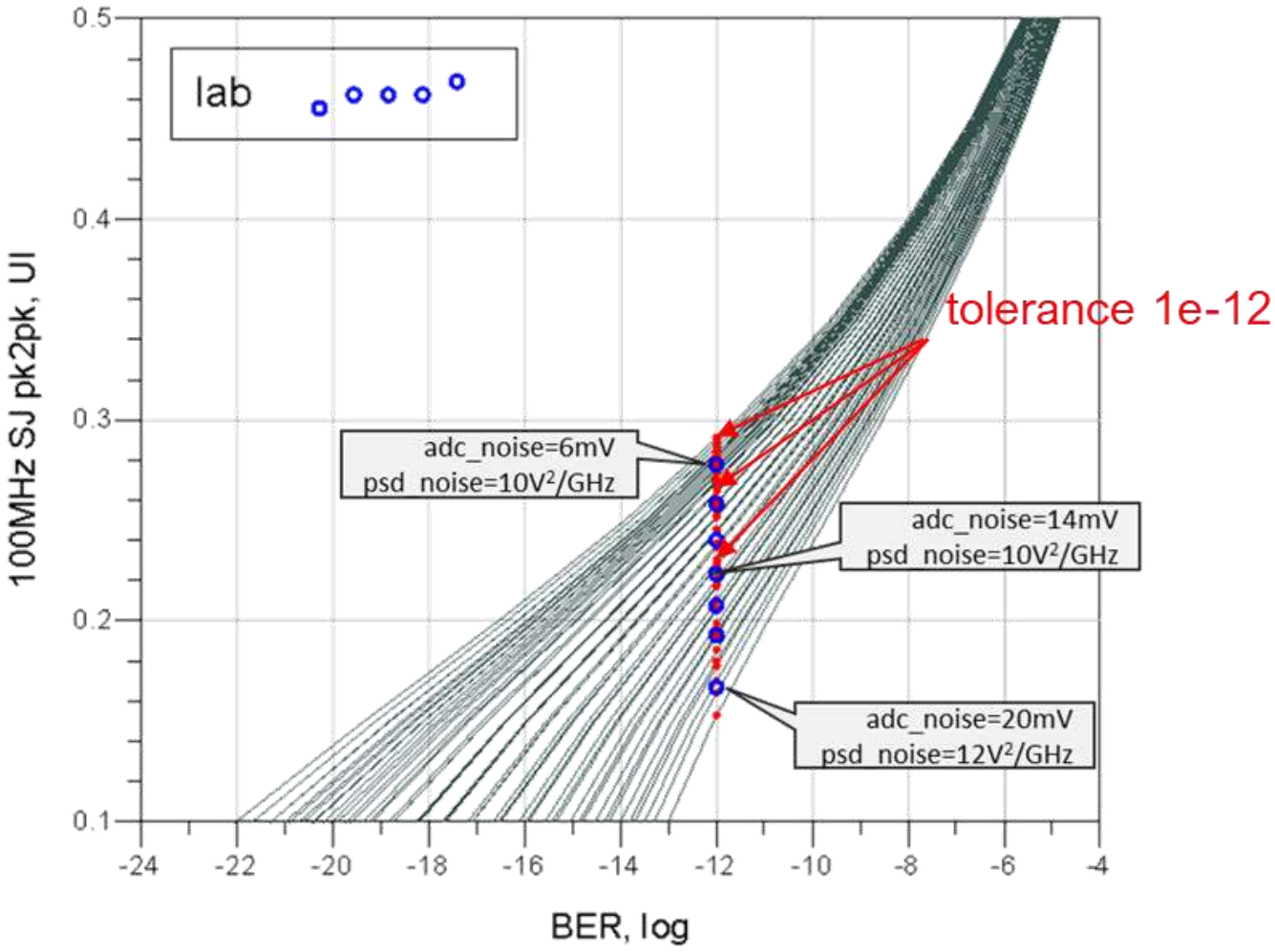
- Simulation environment follow same calibration methodology as in the lab to ensure the signal at the DUT model input is as stressful
- The reference receiver signal processing is wrapped into a generic AMI model to be consumed by the EDA
- The DMI, Rj impairment are applied and swept over as per the calibration methodology until the EDA post-processed eye diagram meet opening target

Correlation regression

Model regression 32GT/s

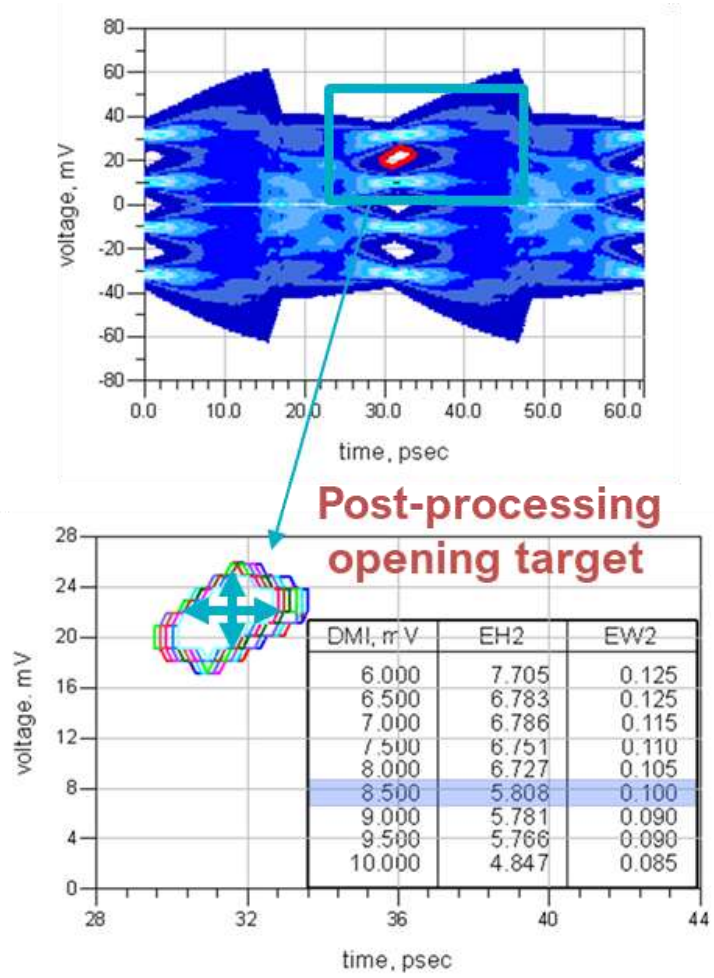


- BERT transmitter impairment were calibrated from previous step and are now fixed, and the reference receiver is replaced with the DUT IBIS-AMI model
- Sweep the model tuning noise and capture SNR/BER vs Sinusoidal Jitter amplitude at 100MHz
  - Sweep PSD noise from 0 to 20 V^2/GHz
  - Sweep ADC noise from 0 to 25mV



Correlation regression

Simulation calibration 64GT/s



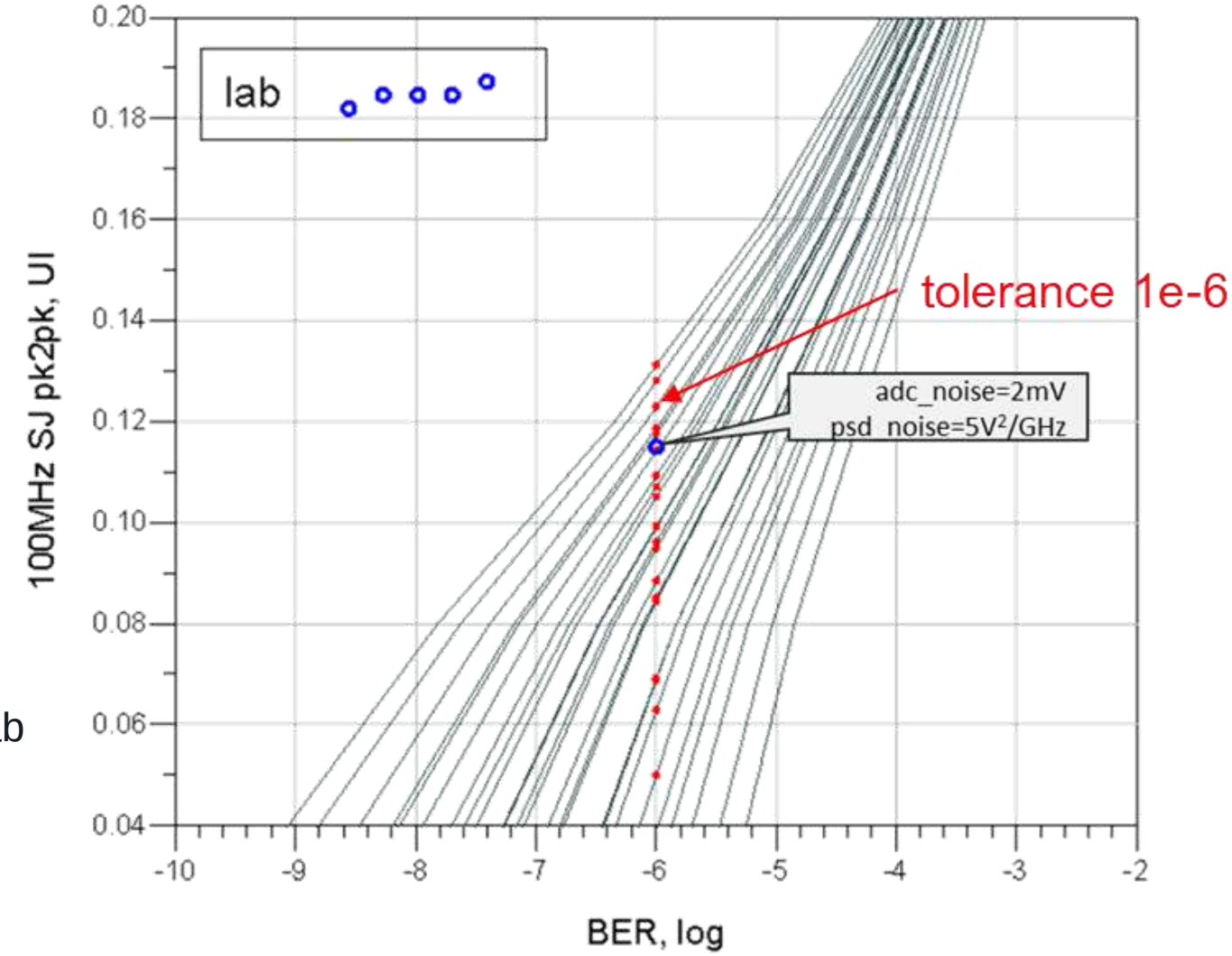
8.5mV DMI
Rj=3.5mUIrms

- Same calibration procedure as for 32GT/s
  - Allowed range for impairment (loss, jitter, noise) are reduced
- Reference models use the parameters for 64GT/s as defined in the PCIe base specification
  - New PKG model
  - Improved CTLE peaking, bandwidth (new set of CTLE curves)
  - Increased DFE number of taps
- For 64GT/s the calibration target is defined on the top eye only

Correlation regression

Model regression 64GT/s

- Sweep PSD noise from 0 to 10 V^2/GHz
- Sweep ADC noise from 0 to 4mV
- Check single-tone 100MHz SJ tolerance (max SJ peak-to-peak)
- Gen6 target BER is 1E-6
- Full PVT data has yet to be collected and only a nominal data point from the Gen6 DUT from the lab is shown



Conclusion

- The IBIS-AMI correlation was aligned with existing PCIe jitter tolerance procedure
- Calibration was reproduced in simulation with reference IBIS-AMI models generated per the specification equalization capability, to guarantee both model and silicon DUT were compared under same condition
- 100MHz single tone test provide SNR penalty from the baseline performance and allow enough error statistics to be recorded in the lab to drive correlation
- Regression over the DSP receiver IBIS-AMI model intrinsic noise tuning knobs provides a range of jitter tolerance that can captures the actual silicon performance
- A multi-corner model can be derived from the above regression to capture the performance envelope of actual silicon

Thank You!