Multi-Level Analog Buffer Modeling in IBIS

IBIS Summit at DesignCon 2023

February 3, 2023

Santa Clara, CA

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Outline

Motivation
Challenges
Potential solution

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Motivation

PAM4 was first introduced in IBIS v6.1 (in September 2015)

- This is only part of the AMI portion of the specification

This has been extended to PAMn in IBIS v7.2

- Still only in the AMI portion of the specification

There are times when simulating multi-level signaling using legacy I-V and V-t table-based IBIS [Model]s would be needed

- See presentation on *GDDR6X IBIS Modeling* at DesignCon 2021 IBIS Summit https://www.ibis.org/summits/aug21b/wolff2.pdf

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Challenges

The **algorithm** to support multi-level buffer models with I-V and V-t tables would not be too complicated

- We would need additional I-V tables to describe the buffer's impedance at each signal level, and
- We would need additional V-t tables to describe the buffer's switching characteristics between each of those levels
- We would need to extend the stimulus to support additional driven states (beyond the logic '1' and '0' states)

The challenges mostly revolve around **specification logistics**

- Inventing new keywords (not so bad)
- Defining the usage rules while maintaining compatibility with the rest of the specification (this is probably the most difficult task with the ever-growing specification)

A suggestion towards a solution (from Randy)

Extend the stimulus definition (only) to support multi-level signaling in the Multi-Lingual extensions of IBIS or in potential new keywords

- This would not pose any complications on the rest of the existing specification
- This would allow model makers to write multi-level analog buffer models using Verilog-A, VHDL-AMS or perhaps even IBIS-ISS. (The GDDR6 presentation mentioned earlier used a Verilog-A model).
- New keywords could also make use of this new stimulus in the future

The easiest way to achieve this might be to extend the currently available ‘1’, ‘0’ and ‘X’ logic state definition with integer values to represent the various voltage levels

- A slight complication would be related to the A_to_D and D_to_A converters, needed by the strictly analog external models
- The solution for that could be to define the stimulus as **V = intStimulus**, or provide an optional conversion factor in the form of **V = k * intStimulus + c**

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Quote from the current IBIS specification

The digital ports delivering signals to the AMS model, D_drive, D_enable, and D_switch, must be limited to the '1' or '0' states for VHDL-AMS, or, equivalently, to the 1 or 0 states for Verilog-AMS. The D_receive digital port may only have the '1', '0', or 'X' states in VHDL-AMS, or, equivalently, the 1, 0, or X states in Verilog-AMS. All digital ports other than the foregoing predefined ports may use any of the logic states allowed by IEEE Std. 1164-1993, or later.

SPICE, IBIS-ISS, VHDL-A(MS), Verilog-A(MS) versus VHDL-AMS and VERILOG-AMS:

SPICE, IBIS-ISS, VHDL-A(MS), Verilog-A(MS) cannot process digital signals. All SPICE, IBIS-ISS, VHDL-A(MS), Verilog-A(MS) input and output signals must be in analog format. Consequently, IBIS multi-lingual models using SPICE, IBIS-ISS, VHDL-A(MS) or Verilog-A(MS) require analog-to-digital (A_to_D) and/or digital-to-analog (D_to_A) converters to be provided by the EDA tool. The converter subparameters are declared by the user, as part of the [External Model] or [External Circuit] syntax, with user-defined names for the ports which connect the converters to the analog ports of the SPICE, IBIS-ISS, VHDL-A(MS), or Verilog-A(MS) model. The details behind these declarations are explained in the keyword definitions below.

Plan

Continue the discussions in the IBIS-ATM Task Group and refine the details

Submit a BIRD with the proposed enhancements for the IBIS specification

Questions, comments, suggestions welcome!

Thank you!

