IBIS: 30 Years and Counting
The Early History

Don Telian
SI Guys, USA
Arpad Muranyi
Siemens EDA, USA
Will Hobbs
Formerly Intel Corp., Retired

DesignCon Hybrid IBIS Summit
February 3, 2023
Santa Clara, California
A WORLD
WITHOUT IBIS

How could that be?!
The Perfect Storm

- PCI Spec -> Behavioral Modeling -> 5,000 hours
  - Arpad Muranyi
- Pentium Chipset
  - Analysis
  - Models to customers
- The “intel Buffer Information Sheet” -> iBIS
- Road trip
  - Some tools already had it

“a match on dynamite”
The 1.0 “Spec”

• Vision: The IBIS Open Forum
  – Begins 4/23/93, iBIS -> IBIS

• 7 to 9 EDA Vendors
  – “Intend to support IBIS”
  – Golden Waveforms -> “IBIS Capable”
  – BIRDs

• 1.0 spec resolved in 4 meetings
  – https://ibis.org/minutes/min1993/
  – Released to larger audience at DAC on 6/17/93
Technical Challenge and Solution

• Challenge simulating EISA bus at 50 MHz—SPICE models not accurate
• Verified inaccuracy on curve tracer
• Devised I/V method under HSPICE and tweaked until accurate enough
• Moved on to PCI development
• Refined model methodology (moved from Ramp to V/t)
Execution, Expansion

- My (Will Hobbs’) charter in Intel as Modeling Manager:
  - Assemble, develop and distribute logic and I/O models of Intel processors and chipsets to help customers with early designs
- Environment for I/O Buffer models within Intel in 1992
  - Spice Netlist level models
    - Not available for customers:
      - Too much proprietary info, too slow to simulate
  - Simplified Electrical Models (SEM/First Order Models)
    - Behavioral, created by x86 CPU division
    - Simple RLCD models tweaked to emulate I/O characteristics
    - Generated largely by hand, then automated
    - Fast, supported by all analog simulators
    - Limited in accuracy at process corners, complex load topologies
    - Time-consuming to generate and validate
  - “Second Order Models”
    - Behavioral, created by chipset division
    - Tabulated list of I/O characteristics over corners
    - Generated by simulation or measurement
    - Fast, but only supported by two analog simulators
- Some inter-divisional friction apparent (1st order versus 2nd order models)
First Intel I/O Modeling Summit and Workgroup

- November 1992 road trip to visit European customers—message clear: accurate and consistent models needed 6 months to 1 year before silicon
- Convened I/O Buffer Modeling Summit within Intel on 12/7/92
  - Participants included divisions producing and consuming models, and technologists
  - Presentations described both SEM and 2\textsuperscript{nd} order models in detail
  - Light bulb moment: SEM is a subset of 2\textsuperscript{nd} order model, not in conflict
- Formed internal working group to hammer out convergence
  - Met weekly, addressed:
    - Model generation and validation methods (automation, “golden topologies”)
    - Accuracy
    - What corners to support (fast, slow, average)
    - Distribution to customers
    - Support by EDA Vendors
  - Coined name, iBIS (Intel Buffer Information Sheet), quickly changed it to IBIS (I/O Buffer Information Sheet) to encourage other IC Vendors to join
  - Final nut to crack: getting more than 2 EDA vendors to support IBIS
Engaging the Industry

• First IBIS Open Forum for the Wider Industry: 4/23/93
  – Don Telian convened meeting to address lack of broader EDA Support
    • 7 Simulator Vendors and Intel took part: Hyperlynx, Integrity, Intusoft, Meta-Software, MicroSim, Quad-Design, Quantic Labs
  – Open Forum met biweekly
    • Other EDA vendors joined: Cadence Design, Contec
    • Agreement reached on content of IBIS V1.0 by third meeting, 5/21/93

• IBIS opened to the industry at DAC, 6/17/93
  – Broader participation:
  – IBIS changed to I/O Buffer Information Specification (instead of Sheet)
  – Version 1.0 ratified
  – Agreed to tri-weekly or monthly meetings and additional Face-to-Face Summits
Subsequent Growth, the Next 3 Years

- Formalized IBIS Open Forum
  - Chose officers
    - Will Hobbs, Chair through 1/97; various treasurers and librarians
  - Addressed improving and enhancing IBIS
    - Introduced the Buffer Issue Resolution Document, or “BIRD”
  - Set up database, email reflector
  - Formalized charter and other administrivia
  - Did Trademark Search
  - Set up bank account
  - Encouraged press, wrote articles and press releases
    - Featured in December, 1993 EDN in their “Hot 100 Products” of the year

- Expanded membership
  - Critically, more silicon vendors
  - Additional EDA Vendors
More Progress

• Created additional support collateral
  – Golden Parser, funded by member companies
    • Suggested by Jon Powell, developed by Paul Munsey and Ron Neville
    • Freed us from having to hand-check users’ models
  – Cookbook—aided model users and developers
• Continued improving the spec
  – E.g., Added Support for more devices (ECL, Open Drain, improved package models, ...)
• Affiliated with standards organizations
  – Nationally (US), IBIS V2.1 became ANSI/EIA-656
  – Internationally, affiliated with IEC, resulting in IEC-62014
• In January, 1997, I (Will Hobbs) turned over the gavel:
  – Chair: Bob Ross
  – Vice Chair: Syed Huq
  – Librarian: Jon Powell
• And the rest, as they say, is history
• Here’s to 30 more years!!

2/3/2023
Appendix
What the early IBIS Sheets Embodied

Elements of an I/O Structure

Example IBIS Sheet
IBIS and Simplified Electrical Model Correlation

Simplified Electrical Model (SEM)

Correlation Between SEM and IBIS Parameters

<table>
<thead>
<tr>
<th>SEM Parameter</th>
<th>Corresponding IBIS parameter</th>
<th>IBIS Diagram Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>dV/dt</td>
<td>Ramp Time</td>
<td>4</td>
</tr>
<tr>
<td>Ro</td>
<td>Simplified Output Resistance</td>
<td>6</td>
</tr>
<tr>
<td>Co, Cin</td>
<td>C_comp</td>
<td>5</td>
</tr>
<tr>
<td>Lp, Cp</td>
<td>L_pkg, C_pkg</td>
<td>5</td>
</tr>
</tbody>
</table>
IBIS Input Structure
### Early IBIS Sheet Example

#### File Name: example.ibs

- **File Name:** example.ibs
- **File Rev:** 1.0
- **Component:** p24c

<table>
<thead>
<tr>
<th>V_ol</th>
<th>I(typ)</th>
<th>I(min)</th>
<th>I(max)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-2.0</td>
<td>-340</td>
<td>-400</td>
<td>NA</td>
</tr>
<tr>
<td>-1.5</td>
<td>-190</td>
<td>-210</td>
<td>NA</td>
</tr>
<tr>
<td>-1.0</td>
<td>-60</td>
<td>-75</td>
<td>NA</td>
</tr>
<tr>
<td>0.0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0.5</td>
<td>19</td>
<td>33</td>
<td>NA</td>
</tr>
<tr>
<td>1.0</td>
<td>33</td>
<td>57</td>
<td>NA</td>
</tr>
<tr>
<td>1.5</td>
<td>41</td>
<td>74</td>
<td>NA</td>
</tr>
<tr>
<td>2.0</td>
<td>44</td>
<td>83</td>
<td>NA</td>
</tr>
<tr>
<td>2.5</td>
<td>44</td>
<td>85</td>
<td>NA</td>
</tr>
<tr>
<td>3.0</td>
<td>45</td>
<td>85</td>
<td>NA</td>
</tr>
<tr>
<td>3.5</td>
<td>45</td>
<td>86</td>
<td>NA</td>
</tr>
<tr>
<td>4.0</td>
<td>45</td>
<td>86</td>
<td>NA</td>
</tr>
<tr>
<td>4.5</td>
<td>45</td>
<td>87</td>
<td>NA</td>
</tr>
<tr>
<td>5.0</td>
<td>46</td>
<td>87</td>
<td>NA</td>
</tr>
</tbody>
</table>

#### Beyond the Rail Info

- **GND_clamp:** NA
- **POWER_clamp:** 140m
- **R_pkg:** NA
- **V_I (typ):** 140m
- **I(min):** 325m
- **max:** 140m
- **L_pkg:** 8.52nH
- **C_pkg:** 6pF
- **C_comp:** 6.1pF

#### Table

<table>
<thead>
<tr>
<th>Variable</th>
<th>typ</th>
<th>min</th>
<th>max</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_comp</td>
<td>12.0pF</td>
<td>10.0pF</td>
<td>15.0pF</td>
</tr>
</tbody>
</table>

#### Pin List

<table>
<thead>
<tr>
<th>Pin</th>
<th>signal_name</th>
<th>model_name</th>
<th>R_pin</th>
<th>L_pin</th>
<th>C_pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RAS0#</td>
<td>Buffer1</td>
<td>200.0m</td>
<td>5.0nH</td>
<td>2.0pF</td>
</tr>
<tr>
<td>2</td>
<td>RAS#1</td>
<td>Buffer2</td>
<td>209.0m</td>
<td>NA</td>
<td>2.5pF</td>
</tr>
<tr>
<td>20</td>
<td>Vcc5</td>
<td>POWER</td>
<td>226.0m</td>
<td>NA</td>
<td>1.0pF</td>
</tr>
</tbody>
</table>

---

**File Name:** example.ibs

- **File Rev:** 1.0
- **Component:** p24c

<table>
<thead>
<tr>
<th>V_ol</th>
<th>I(typ)</th>
<th>I(min)</th>
<th>I(max)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-2.0</td>
<td>-340</td>
<td>-400</td>
<td>NA</td>
</tr>
<tr>
<td>-1.5</td>
<td>-190</td>
<td>-210</td>
<td>NA</td>
</tr>
<tr>
<td>-1.0</td>
<td>-60</td>
<td>-75</td>
<td>NA</td>
</tr>
<tr>
<td>0.0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0.5</td>
<td>19</td>
<td>33</td>
<td>NA</td>
</tr>
<tr>
<td>1.0</td>
<td>33</td>
<td>57</td>
<td>NA</td>
</tr>
<tr>
<td>1.5</td>
<td>41</td>
<td>74</td>
<td>NA</td>
</tr>
<tr>
<td>2.0</td>
<td>44</td>
<td>83</td>
<td>NA</td>
</tr>
<tr>
<td>2.5</td>
<td>44</td>
<td>85</td>
<td>NA</td>
</tr>
<tr>
<td>3.0</td>
<td>45</td>
<td>85</td>
<td>NA</td>
</tr>
<tr>
<td>3.5</td>
<td>45</td>
<td>86</td>
<td>NA</td>
</tr>
<tr>
<td>4.0</td>
<td>45</td>
<td>86</td>
<td>NA</td>
</tr>
<tr>
<td>4.5</td>
<td>45</td>
<td>87</td>
<td>NA</td>
</tr>
<tr>
<td>5.0</td>
<td>46</td>
<td>87</td>
<td>NA</td>
</tr>
</tbody>
</table>

#### Beyond the Rail Info

- **GND_clamp:** NA
- **POWER_clamp:** 140m
- **R_pkg:** NA
- **V_I (typ):** 140m
- **I(min):** 325m
- **max:** 140m
- **L_pkg:** 8.52nH
- **C_pkg:** 6pF
- **C_comp:** 6.1pF

#### Table

<table>
<thead>
<tr>
<th>Variable</th>
<th>typ</th>
<th>min</th>
<th>max</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_comp</td>
<td>12.0pF</td>
<td>10.0pF</td>
<td>15.0pF</td>
</tr>
</tbody>
</table>

#### Pin List

<table>
<thead>
<tr>
<th>Pin</th>
<th>signal_name</th>
<th>model_name</th>
<th>R_pin</th>
<th>L_pin</th>
<th>C_pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RAS0#</td>
<td>Buffer1</td>
<td>200.0m</td>
<td>5.0nH</td>
<td>2.0pF</td>
</tr>
<tr>
<td>2</td>
<td>RAS#1</td>
<td>Buffer2</td>
<td>209.0m</td>
<td>NA</td>
<td>2.5pF</td>
</tr>
<tr>
<td>20</td>
<td>Vcc5</td>
<td>POWER</td>
<td>226.0m</td>
<td>NA</td>
<td>1.0pF</td>
</tr>
</tbody>
</table>
I/O-buffer modeling spec simplifies simulation for high-speed systems

DERRICK DUEHREN, WILL HOBBS, ARPAD MURANYI, AND ROBIN ROSENBAUM, INTEL CORP

Most I/O-buffer modeling methodologies use actual circuit designs and reveal detailed, sensitive information about the buffer design and the underlying fabrication processes. These methods often yield slow simulation, have inaccuracies, and are generally not compatible with all vendors' simulation platforms. A standard called IBIS (I/O-buffer information specification) addresses these shortcomings and fills the need for widely available simulation models for high-speed design. IBIS uses behavioral modeling as opposed to transistor-level Spice simulation. In order to understand the advantages of IBIS, it is helpful to review the two types of modeling.

A designer who wishes to obtain a model for a particular I/O buffer has two options. You can acquire transistor-level Spice models from some manufacturers. A transistor-level model allows for modeling of second-order effects, such as ground bounce. The model is useful for small-scale simulations of a few nets or drivers. Using a detailed model of this type, you can establish project design rules or do a worst-case analysis on a particular net. However, transistor-level models often are not well-suited for simulating an entire PCB board of several hundred nets and drivers.

CAE programs can extract the transmission-line parameters $\Gamma_2$ and $\Gamma_3$ of a net from the board-layout database and put them into Spice elements. However, using Spice to simulate several hundred transistor-level models and then sifting through the results for signal integrity or flight-time information is clearly impractical. In addition, you have the problem of obtaining transistor-level models from manufacturers. An IC vendor is understandably reluctant to reveal the sensitive process and design information contained in Spice models. Also, many manufacturers use their own in-house silicon-simulation tools, so generic Spice models may not be readily available.

Your other simulation option is to construct a behavioral model of the device. With this type of modeling technique, the dc, ac, and packaging information serve to create a "black-box" model of the I/O buffer. This technique has several advantages: It is fast and nonproprietary, and you can easily access the required information via measurement. More important, several CAE vendors, such as Interconnectix, Quad Design Technologies, and Hyperlynx, supply software that specifically targets the simulation of hundreds of nets and drivers on a PCB board.

These large-simulation programs require behavioral-style I/O-buffer models. Unfortunately, until now, no standard method existed to either extract or format the information. A behavioral I/O-buffer model for one vendor's CAE program would at least require retargeting for another program. Because no standard format existed, IC vendors were reluctant to create and maintain several behavioral models of a device. This no-win situation called for a common I/O-buffer model standard administered by an open industry consortium. The standard would have to protect proprietary information, capture significant product details, allow faster time to market, and establish industry-wide compatibility.

How IBIS fills the need

IBIS offers several advantages over previous I/O-buffer model-development methodologies. IBIS relies on tabulated current-vs-voltage (IV) characteristics, rise- and fall-time characteristics, and package information. It protects vendors' intellectual property by providing models that reveal no proprietary information about the design or process technology.
EDN Hot 100 Products of 1993

Active-filter design tool. Filtr 3.1 helps you design, optimise, and analyze active filters on a PC using DOS. The software gives you a choice of 19 active-filter topologies and includes a gain-sensitivity-product minimization algorithm that accounts for both passive and active sensitivities.

Consulting and Training Services, Sharps, Pl. (407) 633-9868. Circle No. 513

Low-cost DSP analysis software. Siglab is an interpretive DSP language for signals and systems analysis. You use it to generate test signals and system responses and display them using 2-D and 3-D graphics in multiple windows that allow data location, zoom, and overlay. The software includes 140 built-in mathematical and systems operations used in DSP, including FFTs, fast Fourier transform, support, matrix algebra, polynomial generation and evaluation, window generation, complex arithmetic, and signal operators (convolution, correlation). DCB, 3417 N. Hwy. 3, Arlington, TX. Circle No. 517

Learn VHDL for free. A self-paced audio-visual tutorial from Racal-Redac lets you use your workstation to learn how to apply VHDL. The tutorial runs under Unix and makes use of the company's Dramatix/Instruct multimedia program. Once you load the program, you sit through a realistic 15-minute overview that steps you through a simple design, runs a simulation, sets breakpoints in the VHDL code, makes corrections, and so on, as you follow along. You also get VHDL-LE, a self-paced education package that lets you work through the exercises in a manual and workbook. The program usually takes 40 hours to complete. The software requires a VAX/VMS or Sun-based workstation and approximately 20 MB of disk space. The company aims to materialize at its customers, but it's free to qualified designers. Racal-Redac, Mahwah, NJ. (201) 848-8000. Circle No. 514

Simulating switch-mode power supplies. A free newsletter from Intusoft describes models for switching converters including buck, boost, buck-boost, and Cuk topologies. Contact the company for a copy of its March newsletter. Intusoft, San Pedro, CA. (310) 633-0710. Circle No. 515

High-precision on-chip Kelvin bridge. A simple circuit is available that allows precise measurement of surface potentials without the need to measure a reference potential. The circuit is called the Kelvin bridge and is designed to have a high input impedance. The company offers a 50-ohm Kelvin bridge with a resolution of 10 nanometers. The bridge is available in a ceramic package and is designed for high-precision measurements. Kelvin Bridge, 500 W. 11th St., Suite 202, Santa Monica, CA. (310) 528-4724. Circle No. 517

Solid-state relay. The HSSR-T110 has four-channel solid-state relays housed in an 8-pin hermetic DIP. Contacts are rated for 0.8A ac/dc at 24V ac or 28V dc. The relay operates from a logic-level control signal (5 mA nom). Input/output isolation equals 1500V dc. The unit operates over the 0 to 125°C military temperature range. R. Hewlett-Packard Co., Santa Clara, CA. (408) 752-6000. Circle No. 518

MS Excel-based worksheets and macros. Nineteen electronic-design tools based on MS Excel spreadsheet software are available individually or as a complete package. The software includes linear system analysis, spectral analysis, RF design, general engineering tools, and hardware component selection. Linear system applications include analyzing both analog and digital systems. A spectral analysis tool produces FFTs of data. Engineering Solutions, Tarzana, CA. (818) 722-2321. Circle No. 519

Input module. The 7835 4- to 20-mA current input module includes an isolated loop power supply, which eliminates the need for an external supply when using a 2-wire transmitter. It operates from a single unregulated 24V supply and features a ±0.1% max span error, ±0.02% span nonlinearity, and ±1°F temperature stability. A galvanic transformer provides 1500Vrms isolation. The module meets IEEE-STD-472 and NEC-253-4 standards for transient protection. From $75 (1000). Analog Devices Inc., Wilmington, MA. (617) 977-1242. Circle No. 52

MOSFETs. The S1940DY and S19410DY are rated 600V and 30V, respectively. The units are housed in 8-pin surface-mount packages and are mounted on low thermal-impedance copper heat sinks, which allow the units to dissipate 2.5W. The

IBIS Technologies, 30 Years and Counting

IBIS: 30 Years and Counting

IBIS Hot 100 Products of 1993
Treat pc-board traces as transmission lines to specify drive buffers

Donald Tellier, Intel Corp.

The Peripheral Component Interconnect (PCI) specification simplifies the design of buffer circuitry in high-speed interface systems. By using transmission-line concepts and employing ac specifications in place of dc values, PCI lets designers more accurately define a buffer's drive capability.

By employing transmission-line models and terms, the PCI specification developed by Intel Corp can thoroughly characterize the dynamic effects that result when you switch large distributed loads with a underspecified drive buffer. Because many designers oversimplify this problem, designing buffers with appropriate drive strength turns into a difficult task. Historically, designers have assumed that buffers work into simple capacitive loads. This assumption created few problems when system clock rates loaded along in the 1-MHz range. In today's world of 30-MHz plus clock rates, however, real system loads are far from purely capacitive. In fact, even pc-board trace lengths can dramatically change the makeup of a buffer's load.

Viewing the buffer load as a simple capacitor can lead to many erroneous conclusions. The most common mistake designers make is to assume that an interconnect with many loads is like a large capacitor, which must therefore require a buffer with a large drive capability. It turns out that this is not the case, and designers must understand the transmission-line mechanisms involved here. To better understand the difference in driver response between a capacitive load and a true system load, consider Fig 1a.

Here, a system load is actually made up of numerous devices interconnected through traces that you can model as transmission lines. Aside from their clamping characteristics, the receiving devices are predominately capacitive. However, the system model represents a distributed capacitance and yields waveforms