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A Practical Review of IBIS DDR5 Enhancements

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DesignCon2024 Hybrid IBIS Summit
Santa Clara, California
February 2, 2024

SPEAKERS

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Douglas Burns is a Principal Consultant and founder of SI-Clarity LLC. He has worked in ASIC design, Package Design, PCB design of Memory and Serial Links, and the development of IBIS-AMI models. Doug's current focus is on solving critical Signal Integrity and Power Integrity problems, accelerating customer analysis, and providing training and mentorship to engineering teams.

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Pegah Alavi is a Senior Applications Engineer at Keysight Technologies, where she focuses on Signal Integrity and High-Speed Digital Systems and Applications. Pegah is focusing on various high speed digital standards which include DDR, PCIe, USB, and UCIe to name a few. Before joining Keysight Technologies, Pegah worked on system level modeling of analog and mixed signal circuits to best predict the overall systems performance and accurately represent each component.

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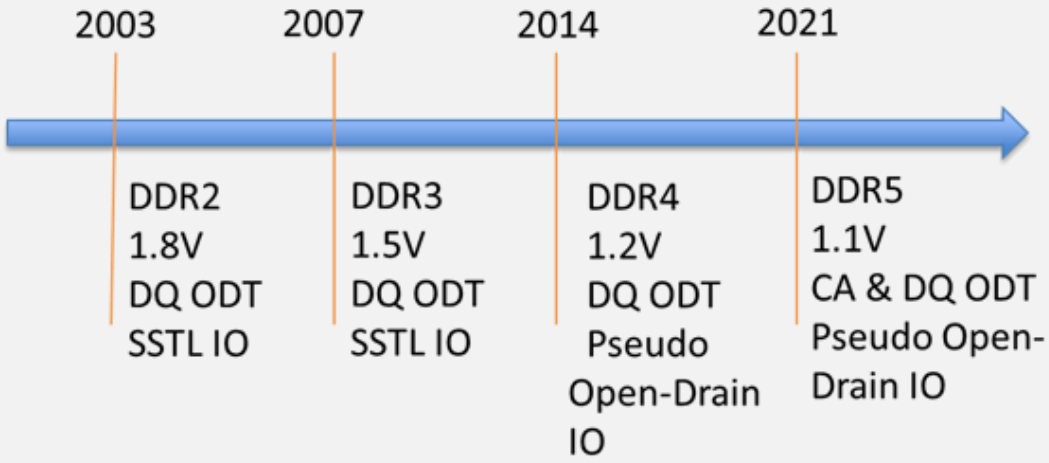
Agenda

- Introduction
  - Memory Performance
  - IBIS and IBIS-AMI Brief Overview
  - DDR5 Overview
- New IBIS-AMI Features for DDR Analysis
  - DC Offset
  - DLL Function Programmability
  - Clock- Data Pin Relationship
  - Clock Forwarding
  - Statistical Back Channel
- DDR5 Equalization Modeled In IBIS-AMI
- Summary

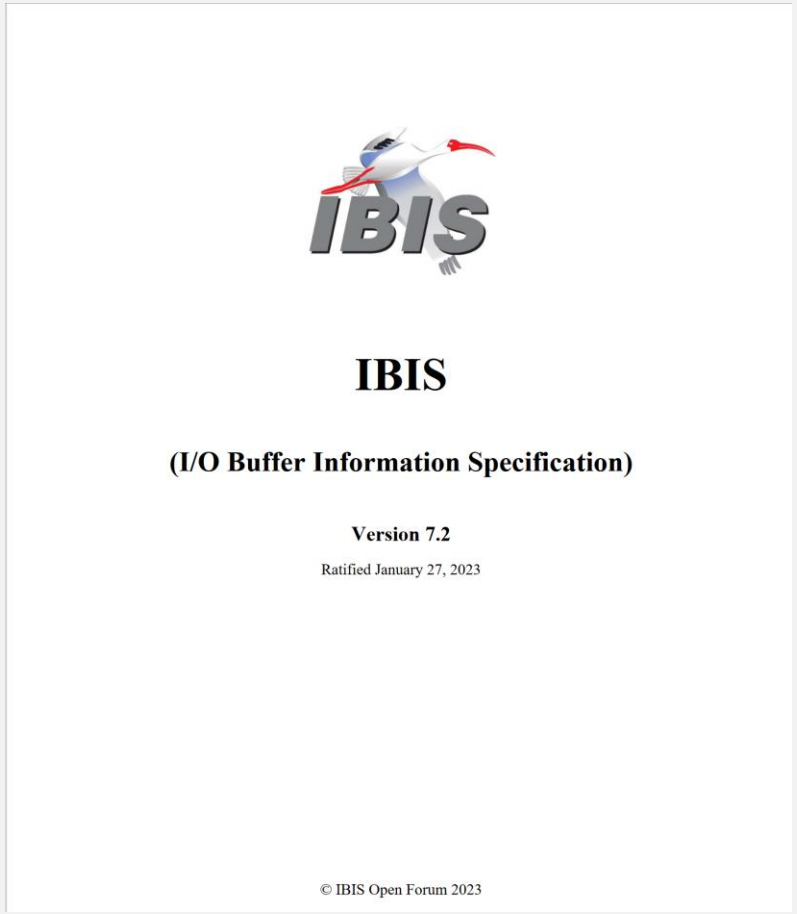
Introduction: Memory Performance

- **Memory Evolution for the Past two Decades**
  - DDR2: 2003: 533 → 800 MTS
  - DDR3: 2007: 1066 → 1600 MTS
  - DDR4: 2014: 2133 → 4800 MTS
    - *Each generation built on:*
      - Improved Memory Architectures
      - Signaling and termination Modifications
  - DDR5: 2021: 3200 → 8400 MTS
    - *Improved Memory Architectures*
    - *Emphasis on signal processing*
      - FFE, DFE



Introduction: IBIS and IBIS-AMI Overview

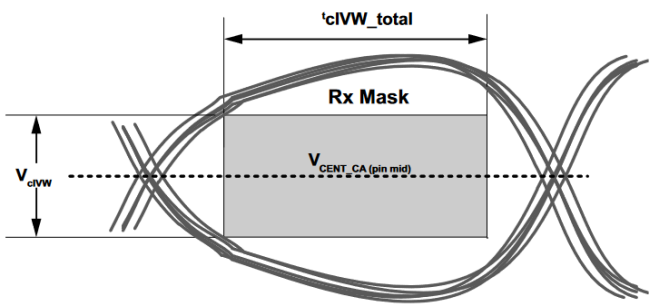
- **IBIS**
  - Behavioral Modeling Standard
  - Created in 1993
  - Improves Simulation speed
  - Protects IO IP
- **IBIS-AMI**
  - Introduces Algorithmic Modeling
    - *Complex modeling of pre driver capabilities*
    - *FFE, DFE, CTLE, etc.*
  - Supports Channel Simulation for LTI models
    - *Statistical (LTI Models)*
    - *Time Domain (LTI & Non LTI Models)*



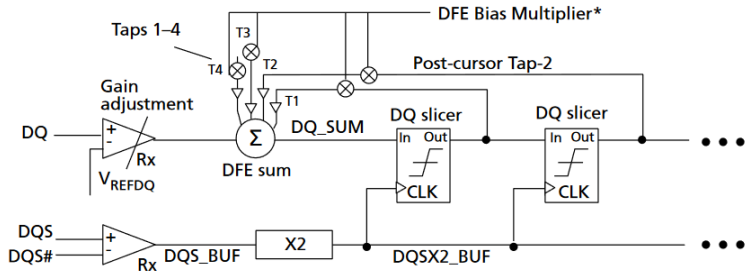
Introduction: DDR5 Overview

- **Improvements over DDR4**
  - Increase Operating Rates: 3200MTS to 8400MTS
    - *2x → 3x improvement in Bandwidth*
  - Address/Command
    - *Clocked on both edges*
    - *Pseudo Open Drain drivers, ODT, and Floating Vref*
    - *Mask based requirements (no longer Setup/Hold)*
  - DQ
    - *RX contains 4 tap DFE*
    - *Controllers can support additional EQ capabilities (FFE, CTLE)*
  - VDD reduced to 1.1V

CA/CS_n Rx Mask



4-Tap DFE



Pictures from Micron product Datasheet: : ddr5_sdram_core.pdf - Rev. B 09/2021 EN

IBIS-AMI and DDR5

- Data Rates are increasing
  - Equalization used in DDR5
- IBIS alone no longer sufficient
  - Equalization blocks must be modeled
- IBIS-AMI Models, then and now
- The journey begins…

SDR/DDR/DDR2
Spice/IBIS

DDR3/DDR4
IBIS

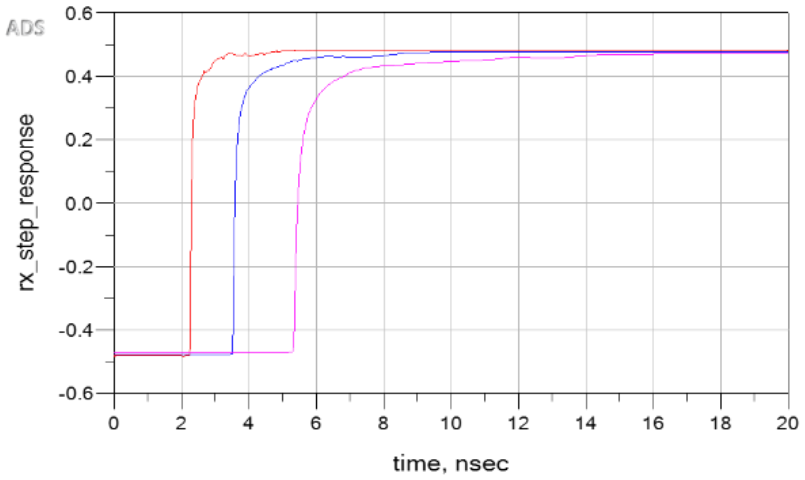
DDR5
IBIS-AMI

New IBIS-AMI Modeling Features: DC Offset: IBIS BIRD 197

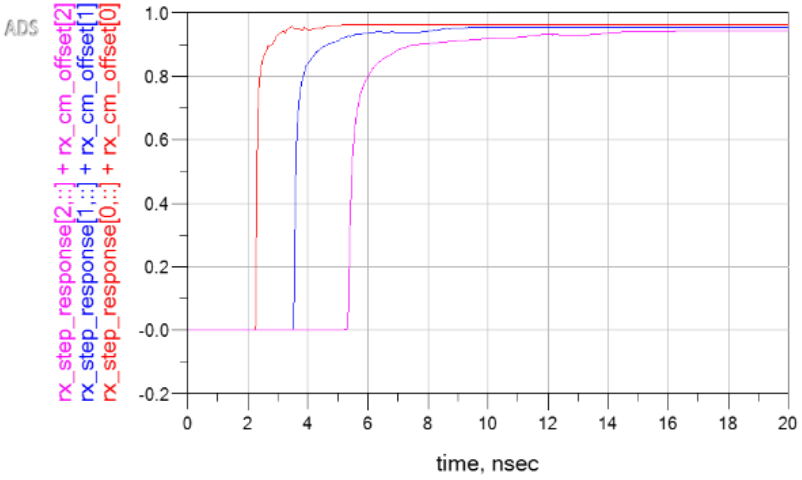
- **IBIS 7.0 and earlier**
  - Original IBIS-AMI meant for Differential Signals
  - Single Ended signals: Common Mode voltage ignored
  - Ignoring Common mode hinders modeling of Voltage Level effects.
    - *Non Linearities*
    - *Saturation*

- **DC Offset**
  - New AMI Reserved Parameter
  - Parameter allows reconstruction of waveform
  - Models support of non-linearities in the Data Path
    - *Saturation*
    - *Gain*
    - *CTLE Response*
    - *DFE filter Response*

Step Response without DC Offset Adjustment



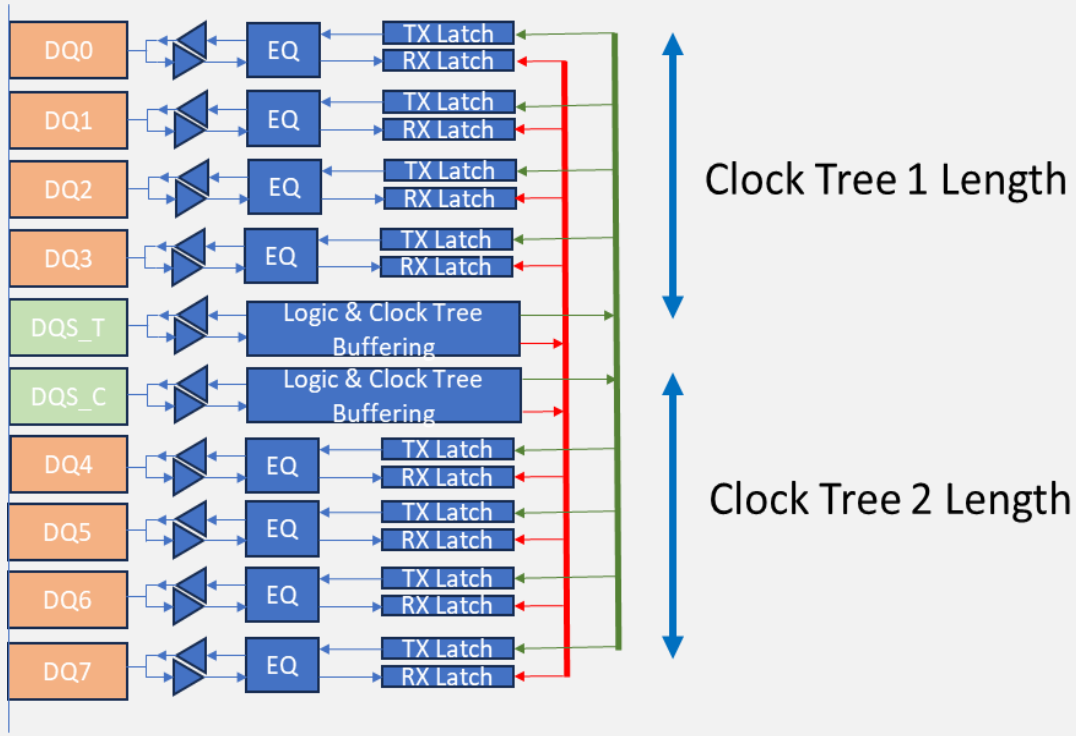
Step Response with DC Offset Adjustment



DLL Function Programmability: IBIS BIRD 207

- **Allows programing IBIS-AMI model functionality based upon IBIS component and Signal Name**
- **Allows capture of skews based upon chip implementation**
  - Allows programming IP based upon IC utilization
- **Capability Enhances**
  - Per bit clock delay: More accurate clock distribution skew definition
  - Improved DFE clocking and Data capture
- **Implementation**
  - IBIS-AMI Reserved Keyword

```
(Component_Name (Usage In) (Type String) (Value "placeholder")
   (Description "The name of the instantiated IBIS Component")
)
(Signal_Name (Usage In) (Type String) (Value "placeholder")
   (Description "The name of the instantiated IBIS Pin's
   signal_name sub-parameter")
)
```



Clock distribution (Red) vs DQ bit position (Green)

Clock-Data Pin Relationship: IBIS BIRD 208

- **DDR interfaces utilize multiple DQS/DQ groups**
- **Feature defines specific DQS/CK to DQ/Address groups**
  - Allows Multi-Byte simulation with correct Clock/Data information
- **Implementation**
  - IBIS-AMI Reserved Keyword
  - Defines the Clock pin (CK, DQS) and an associated Address/DQ bit

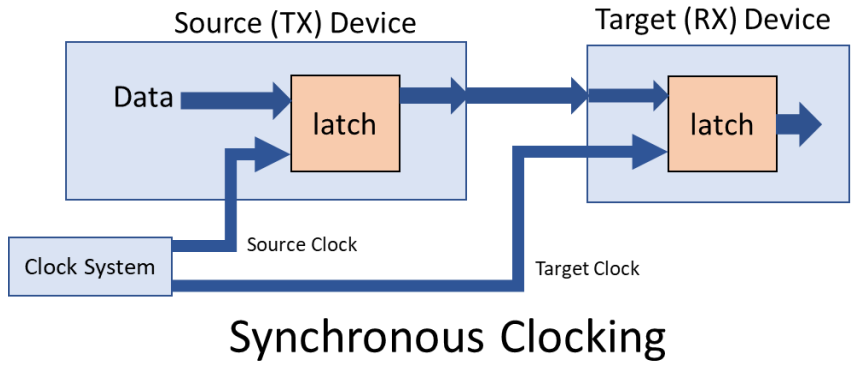
[Clock Pins]	clocked_pins	relationship
A1	B1	Unspecified | Data pin B1 uses clock information from Pin A1
A2	B2	Unspecified | Data pin B2 uses clock information from Pin A2
A3	B3	Unspecified
A3	B4	Unspecified | Pins B3, B4, B5 use clock information from A3
A3	B5	Unspecified | case-sensitive entry

Memory Clocking Methods

Clocks used transfer information between sets of Registers

2 Prevalent Clocking Schemes

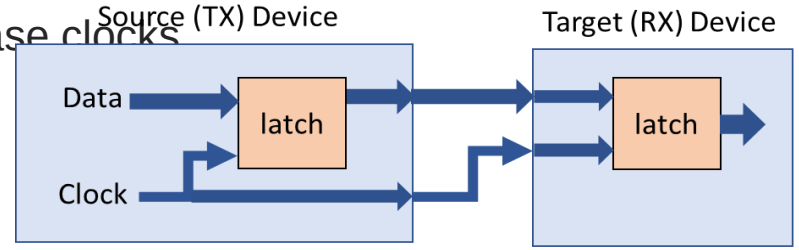
- Synchronous Clocking
- Source Synchronous Clocking



Synchronous Clocking

Synchronous Clocking

- Clock source drives data source and target devices with individual in-phase clocks



Source Synchronous Clocking

Source Synchronous Clocking

- Also Called Clock Forwarding
- Source device drives both Data and Clock to target device

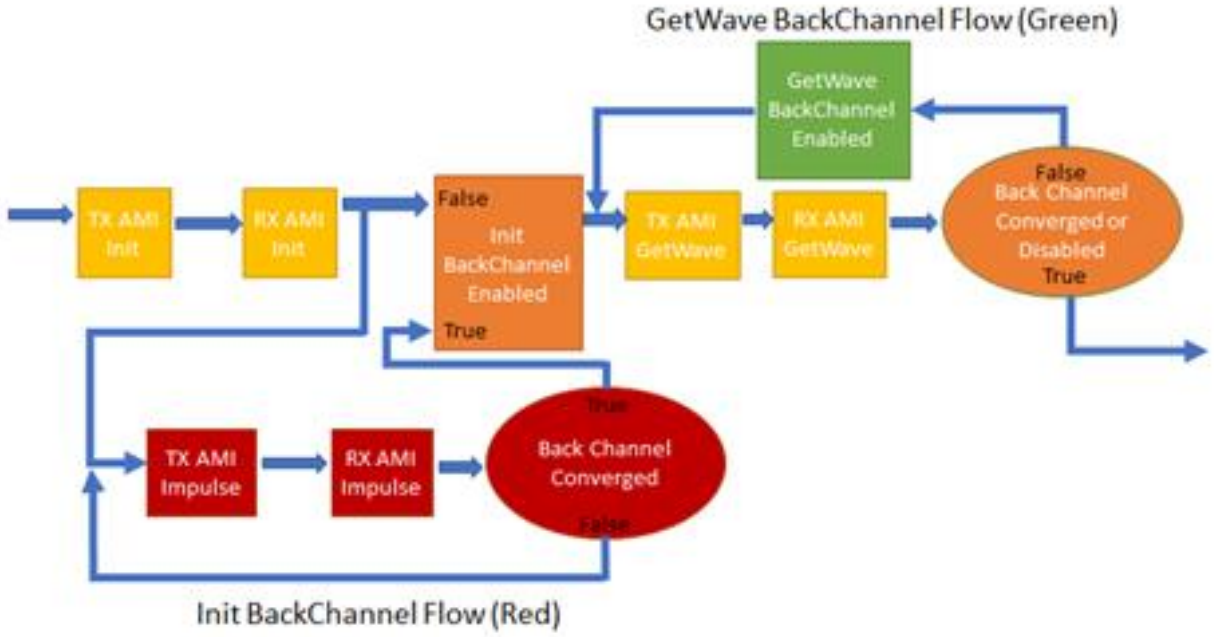
Clock Forwarding Flow: IBIS Bird 209

- Serial interfaces
  - Embed clock in the data stream between devices, thus IBIS-AMI models have only 1 input or Output
  - RX model uses a CDR (Clock Data Recovery) circuit to capture local clock at receiver.
  - Supported by IBIS-AMI as of IBIS Version 5.0
- DDR interfaces
  - Use Source Synchronous (Clock Forwarded) interfaces
  - Requires IBIS-AMI Model to support two inputs (Clock and Data)
  - Unsupported capability before IBIS version 7.1

- **Implementation**
  - Reserved Parameter: RX_Use_Clock_Input
    - *Informs simulator to utilize clock data from Clock_RX_AMI_GetWave and provide it to the Data_RX_AMI_GetWave function*
- **Advantages**
  - Models have access to the true External clock information
  - Clock Position, Slew rate, non-linearities
  - Can model Phase shifts between Clock and Data
  - More accurate DFE analysis
  - Supports Training

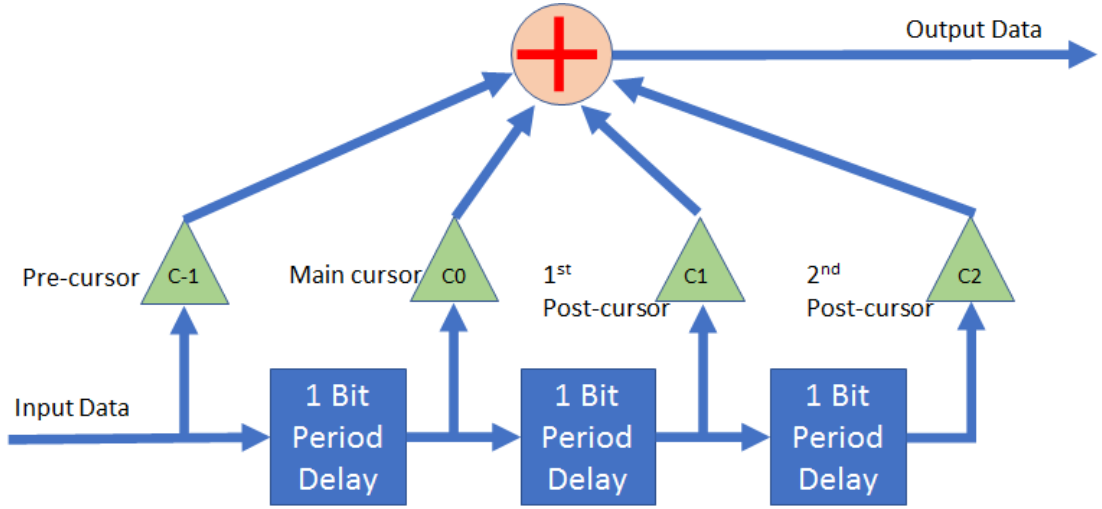
Statistical Back Channel: IBIS BIRD 215

- **Back Channel is a model and simulator capability that allows optimization of both the RX and TX model equalization**
- **BIRD 215 Extends Back Channel operation to Statistical analysis**
- **For DDR, the controller trains the Memory TX and RX remotely**
- **Training Metrics: Eye Height, Eye Width, Eye Area all at a specific BER**
- **New IBIS-AMI Keywords:**
  - AMI_Impulse
    - *TX & RX*
    - *Variable iterated until channel settings converged*
  - BCI_Training_Model
    - *Impulse, Getwave, Both*



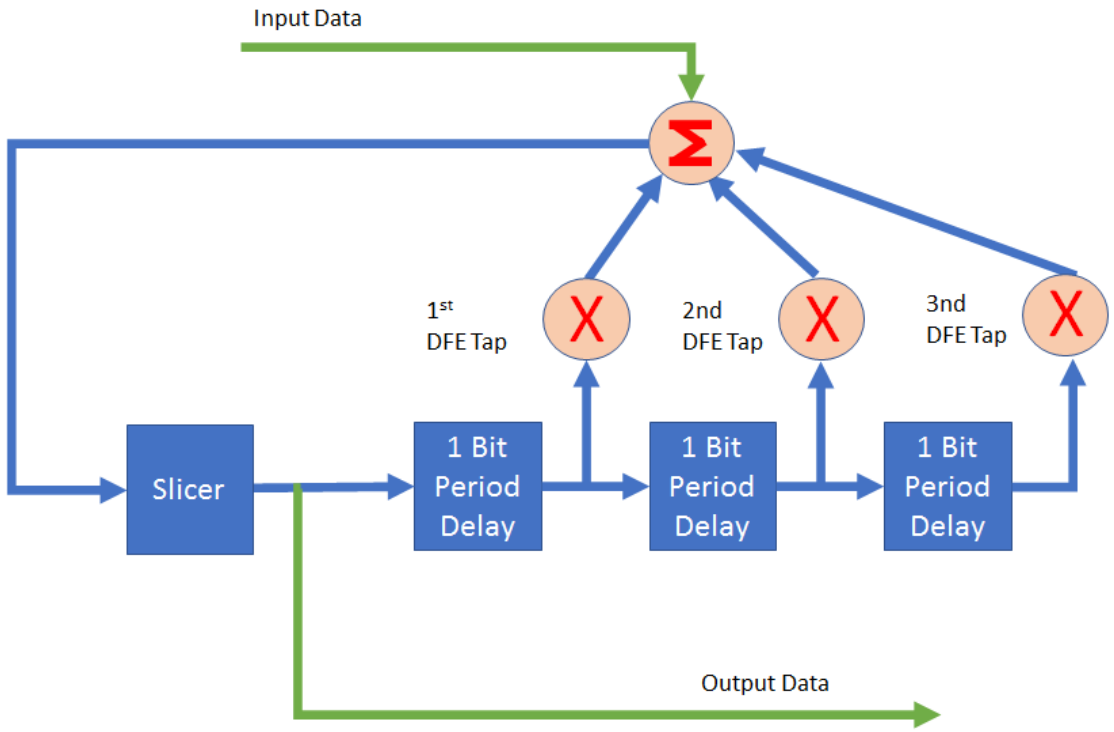
DDR5 Equalization: TX FFE

- **DDR5 Memory will not contain TX FFE**
- **DDR5 Memory Controllers are expected to have FFE**
- **TX FFE Reduces ISI contribution at the Receiver device**
  - Helps Maximize EYE characteristics for Memory Writes
- **Figure depicts 4 TAP FFE**



DDR5 Equalization: RX DFE

- **DDR5 Memory will use RX DFE for Writes**
- **DDR5 Memory Controllers will use RX DFE for Reads**
- **DFE is defined as 4 Taps**
- **Rational For inclusion**
  - Higher bandwidth memory increases ISI on signals
  - Settings set by Memory Controller
    - *Defined by Simulation*
    - *Memory Training*
- **Figure depicts 3 TAP DFE**

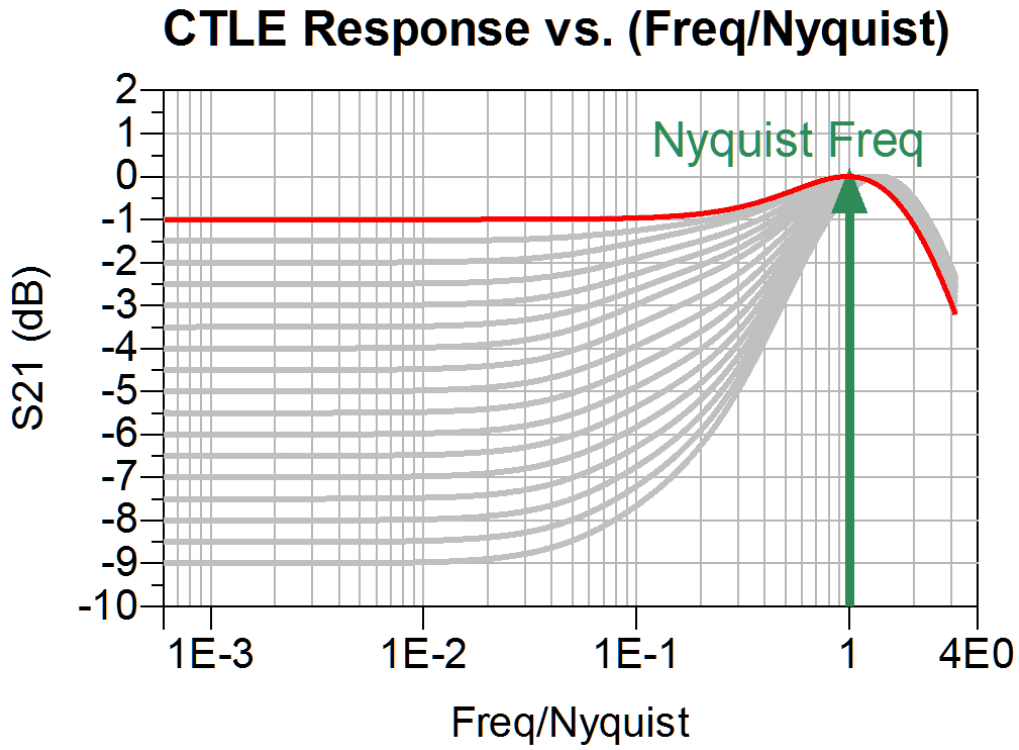


RX CTLE: Why Not Included

- Used to boost High Frequency Spectrum of a signal at the receiver
- CTLE most effective on Higher Loss Channels
- Memory Channels at 4800MTS are generally short (~5 inches) so loss is not the dominant factor
- As speeds increase to 8000MTS, CTLE's may become more useful

- DDR5 specification makes no mention about Memory Controller equalization type. Thus, CTLE's in Memory Controllers may be seen in future DDR5 implementations

- Figure depicts a representative CTLE transfer function.



Summary

- **Before the inclusion of the new capabilities of:**
  - DC Offset, DLL Function Programmability, Clock-Data Pin Relationship, and Clock Forwarding BIRDs, Accurate modeling of the CK/DQS to Command_Address/DQ relationship was impossible.
  - In DDR4, DQS/DQ variations could not be simulated, thereby requiring a guard banded EYE mask to account for skews and non-linear effects.
  - DDR5 speeds require more precision in the analysis
  - These new features along with improved Equalization capabilities in the devices provide the Improvement for next generation designs.

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Thank you

QUESTIONS?