

Add Support of Transient Analysis in SPIM: Update

SPIM = Streamlined Power Integrity Model

Kinger Cai (Arm)

Chi-te Chen (Intel)

Kar Leong Lee (AMD)

Zhiping Yang

Ji Zheng (Aurora-system)



Hybrid IBIS Summit
DesignCon 2025
Santa Clara, CA
January 31, 2025



Speaker

Kinger Cai

Sr. Principal Engineer, Arm

Kinger.Cai@Arm.com



Kinger is Sr. PE driving platform electrical arch. design & val., and industry Power & Signal Integrity standards & EDA tools evolution, in Solution Engineering Group in Arm.

Kinger was a Principal Engineer/Director, in Client Computing Group in Intel, where he led cross-functional teams in driving AI PC coherent architecture strategies across mobile & client platforms and overseen design & sign-off of numerous SoCs spanning media, mobile, client, discrete GPU, & CPU servers.

Kinger earned his Ph. D from Shanghai Jiao Tong University in 2001 and MBA degree from W.P. Carey business school in ASU in 2008.

Kinger has been focusing on signal & power integrity domains for 20+ years.

Kinger holds 14 granted patents, and published 30+ papers.



SPIM Status Quo & Expansion

- Supports in BIRD223.1, approved in [Nov. 2023](#)
 - AC impedance, with [SPIM Touchstone File] and [SPIM Target]
 - DC analysis, with [SPIM Rnetwork File], [SPIM Current] and [SPIM Voltage List]
- Add Support for Transient analysis
 - [Strongly desired by some PI designers, though it is indeed nice to have](#)
 - [“Add \[SPIM **icct** File\], and its generation & application”, is updated to](#)
 - [“Add \[SPIM Transient Current File\], and its generation & application”](#)
 - [The existing \[SPIM Current\] only refers to DC current, for power DC analysis](#)
 - [Add \[SPIM Transient Target\] for Peak-to-Peak noise Vpp, Vmin and Vmax](#)

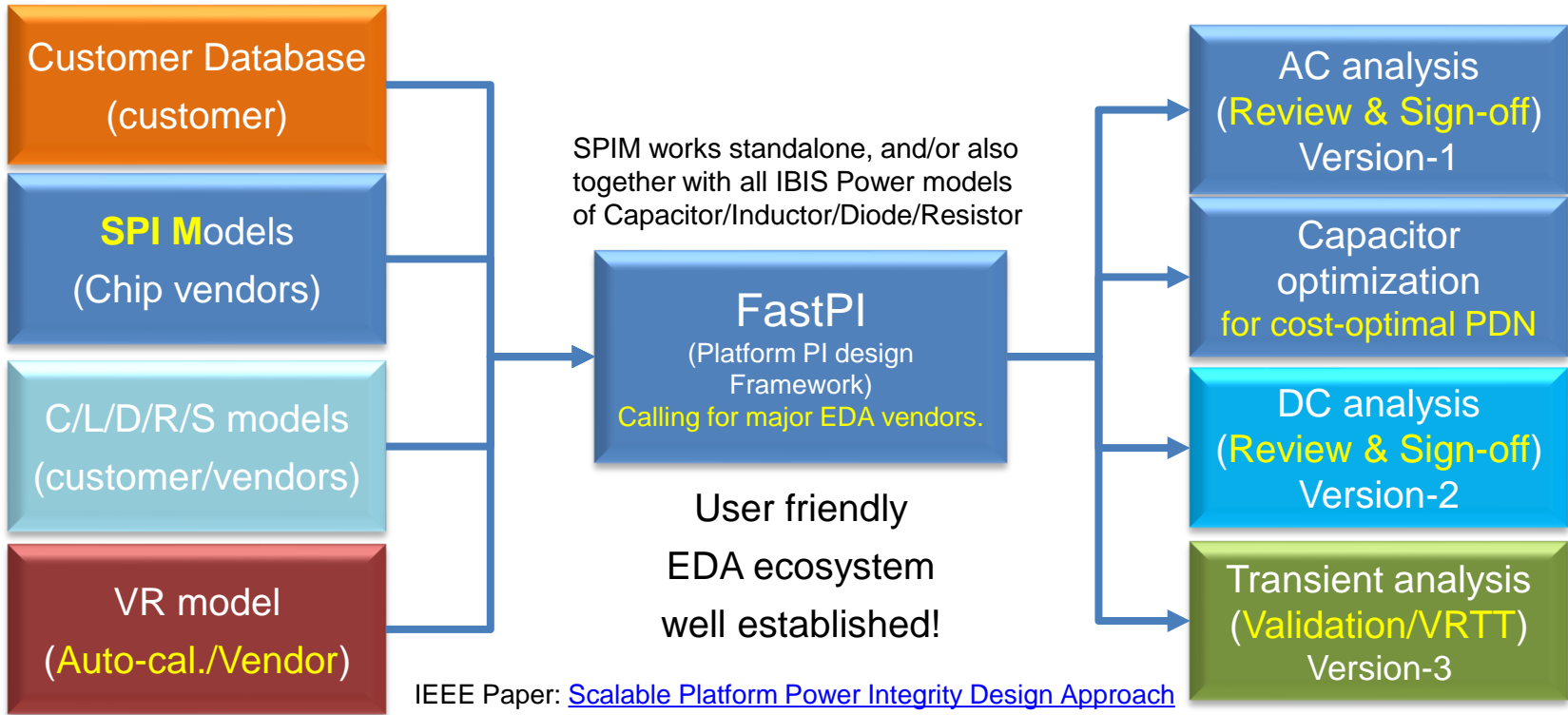
[SPIM](#) - Streamlined Power Integrity Model, approved by IBIS Open Forum in Nov. 2023 , will be included in IBIS 8.0 in 2025

[CVRM](#) - Compact Voltage Regulator Model, published in 2021 IEEE International Joint EMC/SI/PI and EMC Europe Symposium

[FastPI](#) - Fidelity (AC/DC/Transient) Assessment System-level Technology/Tool of Power Integrity



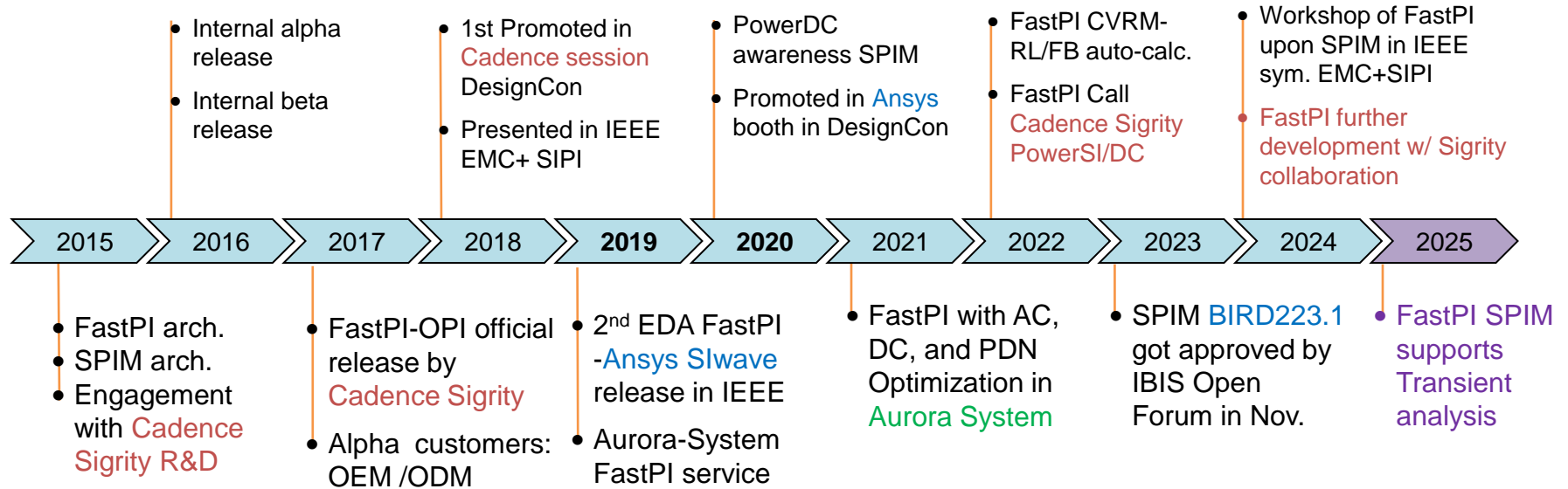
FastPI (Platform PI Arch. with SPIM) Roadmap



IEEE Paper: [Scalable Platform Power Integrity Design Approach with Standard PI Model \(SPIM\) and Unified PI Target \(UPIT\)](#)



FastPI Roadmap with SPIM



Tree Structure of .spim FILE (Defined in BIRD223.1)

.spim FILE

|-- File Header Section

|-- [IBIS Ver]
|-- [Comment Char]
|-- [File Name]
|-- [File Rev]
|-- [Date]
|-- [Source]
|-- [Notes]
|-- [Disclaimer]
|-- [Copyright]

-- [Device SPIM]

|-- [Manufacturer]
|-- [Description]

-- [SPIM Rail]

|-- [SPIM Pin Cluster]

|-- [End SPIM Pin Cluster]

-- [SPIM Port List]

|-- [End SPIM Port List]

-- [SPIM Touchstone File]

|-- [SPIM Stimulus]

|-- [End SPIM Stimulus]

-- [SPIM Target]

|-- [SPIM Observation Port]

|-- [End SPIM Target]

-- [End SPIM Touchstone File]

-- [SPIM Rnetwork File]

|-- [SPIM Current]

|-- [End SPIM Current]

-- [SPIM Voltage List]

|-- [End SPIM Voltage List]

-- [End SPIM Rnetwork File]

-- [End SPIM Rail]

-- [End Device SPIM]

-- [End]



Insert new keywords.



Example .spim FILE -Supports Transient Analysis

```
|
|*****
|Information for Transient analysis
|*****
|
[SPIM Transient Current File]
| File_name           Time_Delay   Repeat_time
Intel_CPU_VCC1_i-t.txt 0.0         0.0
|
[SPIM Transient Target]
[SPIM Observation Port] OB_Sense
| Vpp      Vmin      Vmax
  NA       0.600    1.400
|
[End SPIM Transient Target]
|
[End SPIM Transient Current File]
```

Intel_CPU_VCC1_i-t.txt

*time (second)	Current(A)
0.00000E+00	2
100.000E-09	2
105.000E-09	10
1500.00E-09	10
1505.00E-09	2
3000.00E-09	2
....

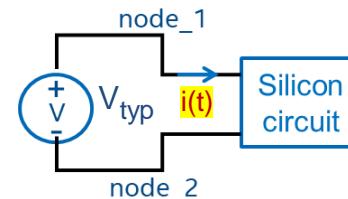
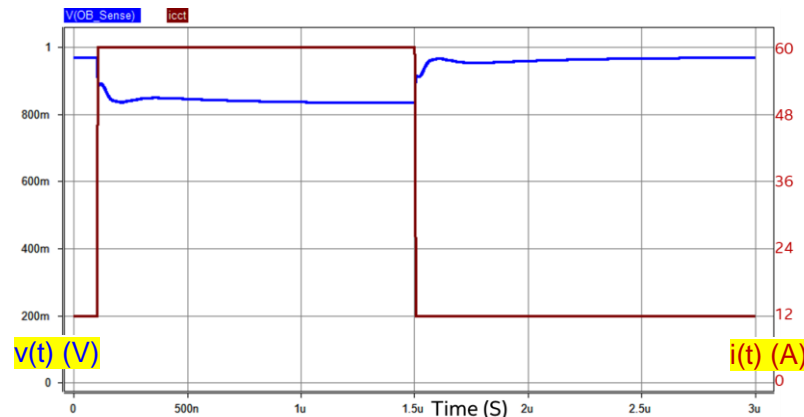


Fig.1 $i(t)$ generation



SPIM Transient Analysis Setup

SOC_CPU_VCC1_i-t.txt

*time (second)	Current(A)
0.00000E+00	2
100.000E-09	2
105.000E-09	10
1500.00E-09	10
1505.00E-09	2
3000.00E-09	2
...	
...	

```
[SPIM Stimulus]
|OB_Stimulus Weighting
OB_Stimulus_1 0.20
OB_Stimulus_2 0.10
OB_Stimulus_3 0.05
OB_Stimulus_4 0.05
OB_Stimulus_5 0.20
OB_Stimulus_6 0.05
OB_Stimulus_7 0.05
OB_Stimulus_8 0.30
[End SPIM Stimulus]
```

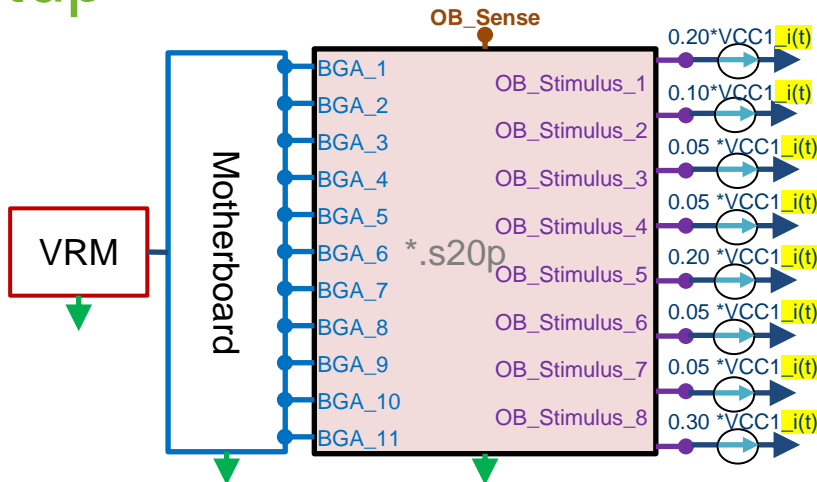


Illustration with the 1st order setup

- i(t) profile under typical voltage directly at circuit node is shown in Fig.1.
- i(t) might specify time delay or repeat time, with default values of 0.
- In Power Integrity transient simulation with an actual power delivery network (PDN), the i(t) profile shall be connected as shown by Fig.3 through G element with the 2nd Polynomial function for accuracy, other than the 1st order connection as shown in Fig. 2 for efficient analysis.

* For example,
 *.SUBCKT VCC1_i-t node1 node2 V_{typ}='1.0'
 *Gpoly node1 node2 POLY(2) node1 node2 p n 0 0 0 0 '1/V_{typ}'
 ****VCCS i12 = 0+0*V₁₂+0*V_{pn}+0*V₁₂*V₁₂+1/V_{typ}*V₁₂

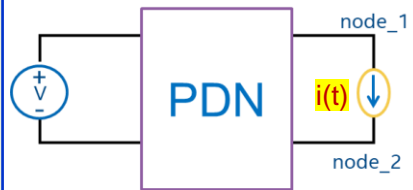


Fig.2 1st order setup

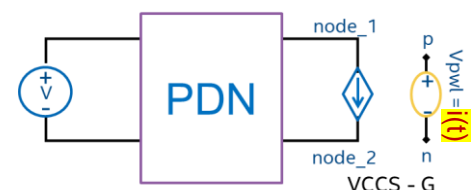


Fig.3 2nd order setup



Next Steps

- Review and revise this proposal through IBIS-ATM
 - Obtain EDA vendors to support Transient Analysis in SPIM
 - Obtain chip vendors to support Transient Analysis in SPIM
 - Obtain platform designers to support Transient Analysis in SPIM
- Submit BIRD of “Add Support of Transient Analysis in SPIM”
- Get approval of the BIRD of the same in IBIS Open Forum
- Integrate the BIRD of the same into upcoming IBIS Version release



Thank you!

QUESTIONS?

Kinger Cai

E-mail: Kinger.Cai@arm.com

Webpage: [FastPI-SPIM](#)

