

# Verification of ASA-ML using IBIS-AMI

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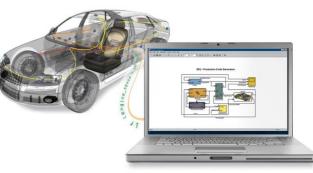
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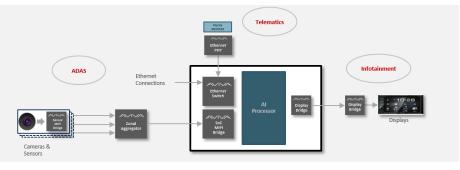


#### **Automotive Networks**









IZC MA.II SC ASE	node3 ASA TRX node2 ASA TRX	Display node4 I <sup>2</sup> C St ASA ASE TRX I <sup>2</sup> C St node5 ASA ASA TRX IZC SLC IZC SLC IZC SLC
ECU IZC MA.i	node1 ASA TRX	TRX ASE ASA ASE TRX ASE Display

- Bidirectional Interfaces:
  - NRZ and PAM4
  - Downstream Baud rates: 8/6/4/2 GHz
  - Downstream Payload rates: 1.8/3.6/6.4/9.7/13 Gbps
  - Upstream Baud rates: 2/4 Ghz
  - Upstream Payload rates: 100M/50M
  - Cabling:

- 50Ω Coax up to 15 meters with Power Delivery
- Synchronization:
  - Half Duplex Precision Time Base (PTB) mechanism enables precise timing synchronization using time stamping, making these parts ideal for use in time sensitive multi-sensor applications.



### Example

#### **AVIVA: Automotive Camera to NVIDIA ORIN System Demo**



#### **Automotive Camera Modules**

- Form factor camera modules
- Include the Sensor + Aviva Ser boards
- Imager examples
  - Omnivision OX03F10 3MP
  - Sony IMX728 8MP

#### Cable support

- Orin Jetson AGX platform
- Camera drivers running on Orin
- > 15m Coax w/ 4 inline connectors
- > 12m STP w/ 4 inline connectors
- Power over Coax and STP supported

## Modeling a Physical Product

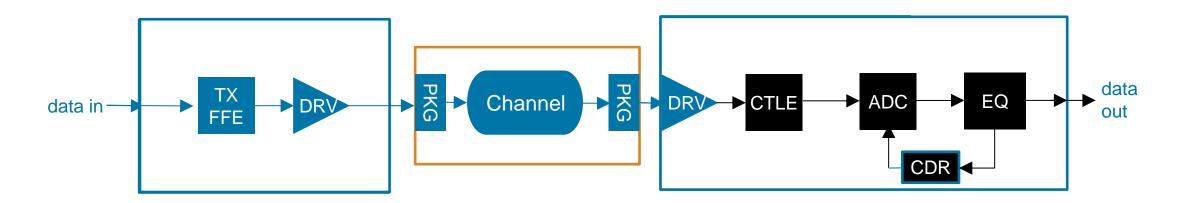
#### **AVIVA** Silicon

- 4-Ports ASA-ML 16Gbps SerDes
- DAC/ADC-based architecture
- Fully Adaptive to channel conditions



#### **IBIS-AMI model using tools from Mathworks**

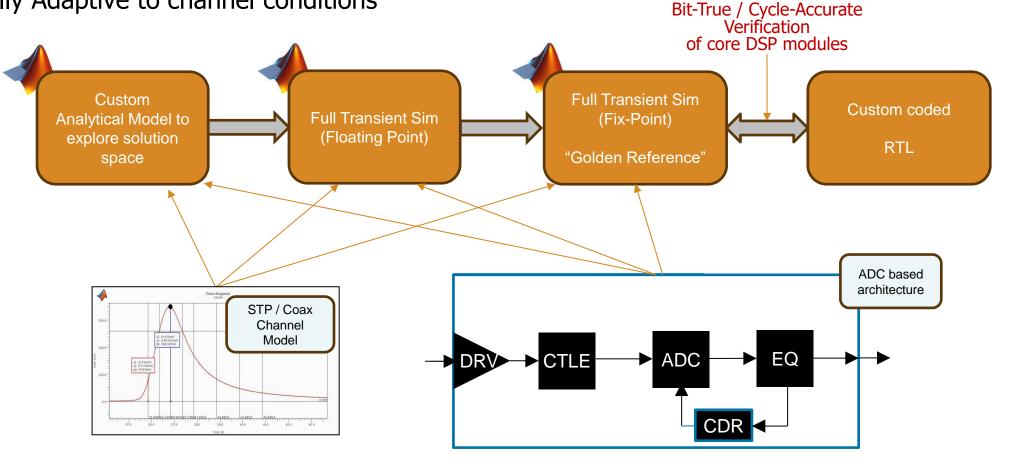
- Import key MATLAB DSP blocks from "Golden Reference"
- Specify CTLE response based on characterized device
- > Validate results against full transient simulations
- Generate and deliver IBIS-AMI model to customers





### **Designing a SerDes Receiver**

High-Speed SerDes for Automotive Connectivity ASA 16Gbps SerDes ADC-based architecture Fully Adaptive to channel conditions



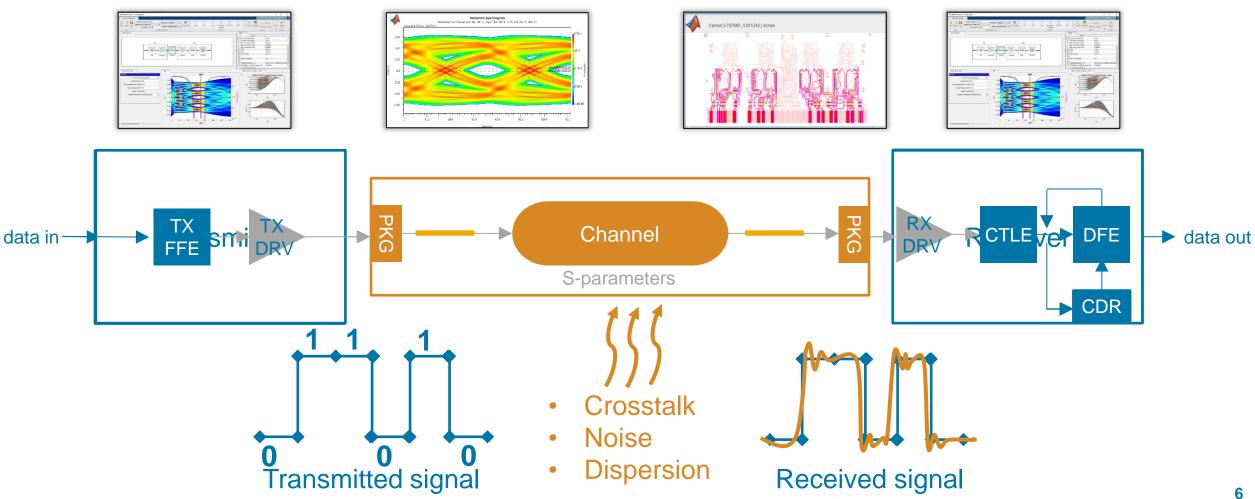


## SerDes and Signal Integrity Analysis with MATLAB®

SerDes Architecture Pre-layout Simulation

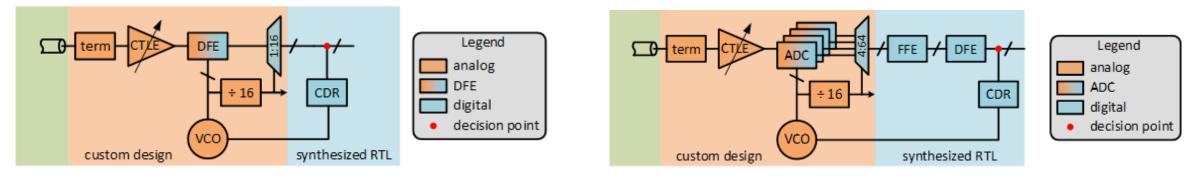
#### Post-layout

#### Model Generation





### **Types of Architecture**



Analog Based SerDes

Smaller Area Lower Power Suitable for high-scale integration in large ASICs ADC Based Digital SerDes

Higher performance Flexible architecture Powerful diagnostics Easier to port to smaller geometries Less susceptible to PVT variations

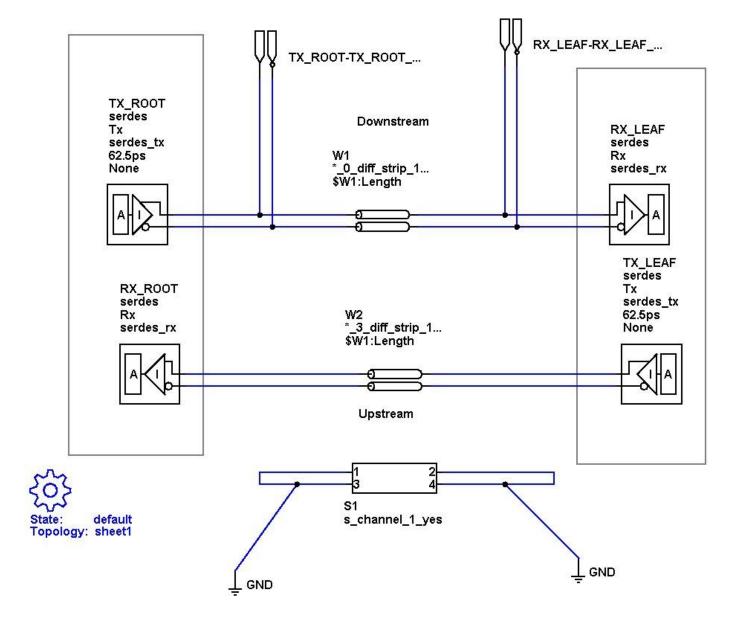


# Signal Integrity Link

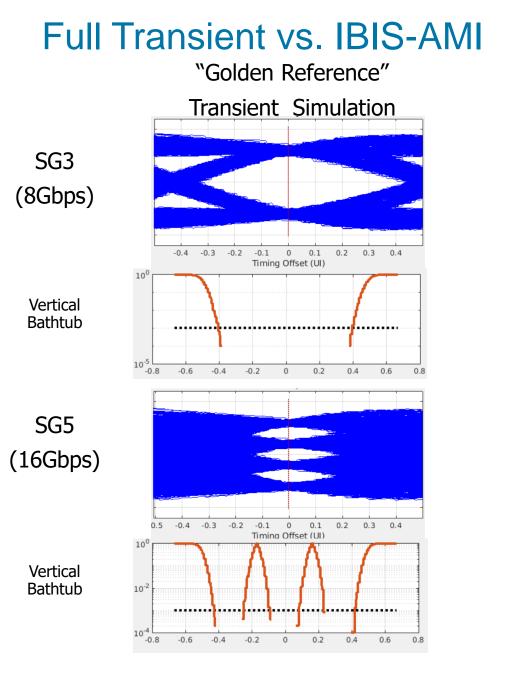
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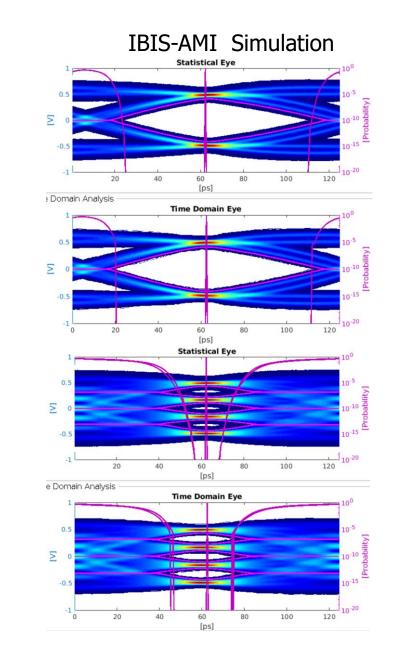


### Signal Integrity setup













### Summary

- Complex architecture can be easily verified for different baud rates
- Time domain simulation to capture time-varying effects and including customization
- Compiling link to IBIS-AMI model to do regression analysis
- Compare results to all standard specification



# Thank you

