S-Parameter Modeling

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Outline

- Background and motivation
- Extracting and simulating an RLC SPICE model
- Extracting 6-port and 8-port models from the SPICE model
- Extracting 6-port and 8-port models using Full-Wave solver
- Simulating the 6-port model correctly
- C_comp
- Questions, comments?
- Future work

Background

- Several presentations in the past pointed out the shortcomings of RLC circuit-based IBIS package modeling mechanisms, highlighting the importance of coupling and loop inductance between power and signal nets
  - https://www.ibis.org/summits/jun05/chen.pdf
  - https://www.ibis.org/summits/oct06b/chitwood.pdf
- The IBIS specification introduced several keywords to address these problems
  - [*** Matrix] keywords in [Define Data] of [Define Package Model] (IBIS v2.0)
  - Support for IBIS-ISS (SPICE) subcircuits and Touchstone S-parameter models was added through the [Interconnect Model] and [EMD Model] keywords (IBIS v7.0 and v7.1)
  - Despite these improvements, “good” models are still hard to come by
- Some of these problems may be traced to the complicated or confusing nature of model extraction and correct choice of referencing in simulations
  - https://www.ibis.org/summits/feb18/dmitriev-zdorov.pdf

Motivation

- Currently the IBIS Interconnect Task Group is working on preparing the next Touchstone (v3.0) specification
- The two major enhancements planned for Touchstone 3 are:
  - Standardized Pole-Residue Representation of Touchstone Data (TSIRD 7.2)
  - Standardized Syntax for Port Mapping (still being drafted)
- The discussions on Port Mapping experienced a significant slow-down, mostly revolving around questions on port referencing and the usage of <u>node0</u> (A_gnd, SPICE node 0, or universal "ground")
  - During these discussions, a few questionable examples were discovered in the [Interconnect Model] and [EMD Model] sections of the IBIS v7.2 specification
- This study is an attempt to answer questions about how to extract S-parameter models with field solvers and how to use them correctly in simulations

Definition of Ports For Circuit Parameters

- Applies to S, Y, Z parameters and others
- A port has two terminals, + and -
- We commonly refer to the negative terminal as the reference
- Voltage is measured between the two terminals of a port
- Current into the positive terminal of a port is equal to the current out of the negative terminal of the same port
- The physical distance between + and – terminals of a port during extraction (measurement or simulation) must be “short” compared to the wavelength of the highest measured frequency
  - Short is often 1/20 the wavelength

Terminology

- We need to use precise and accurate terms when discussing creation and implementation of S-parameter data
  - Port defined in S-parameter creation
  - Port defined in simulation netlist
  - Terminal
  - Node
- Issues involved in creation might be different than issues involved in instantiation in a simulation netlist
- Creation of S parameters is an electromagnetic (EM) field problem
- Simulation of S parameters is a circuit problem
- Be careful in the transfer of data
- S-parameter data is not a model. The model is made in the circuit simulator.

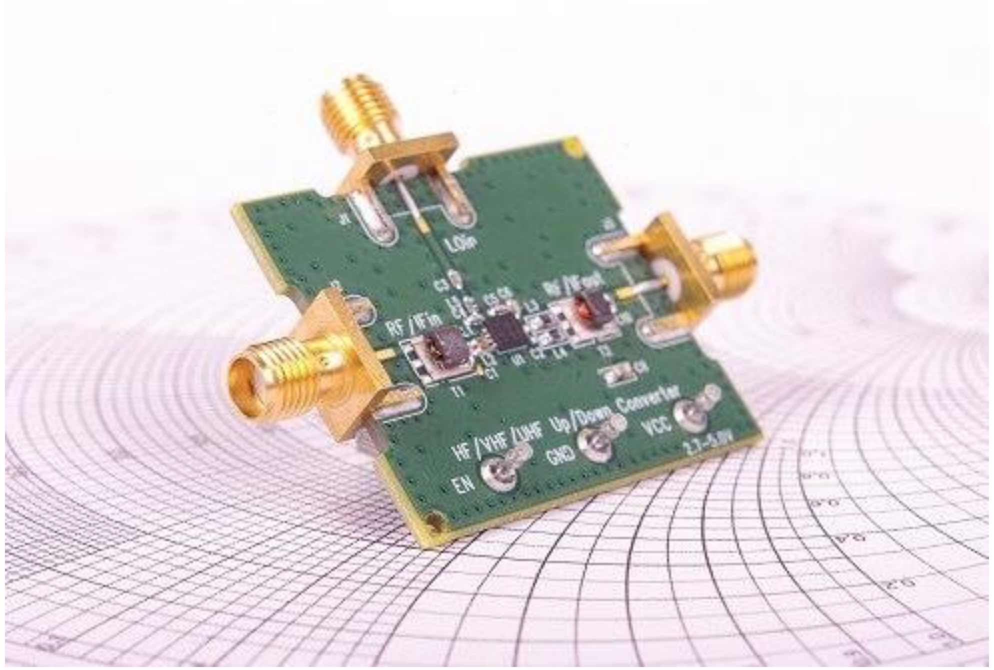
"All models are wrong, but some are useful."

Simplified Ports

- Decades ago, S parameters were measured from relatively simple PCBs or components

- No external circuits between ports of the same S-parameter block

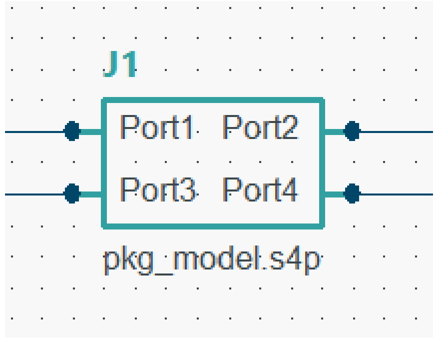
- Thus, a single (positive) terminal was sufficient to represent a port in a schematic



https://www.pcbmay.com/rf-and-microwave-pcb-design-guide/, Jan 2025

Schematic Port Tradition

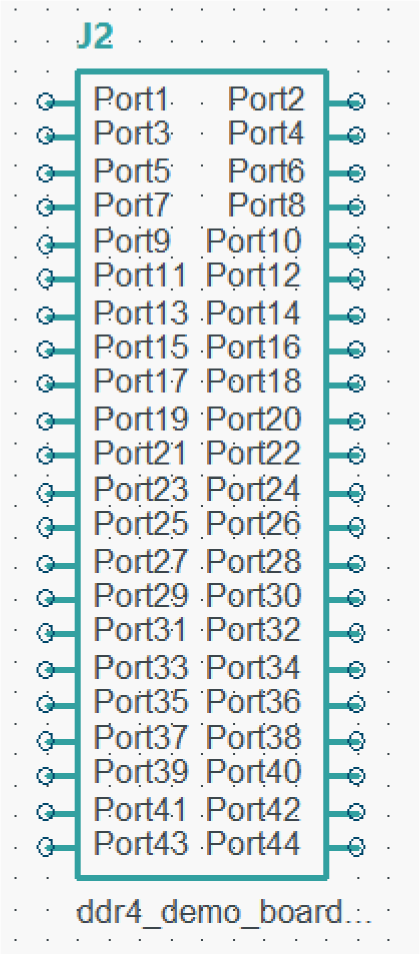
- Now, we end up with many schematic and simulation tools still using one terminal for an S-parameter block with many ports
- This condition is generally usable and correct, but not always
- Only connect circuits between ports of an S-parameter block that have the same, near reference
- Where is the reference terminal connected?
- No reference terminal: the reference must be node0
- One reference terminal: defaults to node0
- negative terminal for each positive terminal: correct and absolutely controllable



Reference Terminals

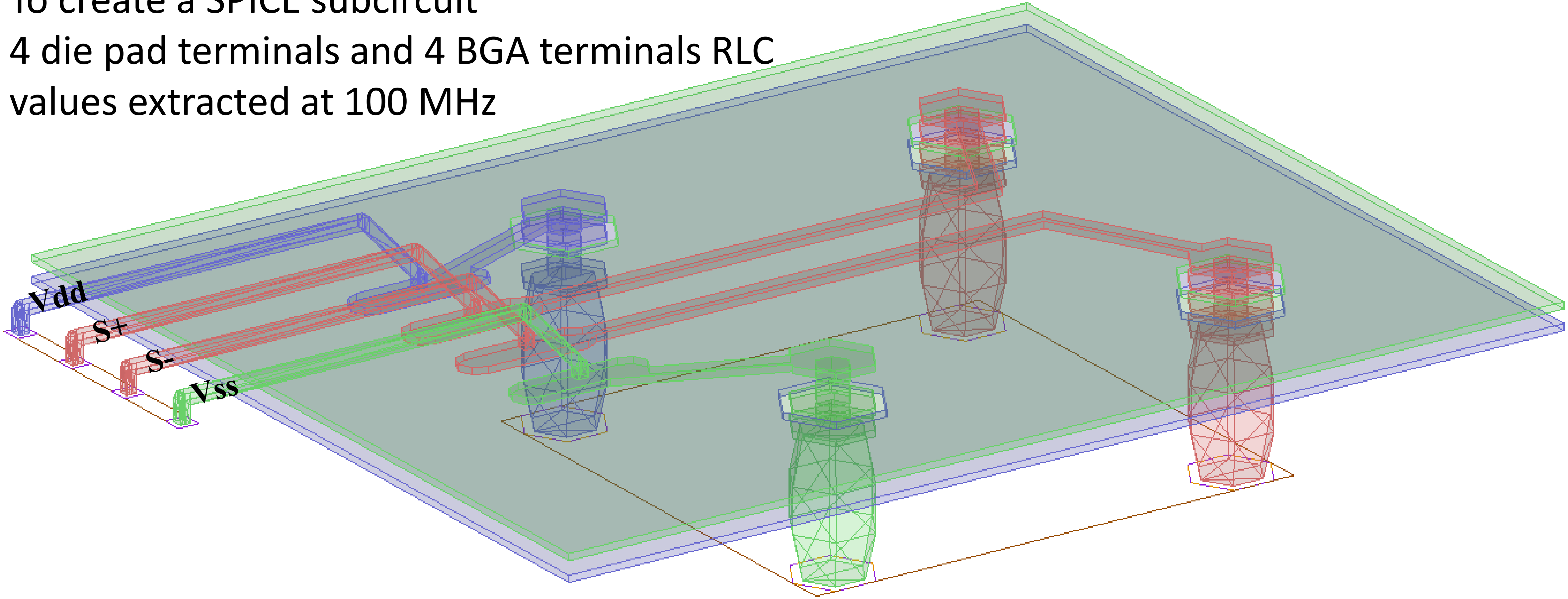
- We should have control of connection to both terminals of each port!

- What does the S-parameter data represent?
- Is a consistent “reference” net available for each signal terminal?
- Do both sides of the measured structure have the same reference?
- Can this method explicitly model the return path between any 2 ports?



Quasi-static Solver Setup

To create a SPICE subcircuit
4 die pad terminals and 4 BGA terminals RLC values extracted at 100 MHz



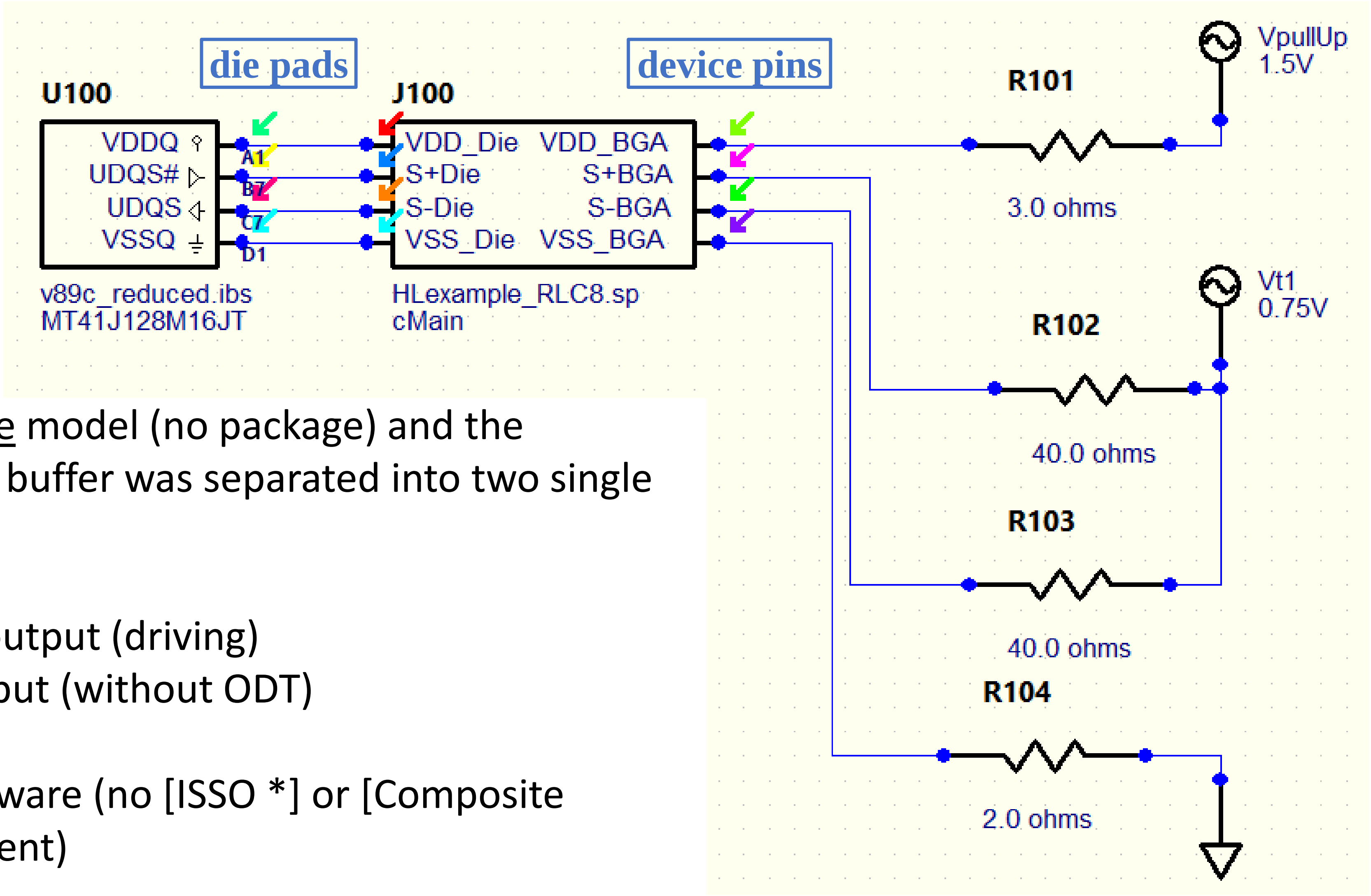
The Extracted SPICE Subcircuit

```
** SPICE Node -1                    Pin     VDD_Die
** SPICE Node -2                    Pin     S+Die
** SPICE Node -3                    Pin     S-Die
** SPICE Node -4                    Pin     VSS_Die
** SPICE Node -5                    Pin     VDD_BGA
** SPICE Node -6                    Pin     S+BGA
** SPICE Node -7                    Pin     S-BGA
** SPICE Node -8                    Pin     VSS_BGA
```

```
.subckt cMain
+ VDD_Die S+Die S-Die VSS_Die VDD_BGA S+BGA S-BGA VSS_BGA
Xsection1
+ VDD_Die S+Die S-Die VSS_Die 9 10 11 12
+ circuitSection
Xsection2
+ 9 10 11 12 13 14 15 16
+ circuitSection
Xsection3
+ 13 14 15 16 17 18 19 20
+ circuitSection
Xsection4
+ 17 18 19 20 21 22 23 24
+ circuitSection
Xsection5
+ 21 22 23 24 25 26 27 28
+ circuitSection
Xend
+ 25 26 27 28 VDD_BGA S+BGA S-BGA VSS_BGA
+ circuitEnd
```

```
.subckt circuitSection
+ 1 2 3 4 5 6 7 8
L1 1 9 2.8006323e-10
L2 2 10 4.0683201e-10
L3 3 11 4.0662683e-10
L4 4 12 2.7627028e-10
K1_2 L1 L2 0.22976021
K1_3 L1 L3 0.31122871
K1_4 L1 L4 0.18981307
K2_3 L2 L3 0.34419621
K2_4 L2 L4 0.3162172
K3_4 L3 L4 0.23400462
R1 9 13 0.019456281
R2 10 14 0.024919517
R3 11 15 0.024919492
R4 12 16 0.017338427
V1 13 5 0
V2 14 6 0
V3 15 7 0
V4 16 8 0
C1_0 1 0 1.792671e-14
C5_0 5 0 1.792671e-14
C1_2 1 2 6.8073378e-15
C5_6 5 6 6.8073378e-15
C1_3 1 3 7.2441612e-15
C5_7 5 7 7.2441612e-15
C1_4 1 4 6.282816e-13
C5_8 5 8 6.282816e-13
C2_0 2 0 1.1742443e-15
C6_0 6 0 1.1742443e-15
C2_3 2 3 7.366555e-16
C6_7 6 7 7.366555e-16
C2_4 2 4 3.0017958e-14
C6_8 6 8 3.0017958e-14
C3_0 3 0 1.1830427e-15
C7_0 7 0 1.1830427e-15
C3_4 3 4 2.9612967e-14
C7_8 7 8 2.9612967e-14
C4_0 4 0 6.9486113e-15
C8_0 8 0 6.9486113e-15
.ends circuitSection
```

Simulating With The RLC SPICE Model In J100

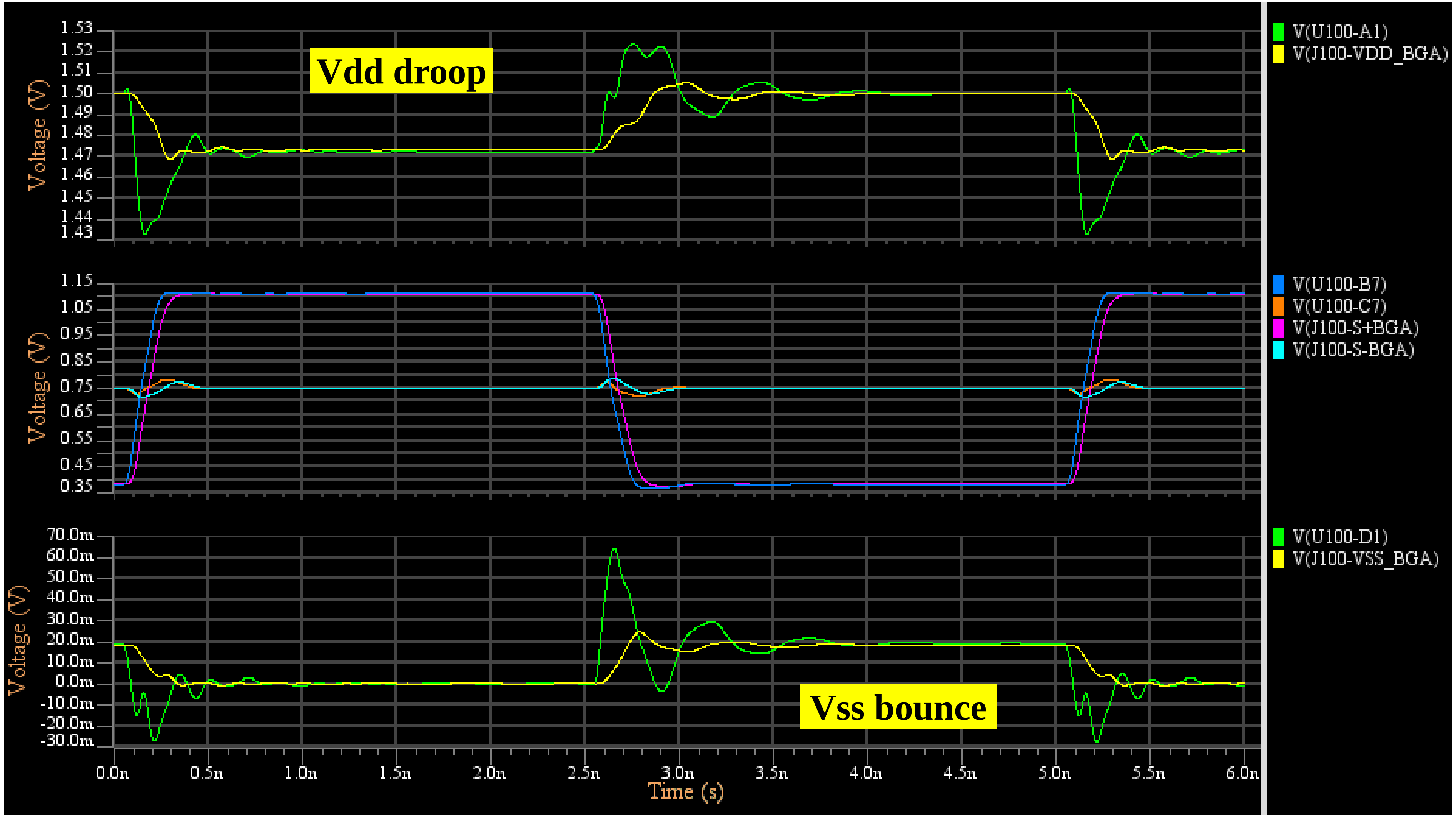


Note that U100 is a bare-die model (no package) and the (originally differential) DQS buffer was separated into two single ended models:

UDQS# (U100.B7) is an output (driving)
UDQS (U100.C7) is an input (without ODT)

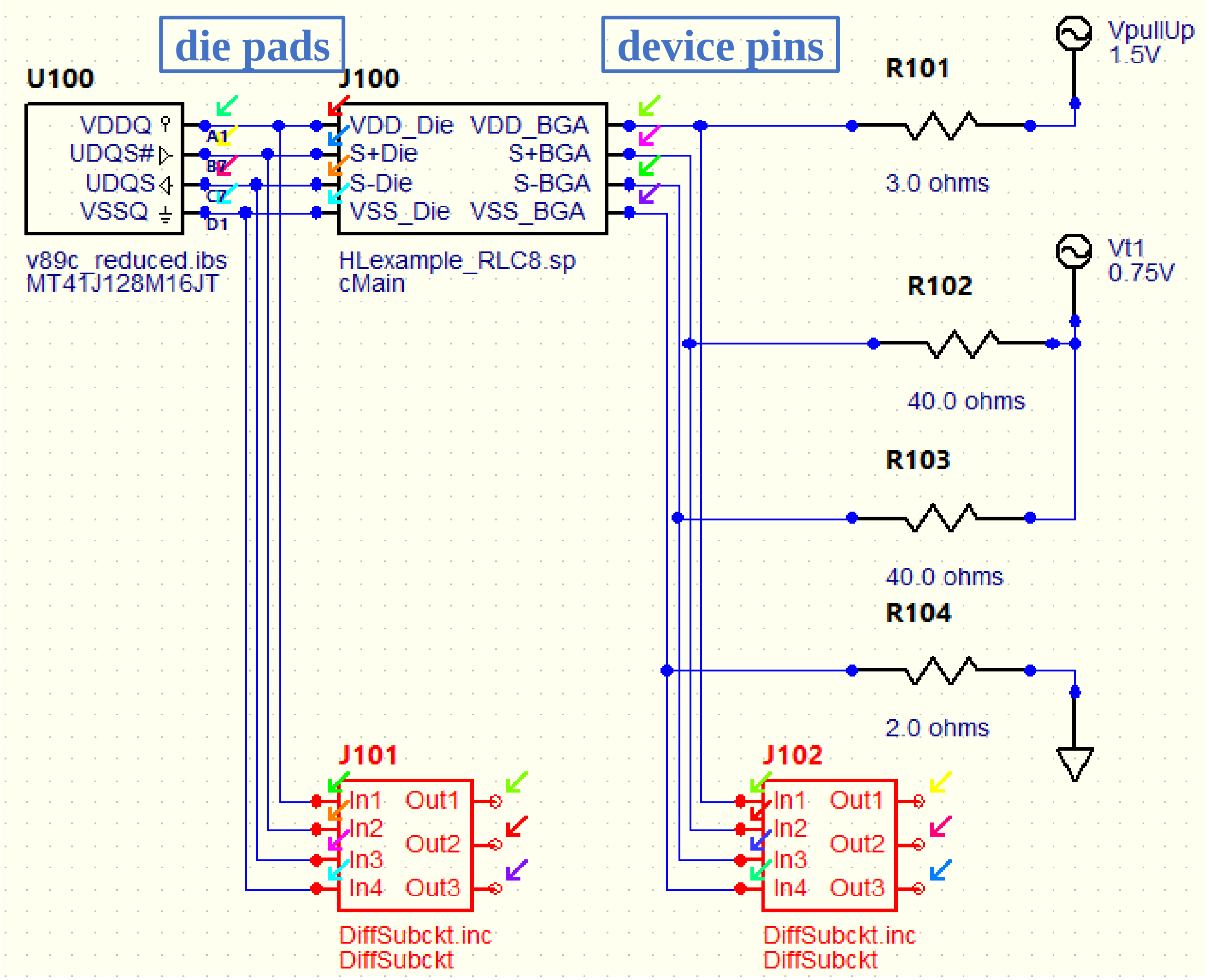
The [Model] is not power aware (no [ISSO *] or [Composite Current] keywords are present)

Node0 Referenced Pad and Pin Waveforms



Can you see what's wrong with these waveforms?

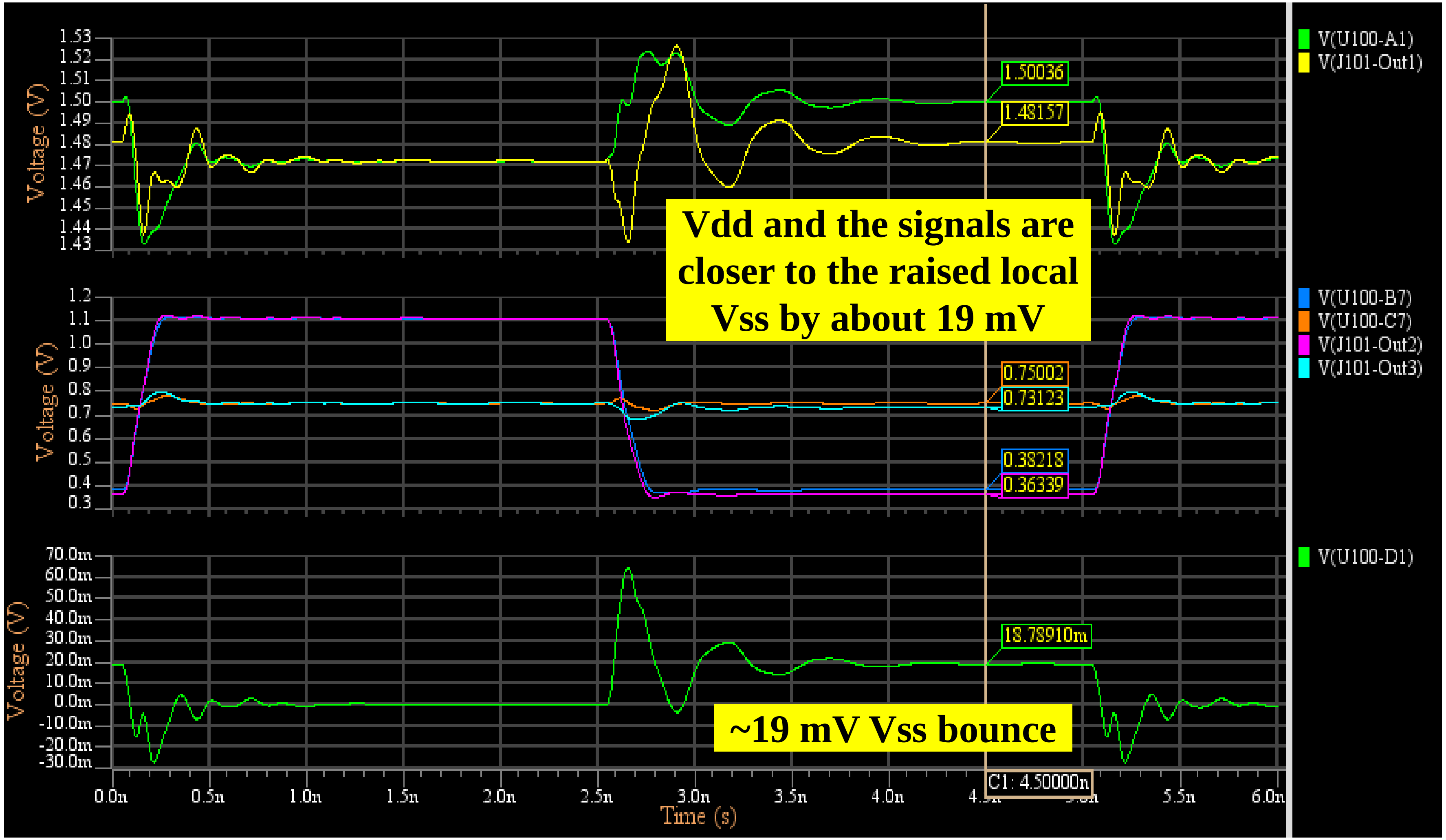
Subcircuits To Help Plotting Waveforms



Connected a SPICE subcircuit to the buffer and package model instances to make it easier to plot locally referenced pad and pin waveforms using their local Vss node

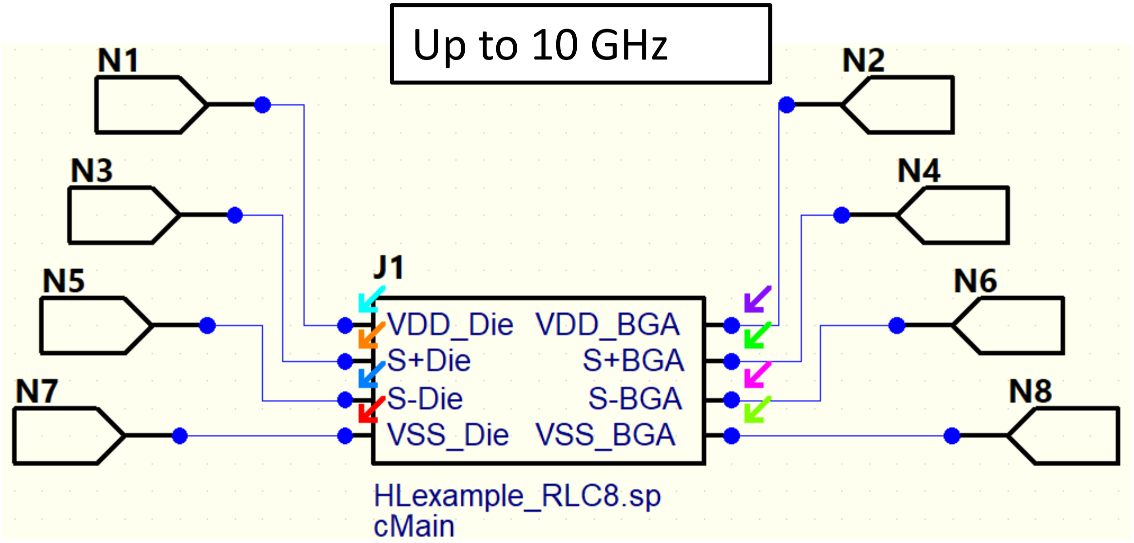
```
.subckt  DiffSubckt  In1  In2  In3  In4  Out1  Out2  Out3

E1  Out1  0  VCVS  In1  In4  1
E2  Out2  0  VCVS  In2  In4  1
E3  Out3  0  VCVS  In3  In4  1

.ends
```

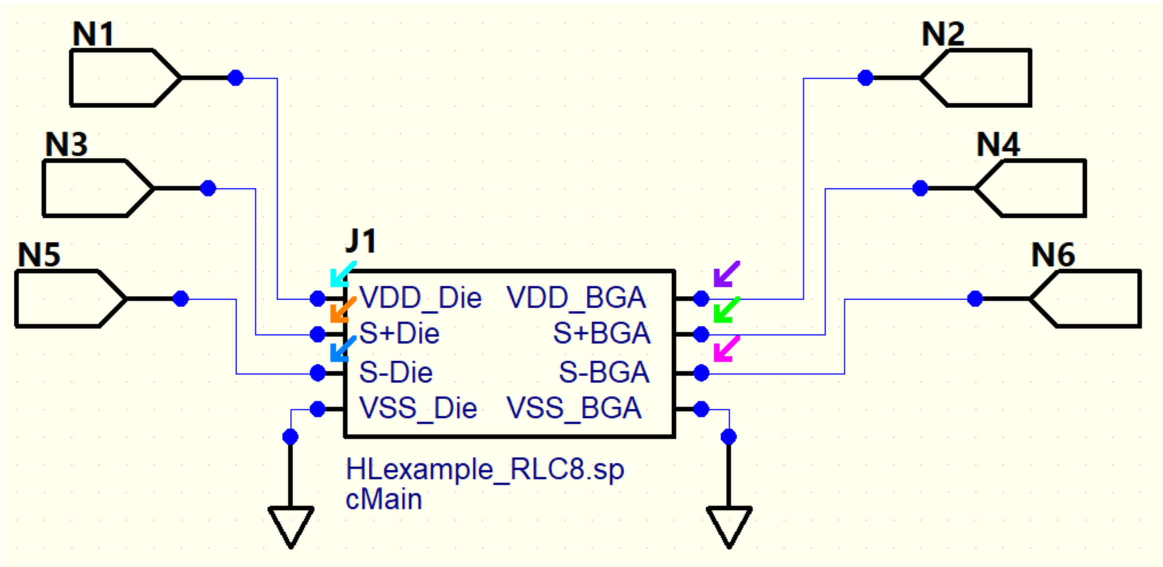
Compare Node0 and Vss-Referenced Waveforms



The node0 referenced waveforms are incorrect when the buffer is driving low because Vss in the buffer rises due to "ground bounce". Consequently, the actual voltages across the buffer's terminals and the transmitted signal are smaller than the voltages measured with respect to node0.

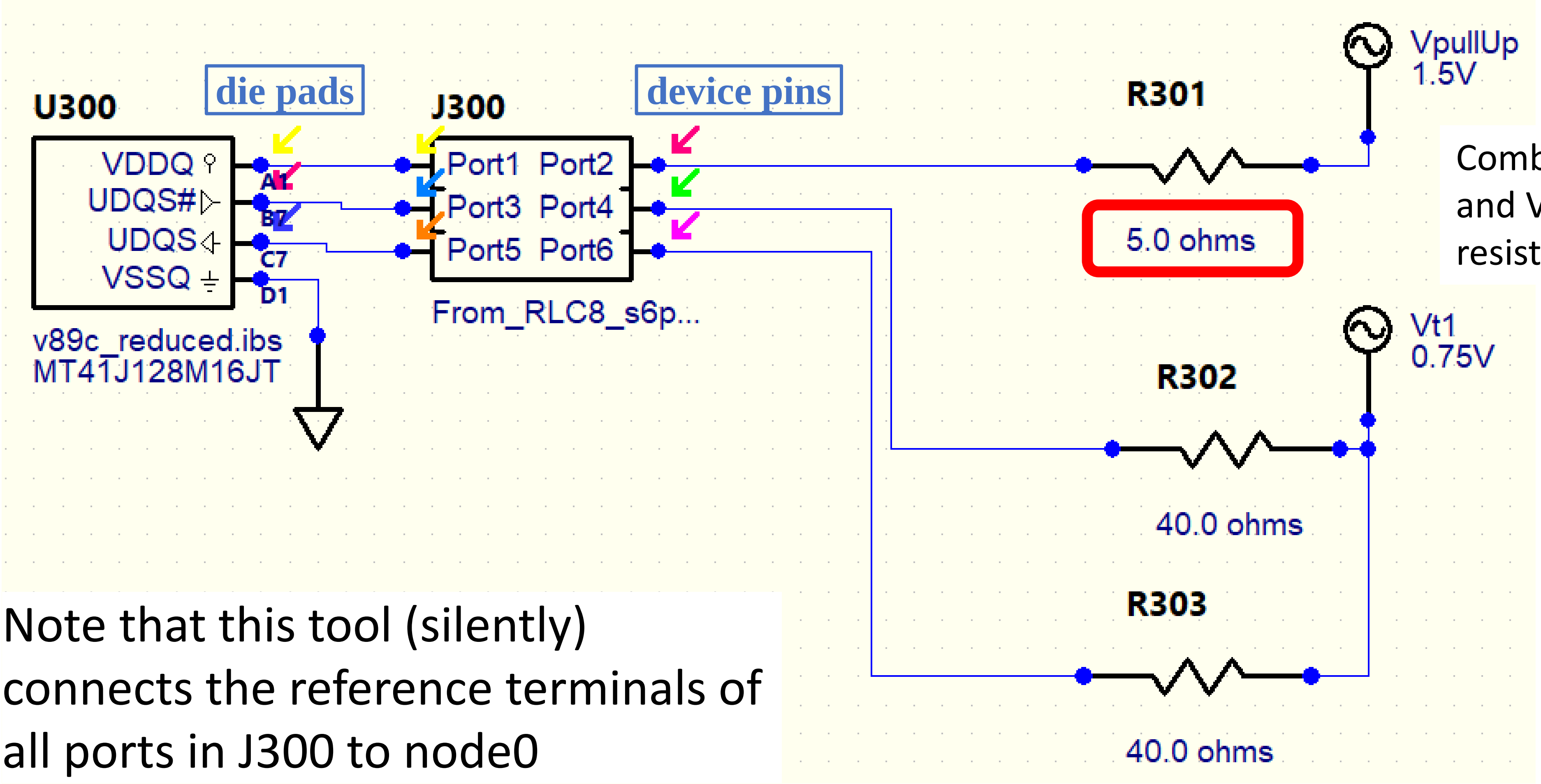
S-Parameter Model From The SPICE Model





This should produce 3 models (RLC, S6P, S8P) with the same electrical behavior.
Which one is correct?
Note that this tool applies an invisible reference connection to node0 for each port symbol.
The 6-port extraction circuit on the right can’t be correct because it shorts the circuit elements between Vss_Die and Vss_BGA (but we will try it anyway).
Or should we extract an s7p model?

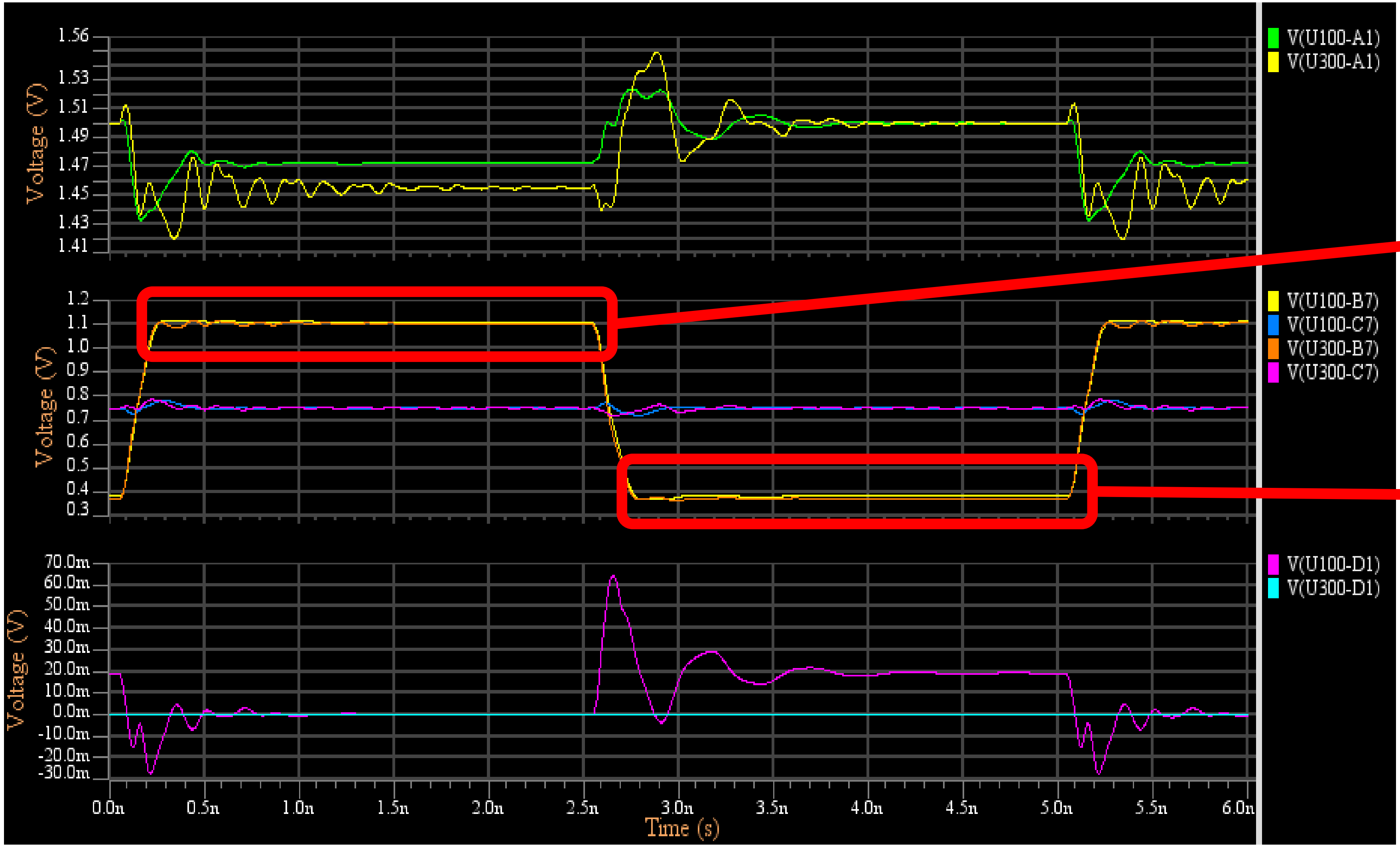
Simulating With The 6-Port Model In J300



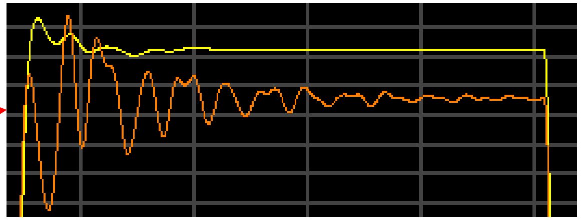
Combined VDD and VSS path resistances

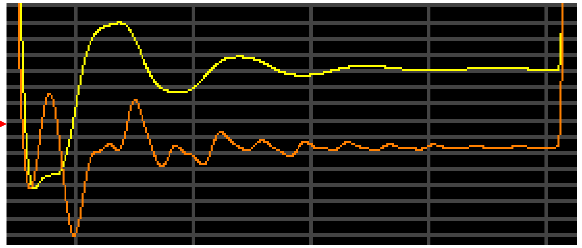
Note that this tool (silently) connects the reference terminals of all ports in J300 to node0

SPICE and 6-Port Model Waveforms

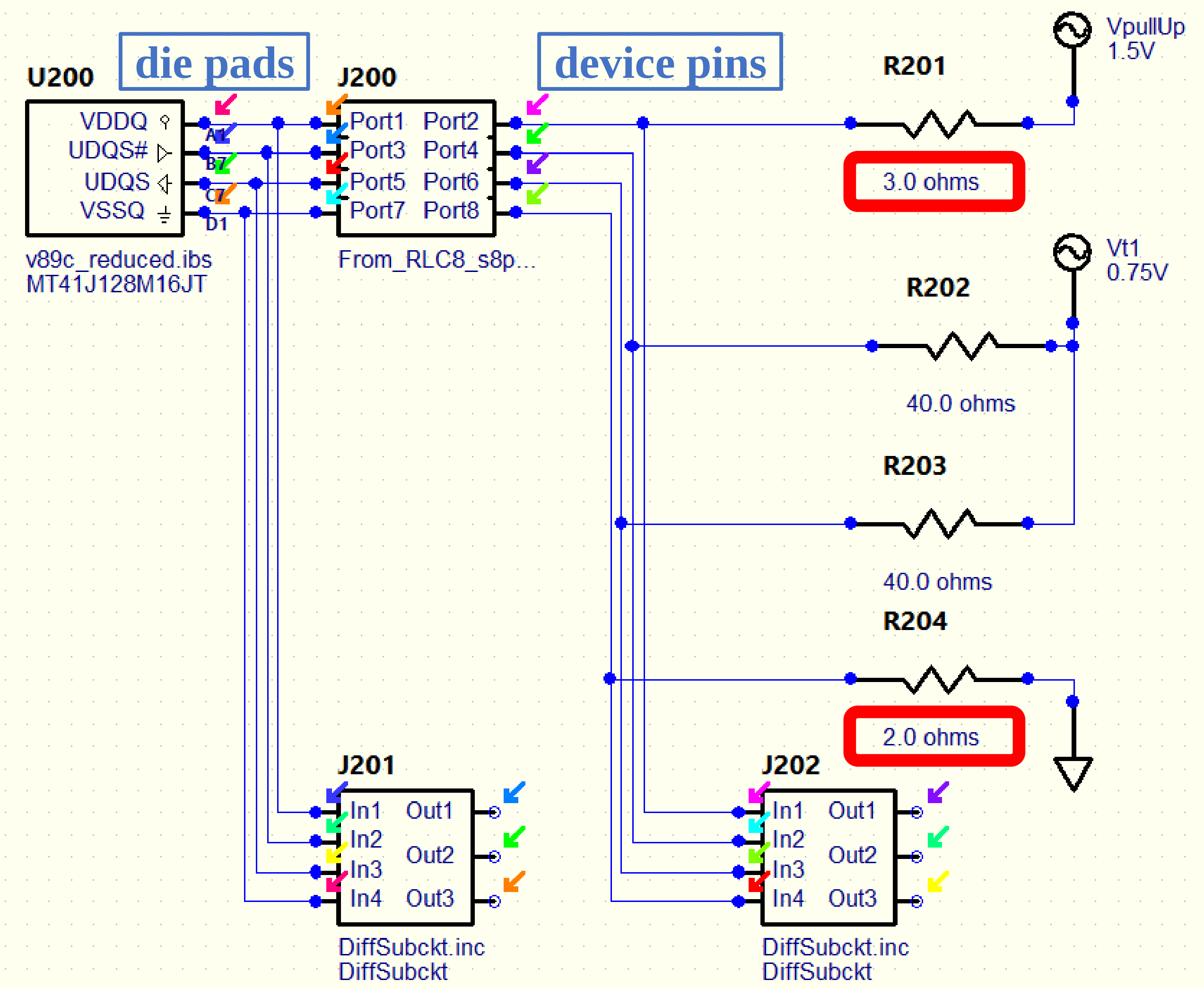


node0-Referenced





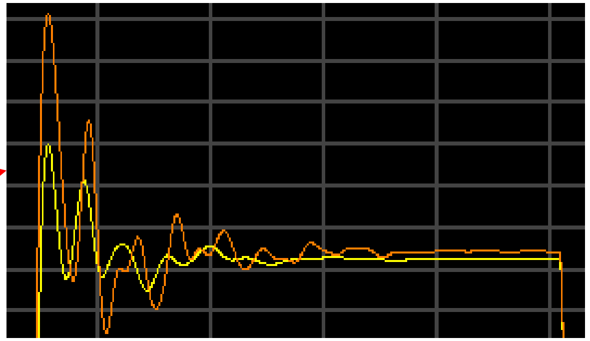
Simulating With The 8-Port Model In J200

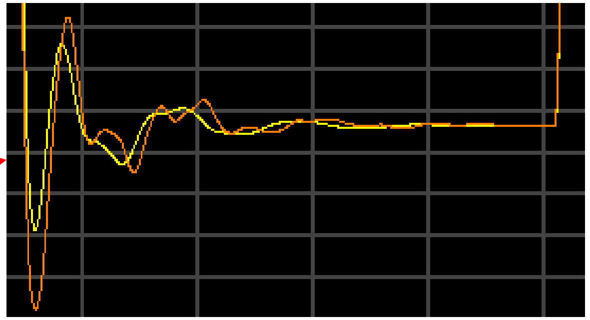


Remember, this tool (silently) connects the reference terminals of all ports in J200 to node0

SPICE and 8-Port Model Waveforms

local Vss referenced





Conclusions On The Previous Slides

- We have seen that even with a “pure” SPICE subcircuit model, the waveforms are only correct when displayed with respect to a local Vss reference node

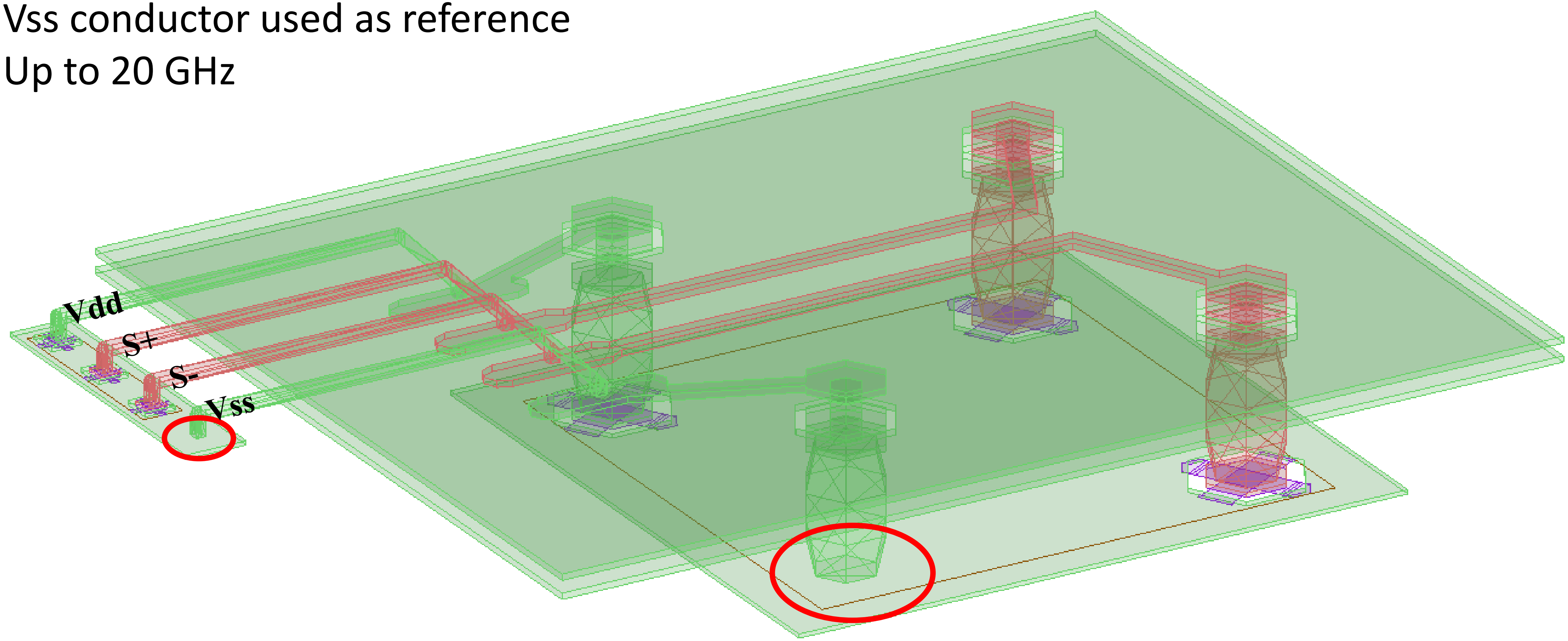
- The Touchstone model extracted from the SPICE subcircuit is only correct if the number of ports equals the number of SPICE terminals
  - Pay attention to how the extraction tool references the ports
  - Use the same (or compatible) referencing scheme when instantiating the model in simulations

- The slight level difference in the 8-port waveforms is probably due to how the simulator transforms frequency-domain S parameters to a time-domain model

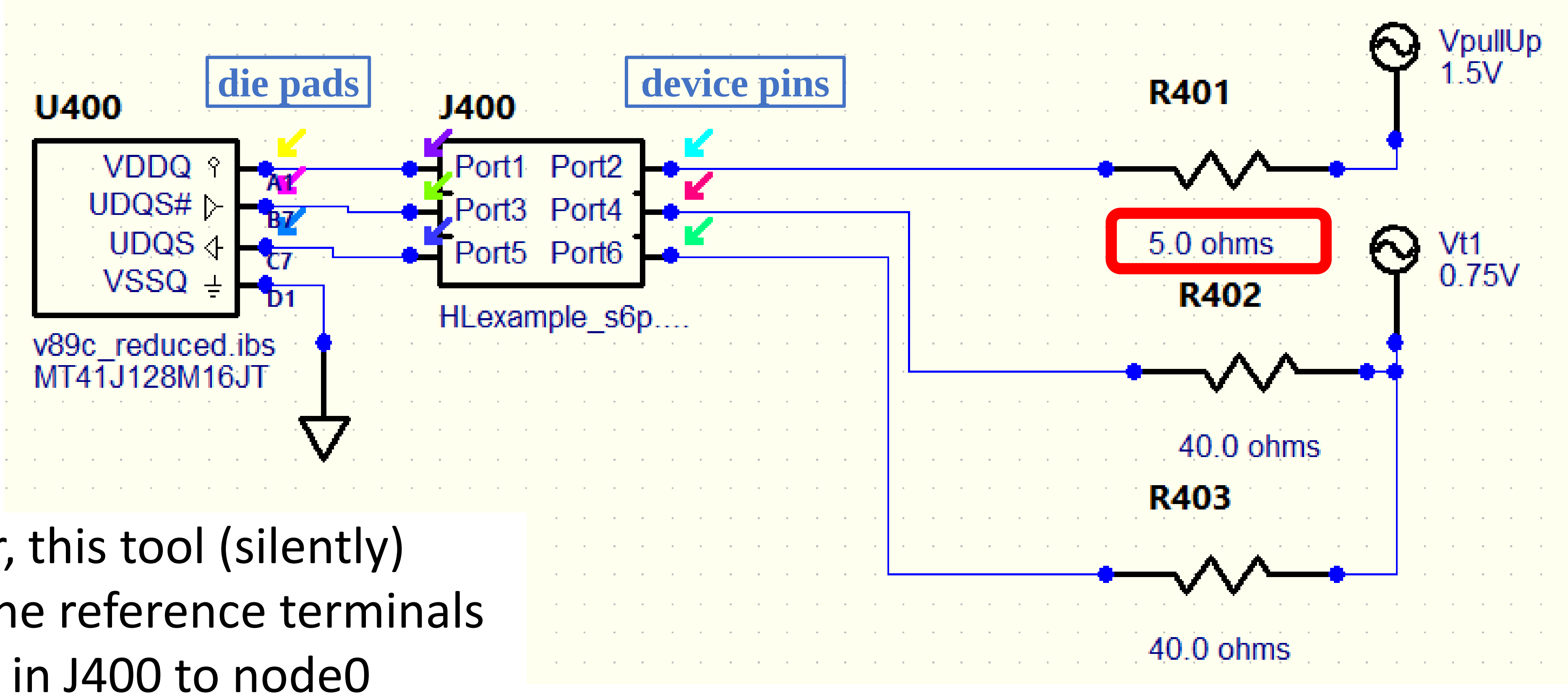
- Moving on: How should we extract a Touchstone model from a physical structure using a Full-Wave solver?

Full-Wave Solver 6-Port S-Parameter Extraction

Vss conductor used as reference
Up to 20 GHz



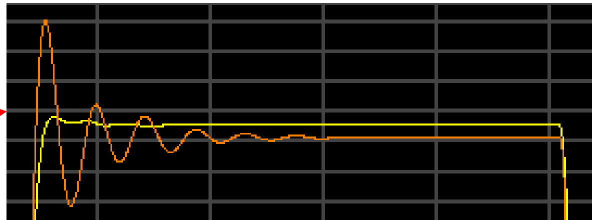
Simulating The Full-Wave 6-Port Model In J400

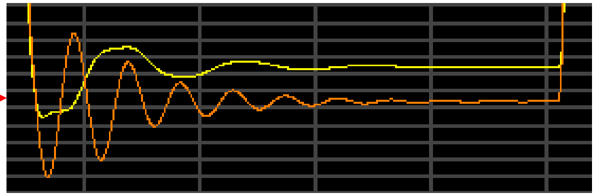


Remember, this tool (silently) connects the reference terminals of all ports in J400 to node0

SPICE and Full-Wave 6-Port Model Waveforms

node0 referenced





Comments On The 6-Port Model

- Since this simulator connects the reference terminals of all ports to node0:
  - the buffer’s Vss pad has to be connected to (the rock solid) node0 too
  - the waveforms are displayed with respect to node0

- Consequently, the simulation results and waveform plots are ***both*** wrong

- NOTE: Using the Vss net as the reference net for the ports during extraction ***does not imply*** that the reference terminals of the ports must be connected to node0 during simulation
  - “Reference” and “node0” are two completely different things
  - While reference terminals are often connected to node0, they are not the same thing

Workaround

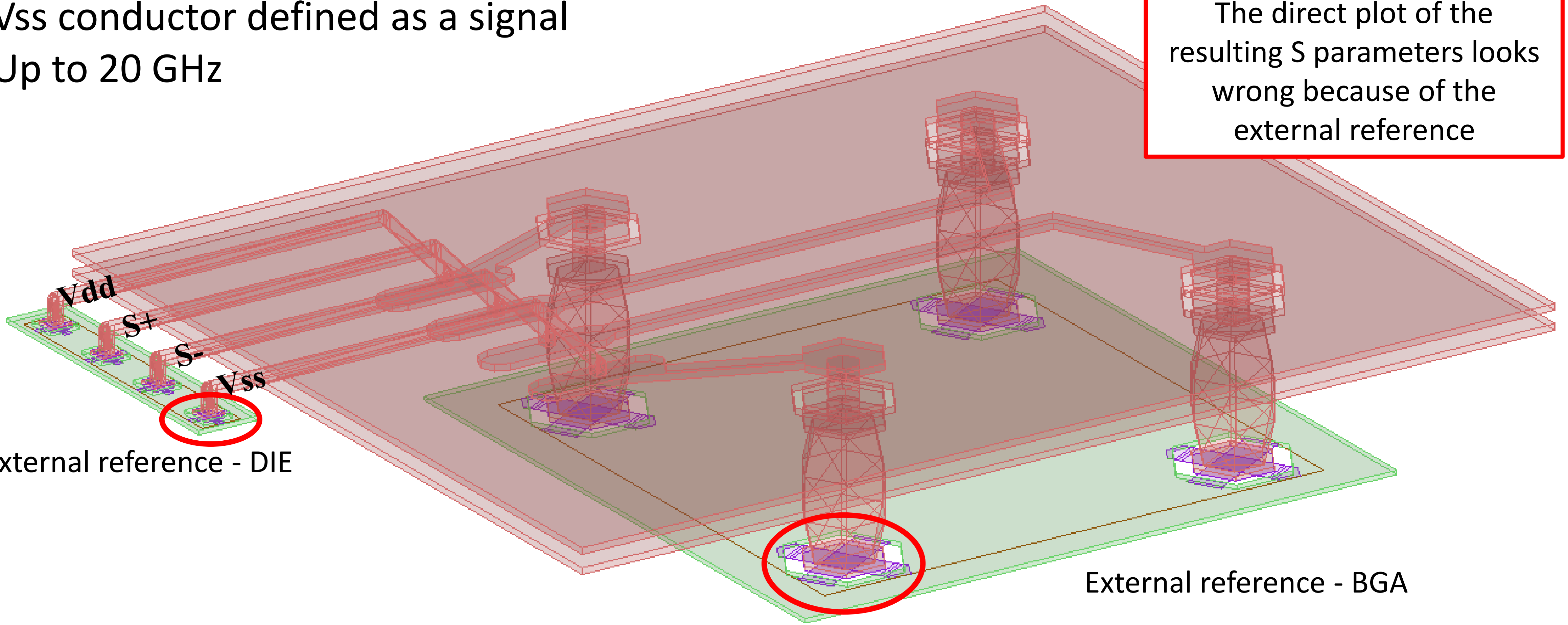
- The following example is a useful trick to work with S-parameter data in simulators that do not provide access to the negative terminal of each port
- This is not a recommendation to move forward with this method

Full-Wave Solver 8-Port S-Parameter Extraction

Vss conductor defined as a signal

Up to 20 GHz

The direct plot of the resulting S parameters looks wrong because of the external reference



External reference - DIE

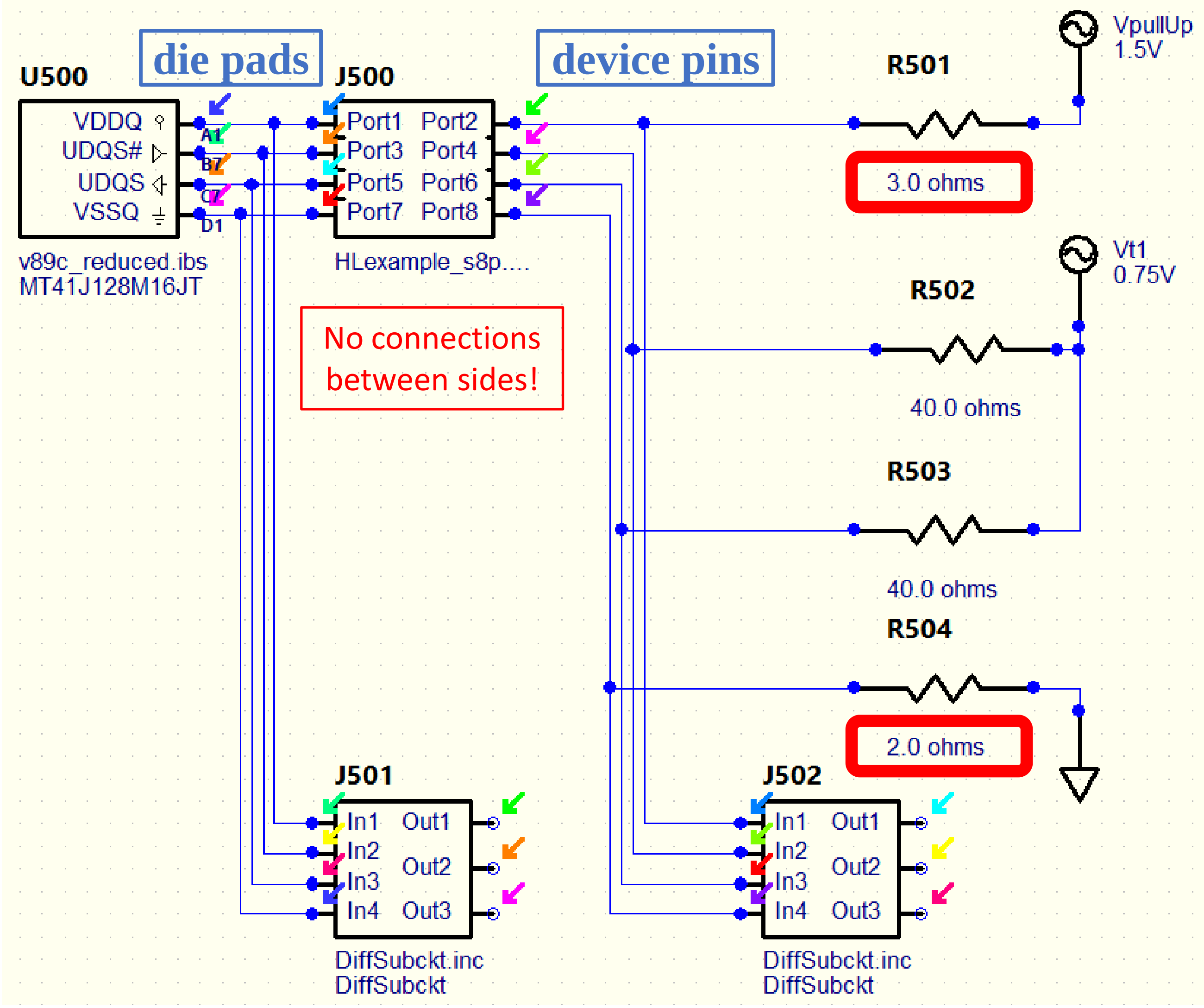
External reference - BGA

Careful

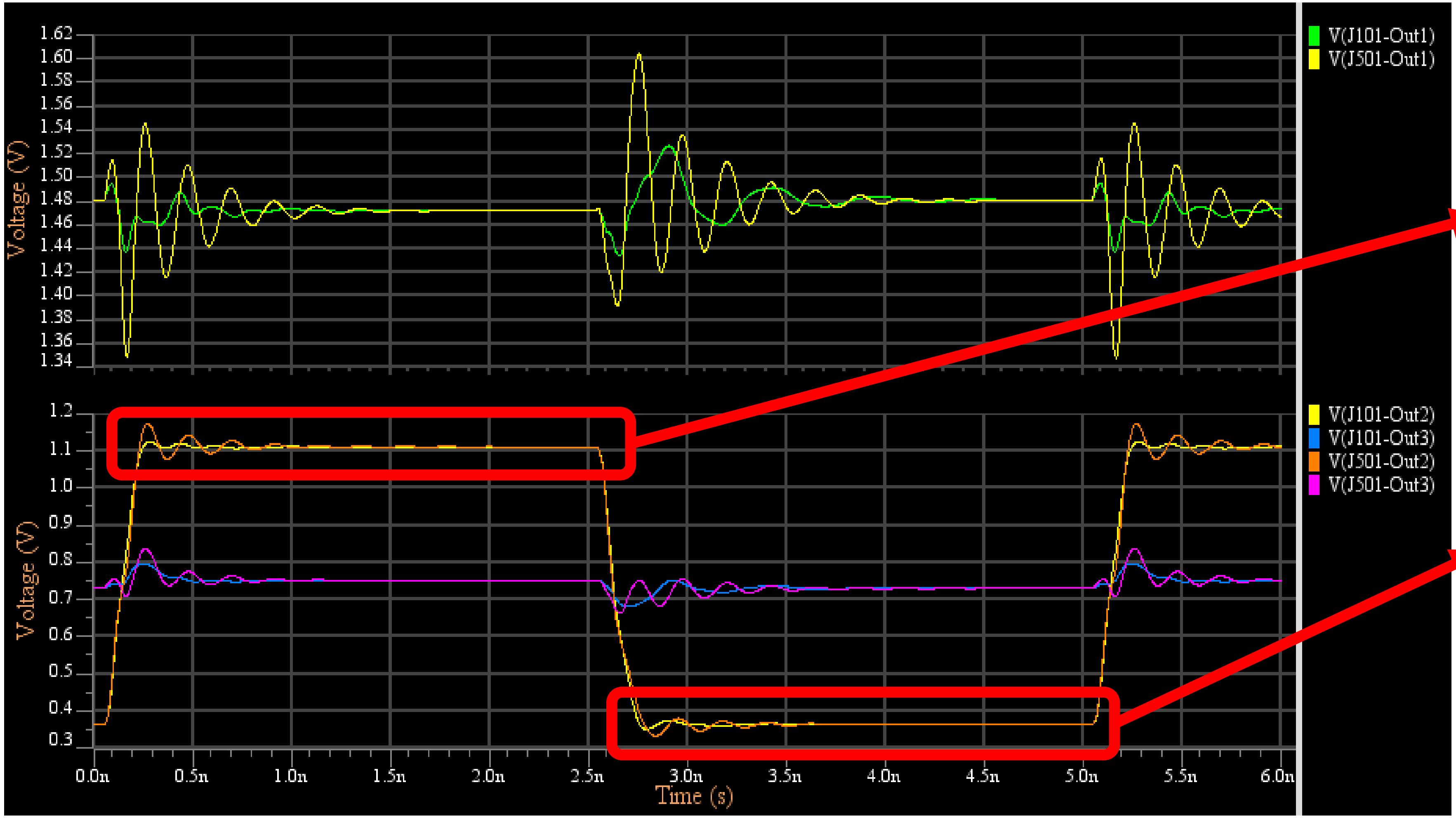
- Be careful with the data transfer from extraction to simulation
- It is practical to connect circuit elements between ports that have the same reference conductor
- Probing a voltage or connecting elements between ports that use different references conductors might produce wrong results

Simulating The Full-Wave 8-Port Model In J500

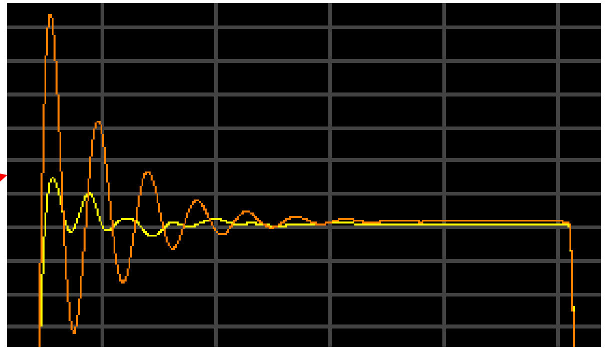
Remember, this tool (silently) connects the reference terminals of all ports in J500 to node0

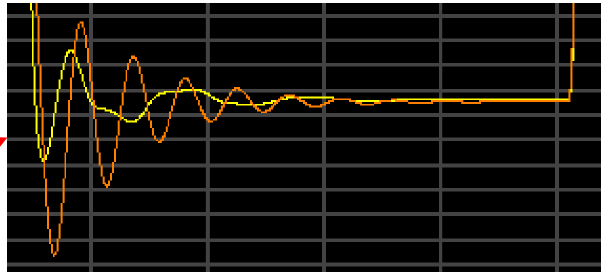


SPICE and Full-Wave 8-Port Model Waveforms



Local Vss referenced

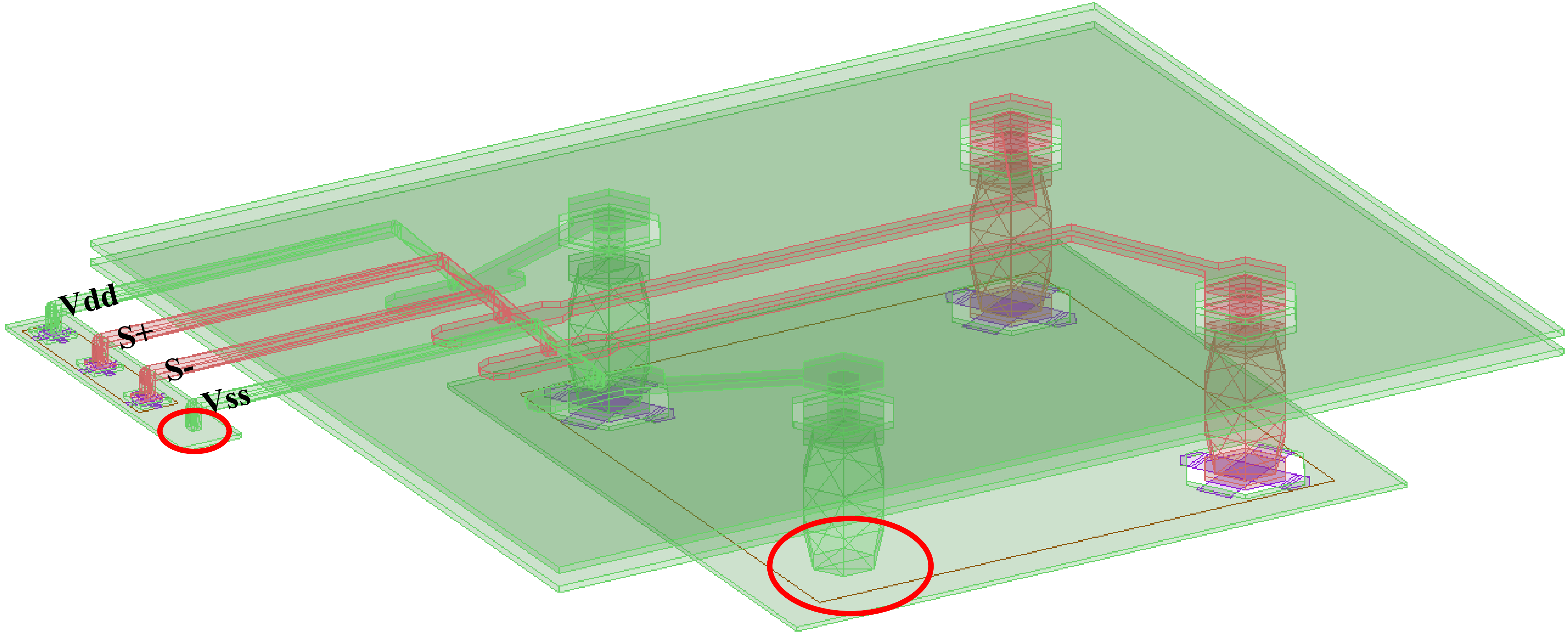




Comments On The 8-Port Model

- Since the Vss net was not the same as node0, the simulation results and waveform plots are both correct this time
  - Note that the Vss referenced waveforms still had to be defined explicitly to bypass the automatic probing “convenience” provided by the tool
- The high frequency oscillations in the 8-port waveforms are probably due to the higher bandwidth (20 GHz) of the 8-port S-parameter model vs. low-pass filter nature of the SPICE model
- Extracting the 8-port model this way is uncommon but useful

Full-Wave Solver 6-Port S-Parameter Extraction

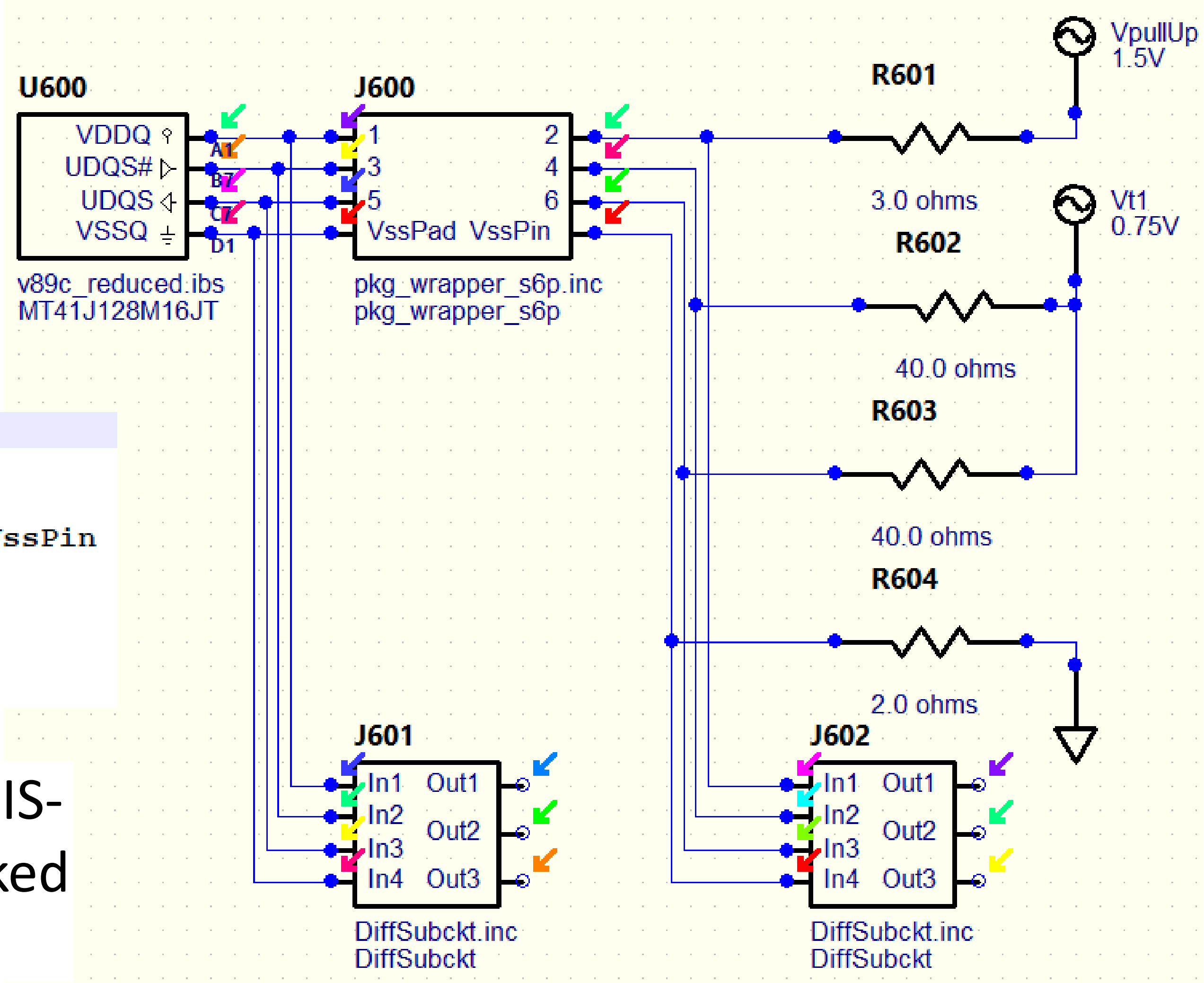


Per Interface Referencing In J600

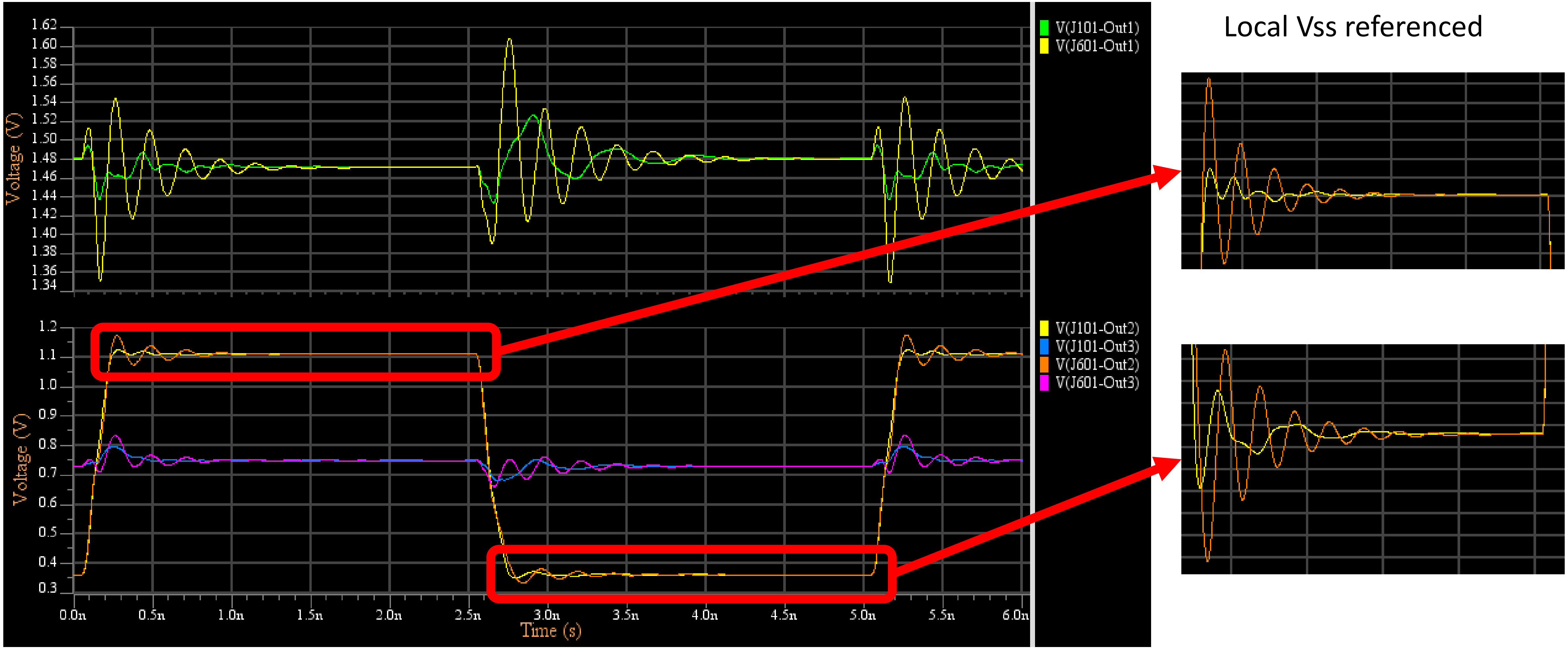
Since the [Interconnect Model] and [EMD Model] keywords do not support multiple reference terminals for S-parameter models, I had to make a wrapper SPICE subcircuit to achieve this goal:

```
.subckt pkg_wrapper_s6p 1 2 3 4 5 6 VssPad VssPin

Ypkg_model FBLOCK
+ PIN: 1 VssPad 2 VssPin 3 VssPad 4 VssPin 5 VssPad 6 VssPin
+ PARAM:
+ STRING: 'HLexample_s6p.s6p'

.ends pkg_wrapper_s6p
```

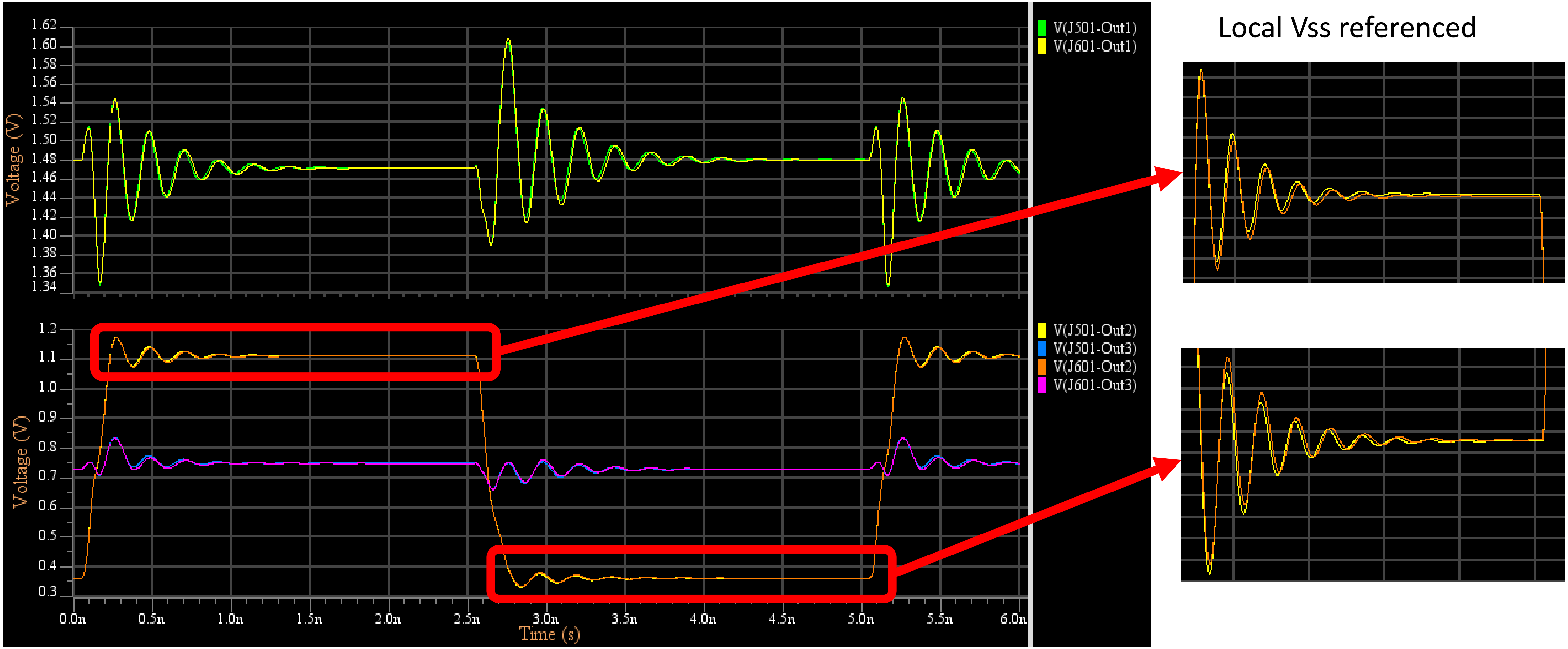
The same can also be achieved using the IBIS-ISS syntax if the S-parameter model is invoked from inside the IBIS file (U600)



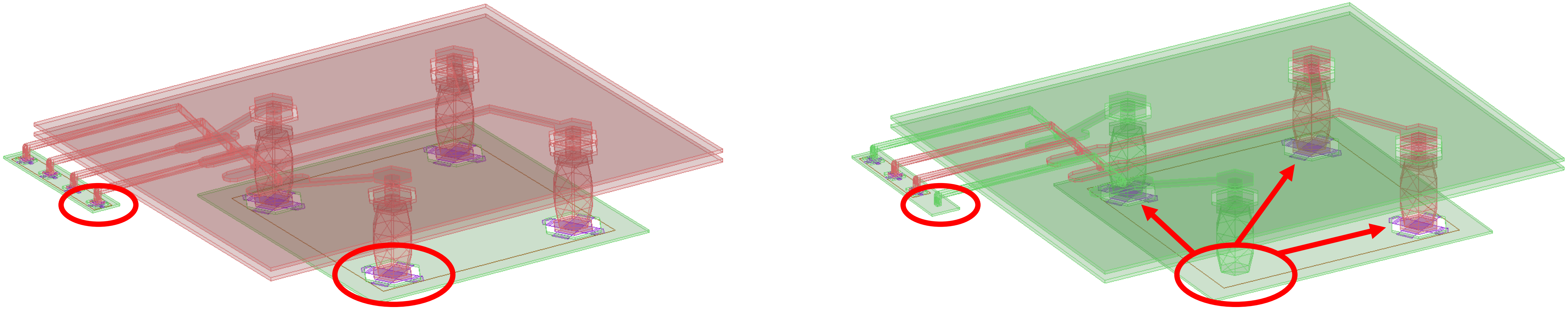
SPICE And Per Interface-Referenced 6-Port Model Waveforms



8-Port And Per Interface Referenced 6-Port Models



Slight Differences



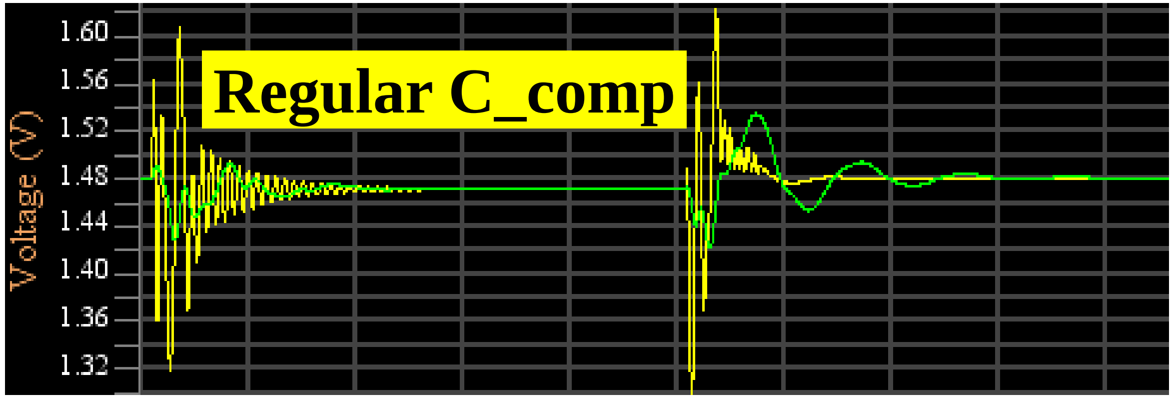
A possible explanation for the slight differences between the waveforms shown on the previous slide is that the metal between the solder balls (marked with the red arrows on the right) is part of VSS net in the 6-port model but not in the 8-port model. This slightly increases the capacitance between signals and VSS and also increases the length of the return path in the 6-port model.
The same also applies to the die-pad ports (not marked to avoid cluttering the image).

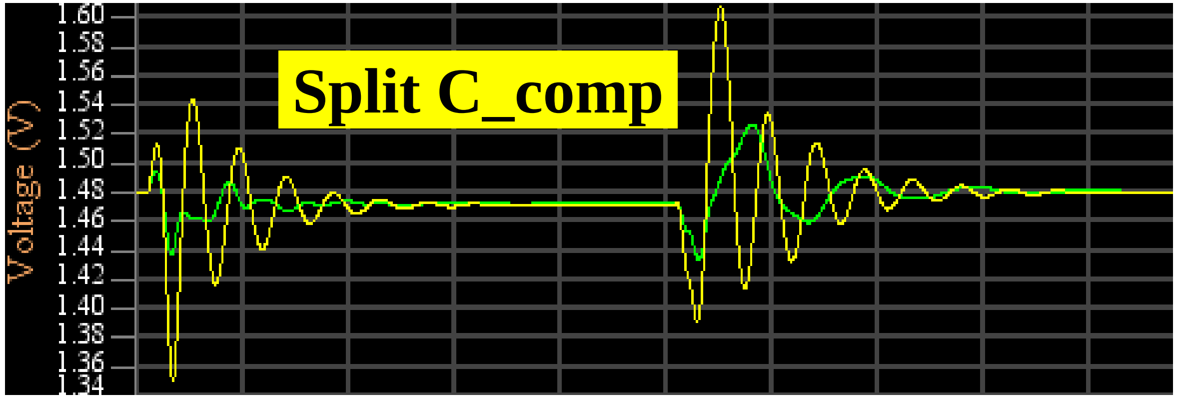
Conclusions

- Use “per interface” referencing where possible
  - The [Interconnect Model] and [EMD Model] keywords in the IBIS specification need to be enhanced to support this
- While waiting for the next IBIS specification, consider the following workarounds
  - Wrap the S-parameter model in an IBIS-ISS (SPICE) subcircuit
    - In this case, make an independent reference terminal for each “interface” (or “side”)
  - Extract the S-parameter model so that Vss is a signal (not a reference) net (see 8-port example)
    - In this case, use node0 (A_gnd) as the reference connection for all ports in simulations
- Waveforms should be plotted with respect to a local reference, not node0
  - True when using RLGC SPICE models
  - True when using S-parameter models with “per interface” reference or Vss defined as signal ports
  - Irrelevant when node0 is used as the reference for Vss pins or pads. The waveforms will be wrong anyway due to incorrect modeling.
- Simulators and their associated schematics need to provide connectivity to both terminals of all S-parameter ports for extraction and implementation

Bonus Point

- It is crucial to have the “split C_comp” subparameters in the [Model] keyword
- The C_comp_pullup, C_comp_pulldown, C_comp_power_clamp, and C_comp_gnd_clamp capacitors are connected in parallel with their respective I-V tables which are connected to the corresponding supply rails defined by the [Pullup Reference], [Pulldown Reference], [POWER Clamp Reference] and [GND Clamp Reference], and [Pin Mapping] keywords
- The “regular” C_comp capacitance is connected between the signal pad and node0 (A_gnd), consequently this capacitor’s current will not go through the buffer’s supply rails which can result in unexpected oscillations

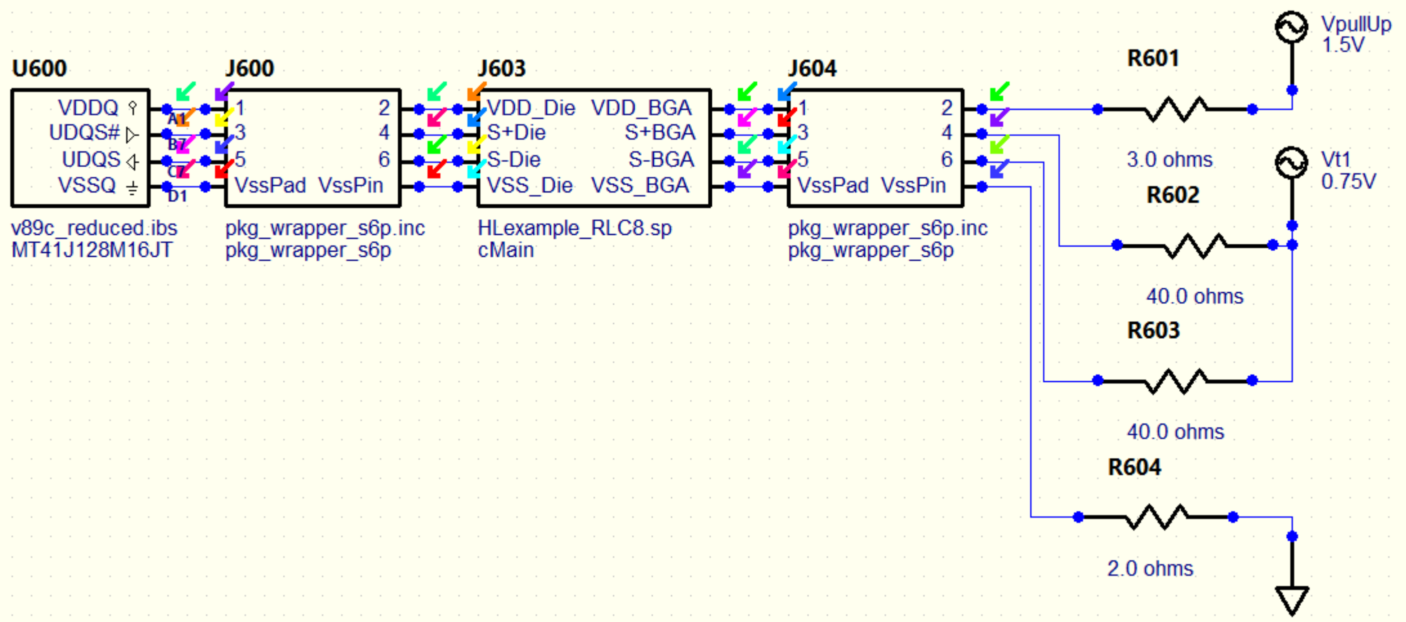




Full-Wave 8-port package model (yellow) vs. SPICE subcircuit package model (green)

Ideas For Future Exploration

1. Show that “per interface referencing” works also when cascading mixed SPICE and S-parameter models



2. Perform the same experiments with a fully power aware buffer model

- Expecting cleaner waveforms due to additional on-die decoupling and because the [ISSO ***] data acts similar to negative feedback, weakening the driver when the supply voltage collapses

Questions, comments?

Thank you!