IBIS-AMI Modeling Methodology for Simultaneous Bi-Directional (SBD) Die-to-Die Chiplet Connectivity

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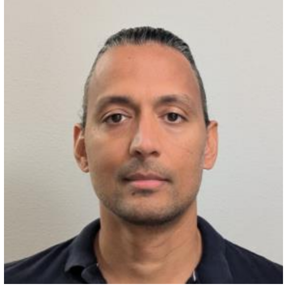
Speakers



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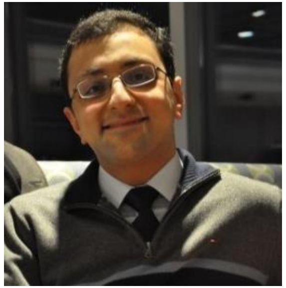
Arpit Kothari is a Principal Engineer at Eliyan Corp, specializing in Signal and Power Integrity.



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Mohammad started with Eliyan in 2021 as an analog/Mixed-Signal design engineer where he focused on developing circuits for Die-to-Die high speed links. He is currently a SIPI engineer focusing on Electro-Optical system integration, 224G/448G SerDes and Die-to-Die links' signal and power integrity.

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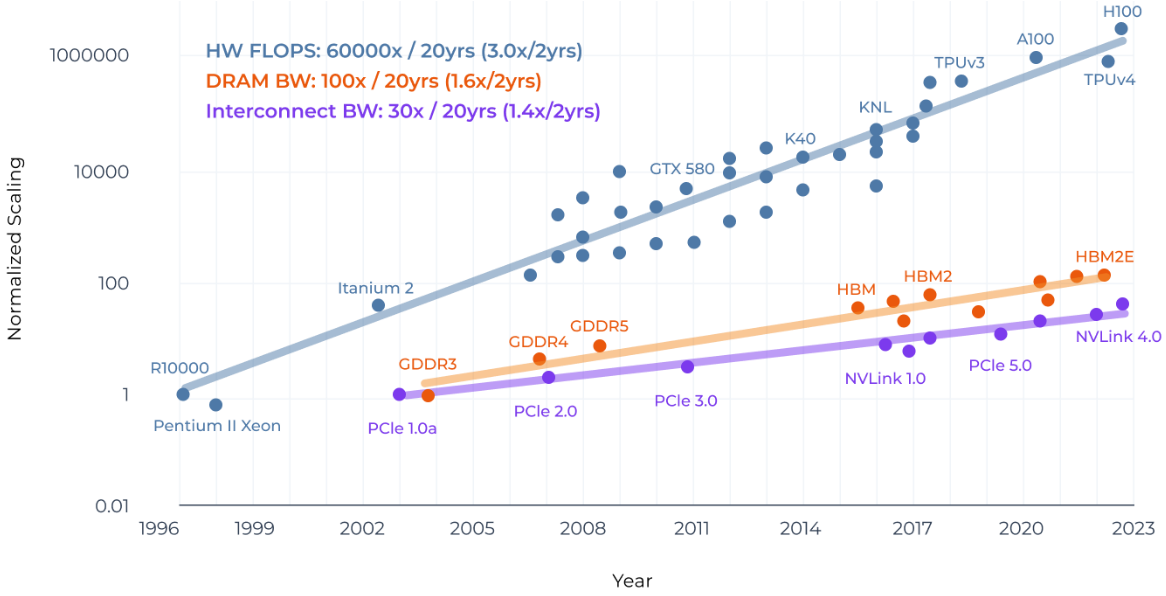
Ali is currently Director of Packaging, Signal, and Power Integrity at Eliyan, focusing on high-speed digital design including 224G/448G SerDes, UCIe and BoW Die-to-Die interconnects for next-generation chiplet architectures.

Outline

- Top bottlenecks in AI performance
- Die-to-Die interfaces
- Uni-Directional vs Simultaneous Bi-Directional signaling
- SBD architecture
- Echo cancellation
- IBIS-AMI modelling for SBD signaling
- Simulation details and results
- Conclusion

Today's Top Bottlenecks in AI Performance: Memory & I/O

Scaling of Peak hardware FLOPS, and Memory/Interconnect Bandwidth



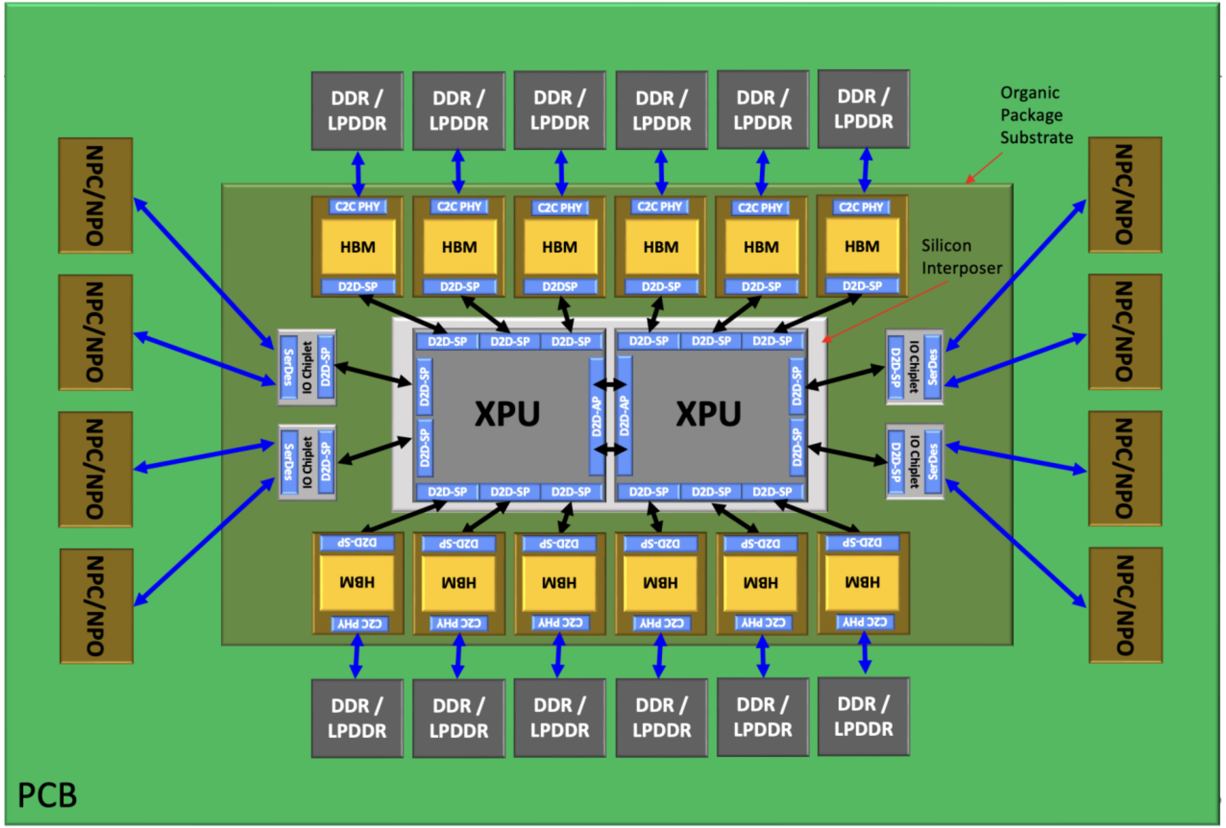
Note: HW (Hardware), FLOPS (Floating-point Operations Per Second), BW (Bandwidth)

Source: Amir Gholami et al. (2024), *AI and the Memory Wall*, UC Berkeley

TrendForce

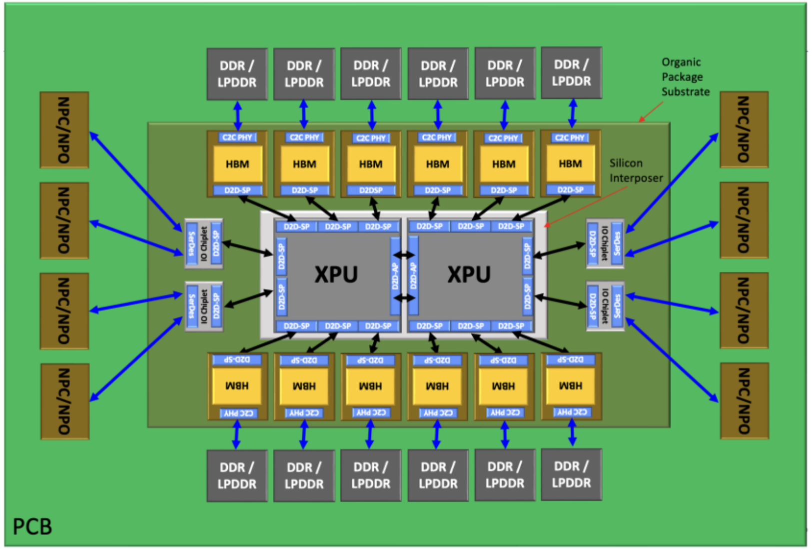
Enabling Next-Generation Bandwidth Requirements

- **High-Speed Link Architecture:**
- *Within Package:*
    - Die-to-die: XPU-to-XPU on silicon interposer
    - Die-to-die: XPU-to-memory/IO chiplets on organic substrate
- *Beyond Package:*
    - Chip-to-chip: Off-package memory extension
    - SerDes-to-PCB: IO chiplet to NPC/NPO interconnects



Die-to-Die Interfaces – Standards

- Goal:
    - Create SoCs using chiplets as “Lego” blocks with “standard” Die-to-Die link



- UCIe and BoW:
    - Use chiplets with D2D IPs from different vendors
    - Use D2D IPs to connect chiplets from different process nodes

- Package Type:
    - Organic Substrate (Standard Packaging)
    - Silicon Interposer or Fanout RDL (Advanced Packaging)
- Reach (Channel Length):
    - Up to 25mm in Standard Packaging
    - Very Short (less than few mm) in Advanced Packaging
- Signaling:
    - Single Ended
    - CLK Forwarded
- Data Rate:
    - Up to 64 Gbps

Figure of Merit: Beach Front Density

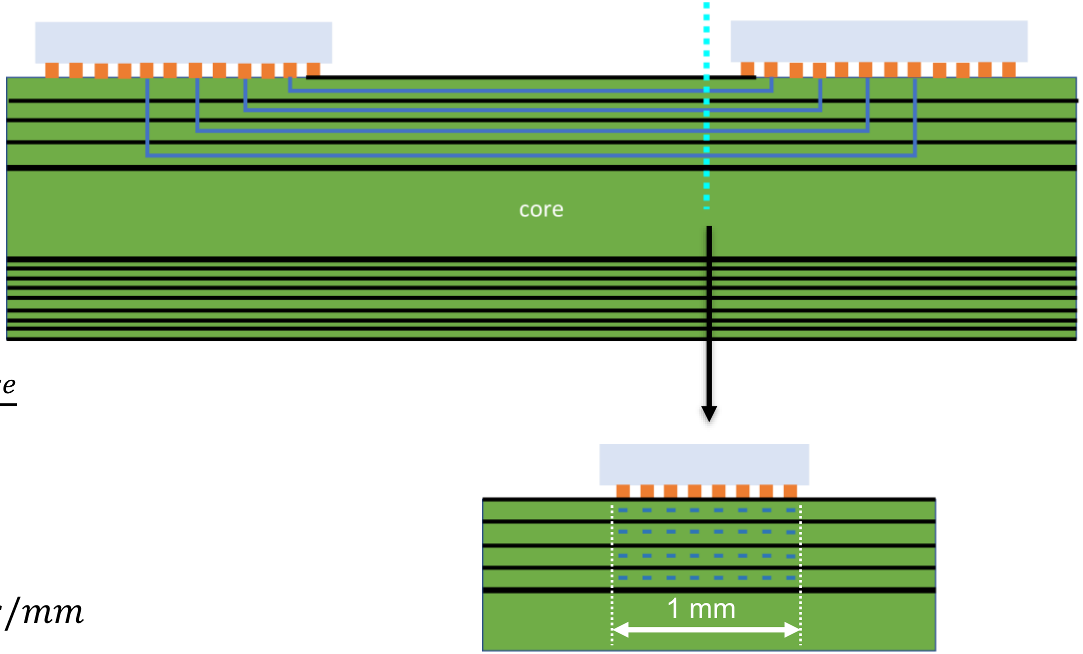
- Market demand: increase the performance!
  - Increase the bandwidth
  - Reduce the power
  - Reduce the active area on the silicon

- Beach Front Density =

$$\frac{Number\ of\ signal\ wires\ in\ breakout \times Data\ rate\ per\ wire}{Width\ of\ the\ breakout}$$

- Example:

Beach Front Density = $\frac{32 \times 32\ Gbps}{1mm} = 1024\ Gbps/mm$



Breakout Cross-section

How to Double the FoM?

Typical Solutions

- Double the data rate per wire
    - Deal with higher loss as the Nyquist frequency is doubled
    - Deal with more crosstalk
- Change the line coding scheme from NRZ to PAM4
    - Deal with circuit and DSP complexity
    - Deal with worse signal to noise ratio
- Double the number of wires in the same cross-section
    - Double the substrate layer count: deal with higher manufacturing cost, higher reflection and higher crosstalk in deeper signal vias
    - Reduce signal to signal pitch to half: deal with higher trace to trace crosstalk

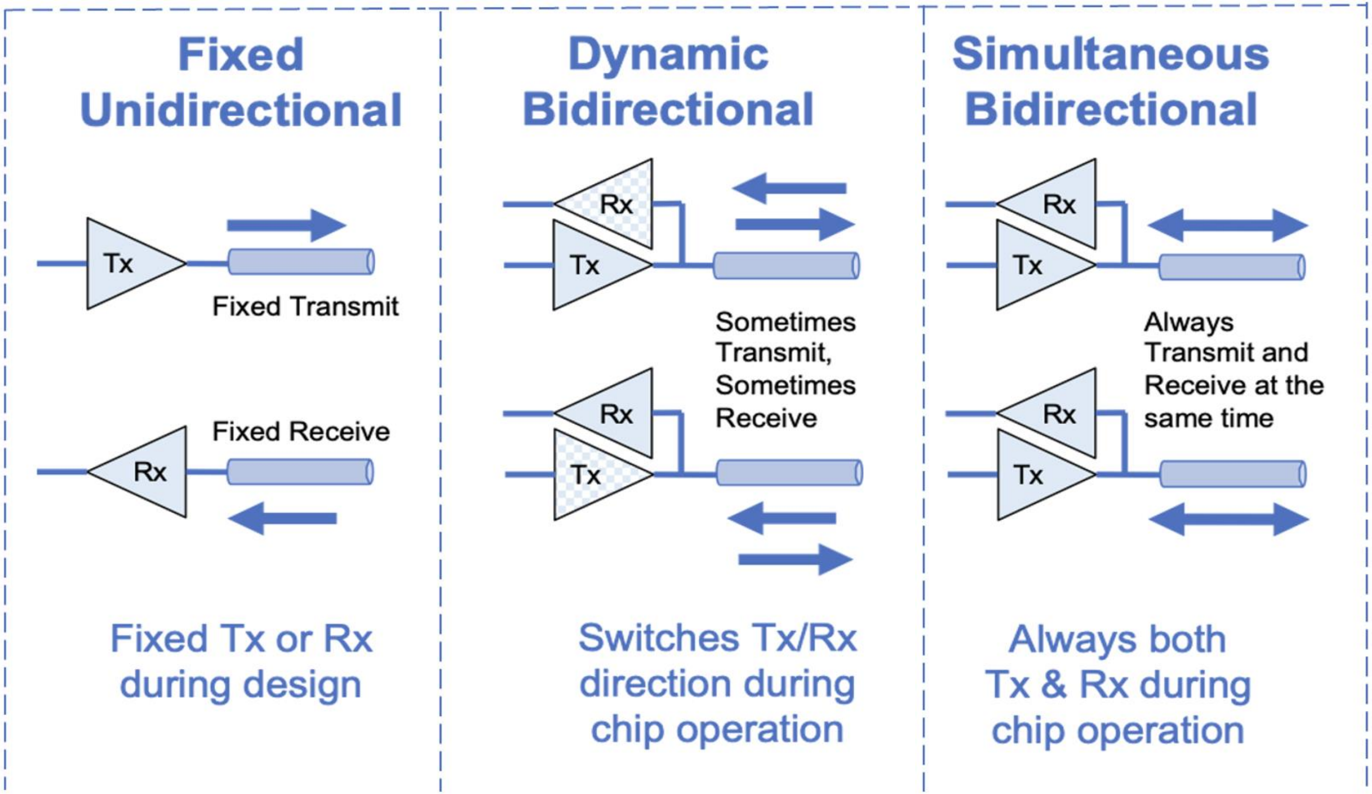
SBD Solution

- Keep the same layer count, signal count, and data rate per wire
- Use the same wire for transmit and receive of the signal

- Effective bandwidth is doubled

Brilliant!!!

Uni-Directional vs Bi-Directional Signaling



Fixed Unidirectional

Fixed Transmit

Fixed Receive

Fixed Tx or Rx during design

Dynamic Bidirectional

Sometimes Transmit, Sometimes Receive

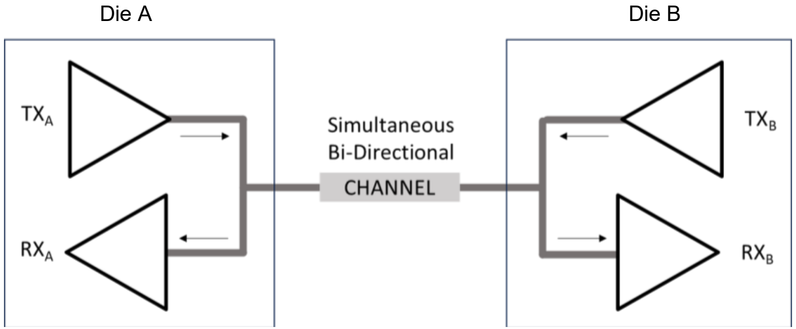
Switches Tx/Rx direction during chip operation

Simultaneous Bidirectional

Always Transmit and Receive at the same time

Always both Tx & Rx during chip operation

The Fundamental SBD Problem



Signals present at RX_B:

1. Main signal from far-end TX_A (weak, attenuated by channel).
2. Echo from local TX_B (strong, minimal attenuation).
3. Crosstalk from neighboring lanes.

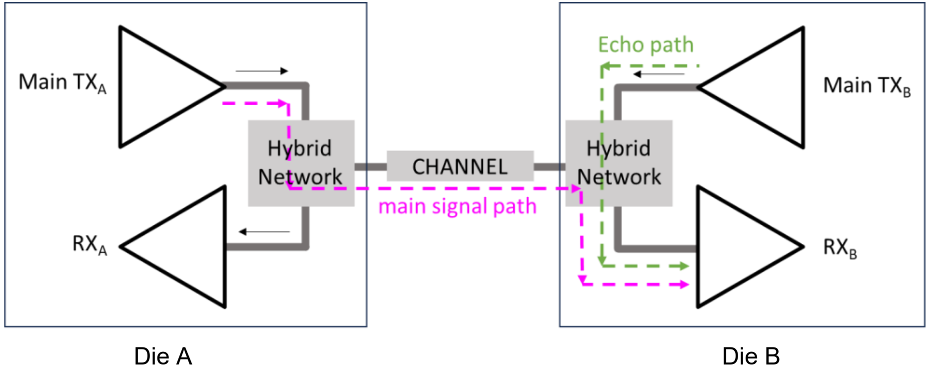
Challenges:

- Echo is usually stronger than the main signal depending on the loss of the channel.
- Receiver cannot distinguish the two signals.

Analogy: Like trying to hear someone across a room while someone next to you is shouting

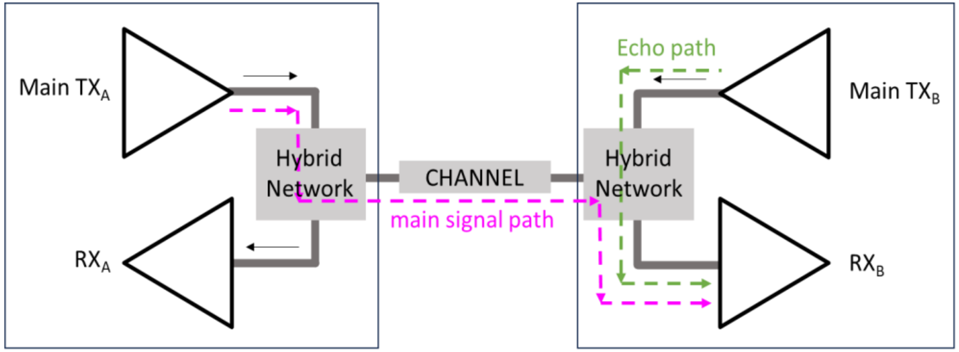
SBD Architecture Details

- **Die A**:
  - Main TX_A: Transmits data to Die B
  - RX_A: Receives data from Die B
  - Both connected to same node/wire
- **Die B**:
  - Main TX_B: Transmits data to Die A
  - RX_B: Receives data from Die A
  - Both connected to same node/wire
- **Channel**:
  - Package substrate traces & vias
  - PCB traces (if applicable)



- **Hybrid network**:
  - Separates main signal from the echo.

Signals Paths in SBD



Die A

Die B

Main signal path (Desired):

TX_A → Hybrid Network (Die A) → Channel (substrate/PCB) → Hybrid Network (Die B) → RX_B

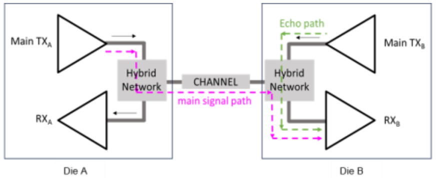
- Must be preserved.
- Goes through channel and transitions in between. Subject to channel loss and reflections.

Echo path (Undesired):

TX_B → Hybrid Network (Die B) → RX_B

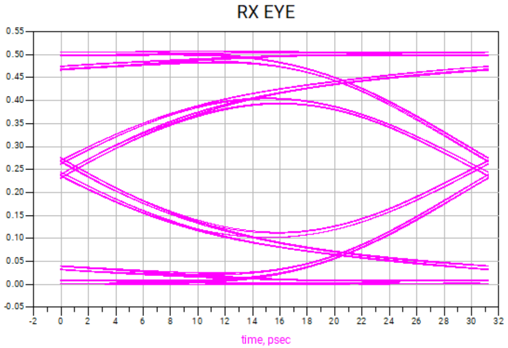
- Must be eliminated.
- Minimal loss irrespective of channel length.
- Same-side as the receiver, coupling through the hybrid network.

Visualizing the Problem (EYE)



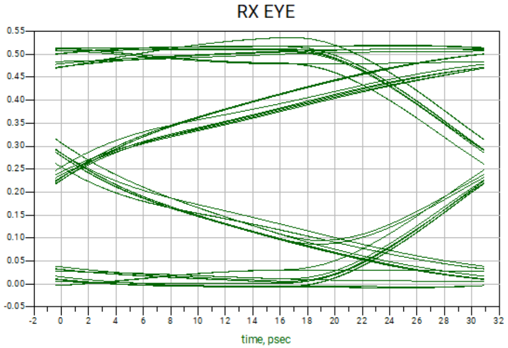
Main signal:

- TX_A to RX_B
- Clean eye
- Two clear signal levels
- This is what we want to see



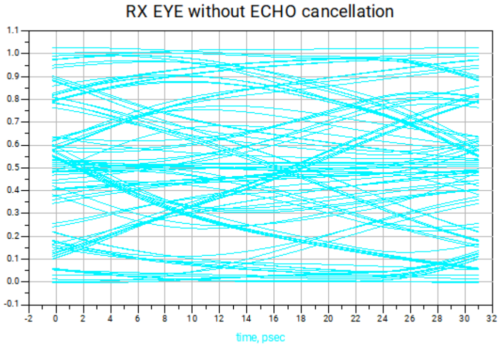
Echo signal:

- TX_B to RX_B
- Strong, clean eye
- Two clear signal levels
- Minimal distortion (short path)



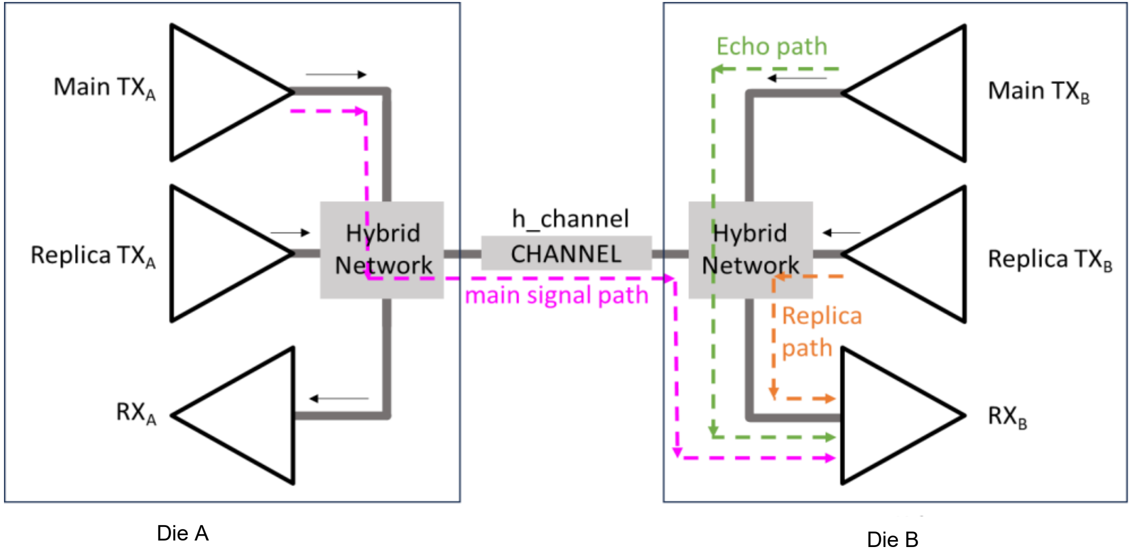
Main + Echo:

- Completely scrambled eye pattern
- Impossible to recover data
- System is non-functional



Echo Cancellation Concept

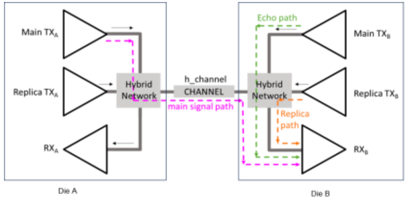
Solution: Generate a "replica" of the echo signal and subtract it from the received signal



$$V_{RX} = V_{main} + V_{echo} - V_{replica}$$

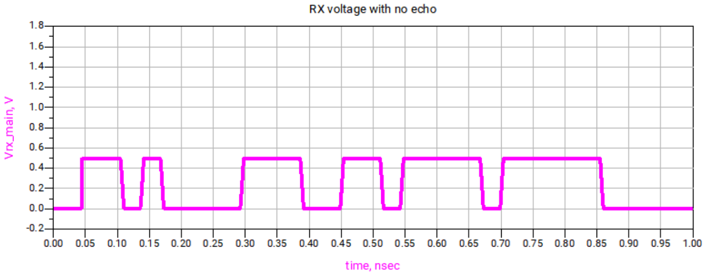
$$V_{replica} \approx V_{echo} \Rightarrow V_{RX} \approx V_{main}$$

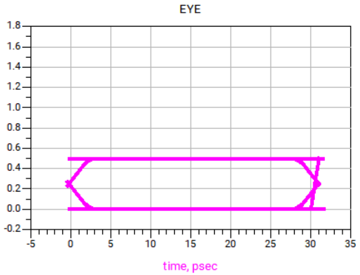
Visualizing Echo Cancellation



Main path signal (no echo)

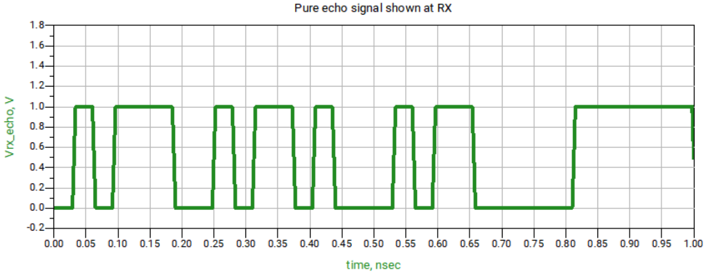
- Good signal quality
- Open Eye at receiver

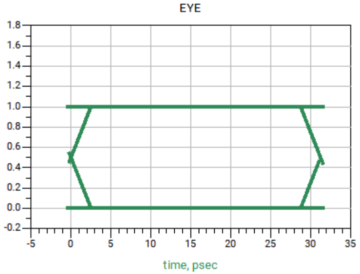




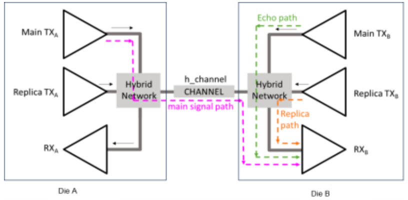
Echo path waveform

- Shows the strong local TX coupling
- Open Eye at receiver
- Larger signal swing at receiver compared to main path





Visualizing Echo Cancellation

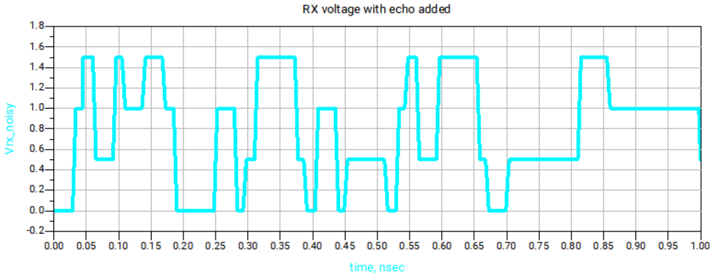


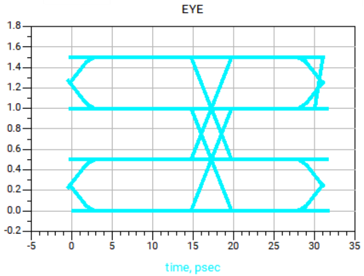
Receiver signal with echo

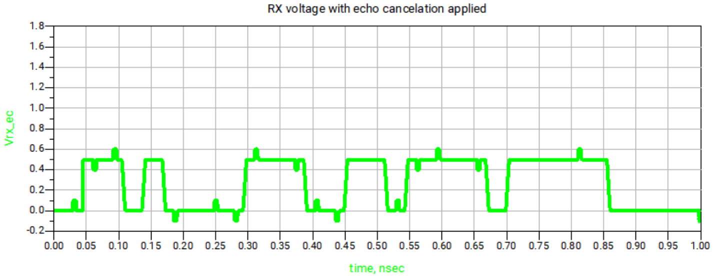
- Main and echo signals superimpose
- Four signal levels instead of two (superposition)
- Closed eye

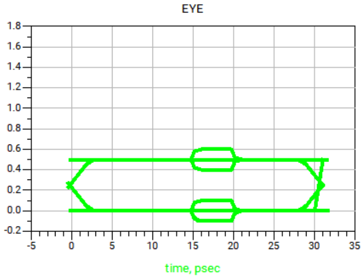
Receiver signal with cancelled echo

- Replica signal simulated to be same as echo with a 0.5 ps delay to illustrate one possible mismatch source
- Echo & Replica signals do cancel each other except for a small remnant in the form of tiny bumps demonstrating echo cancellation – Open Eye


RX voltage with echo added


EYE


RX voltage with echo cancelation applied


EYE

Modeling Challenge

- IBIS-AMI is the industry standard for high-speed link analysis
    - Fast simulations (minutes vs. days in SPICE)
    - Protects design IP through abstraction
    - Extensive EDA tool ecosystem
    - Proven for unidirectional SerDes
- THE PROBLEM: IBIS-AMI was designed for unidirectional links
    - Originally designed to support a balanced DIFF topology – highest number of features are supported here
    - Designed for a clear TX to RX signal flow
    - No provision for simultaneous transmission from both ends
    - No framework for echo cancellation paths
    - The Framework for Singled-Ended simulations is more constrained than Differential

IBIS™

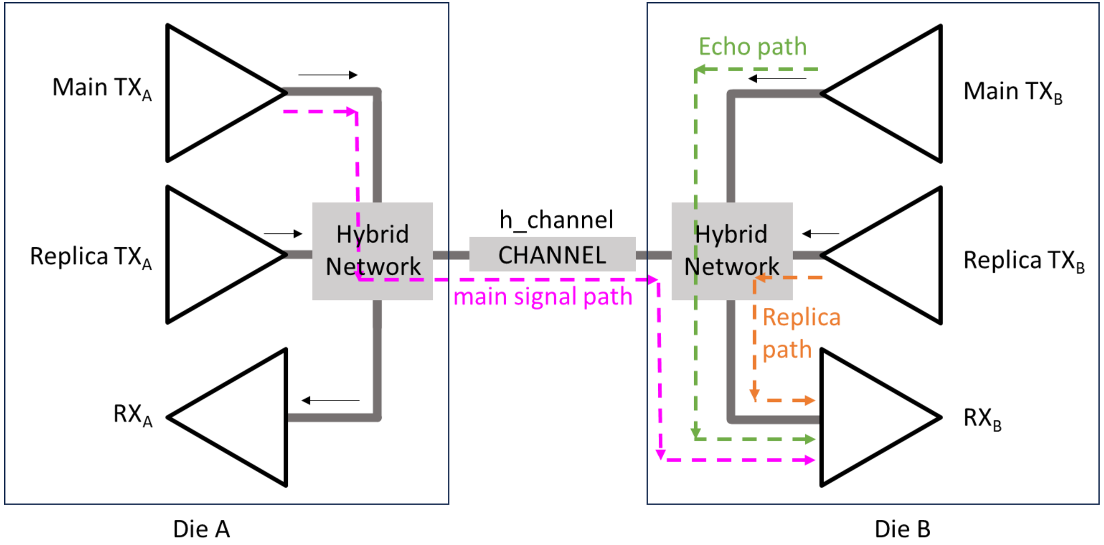
An SAE Industry Technologies Consortia Program

Proposed Methodology

Our Solution: Novel decomposition methodology using signal superposition - First industry approach for single-ended SBD in IBIS-AMI

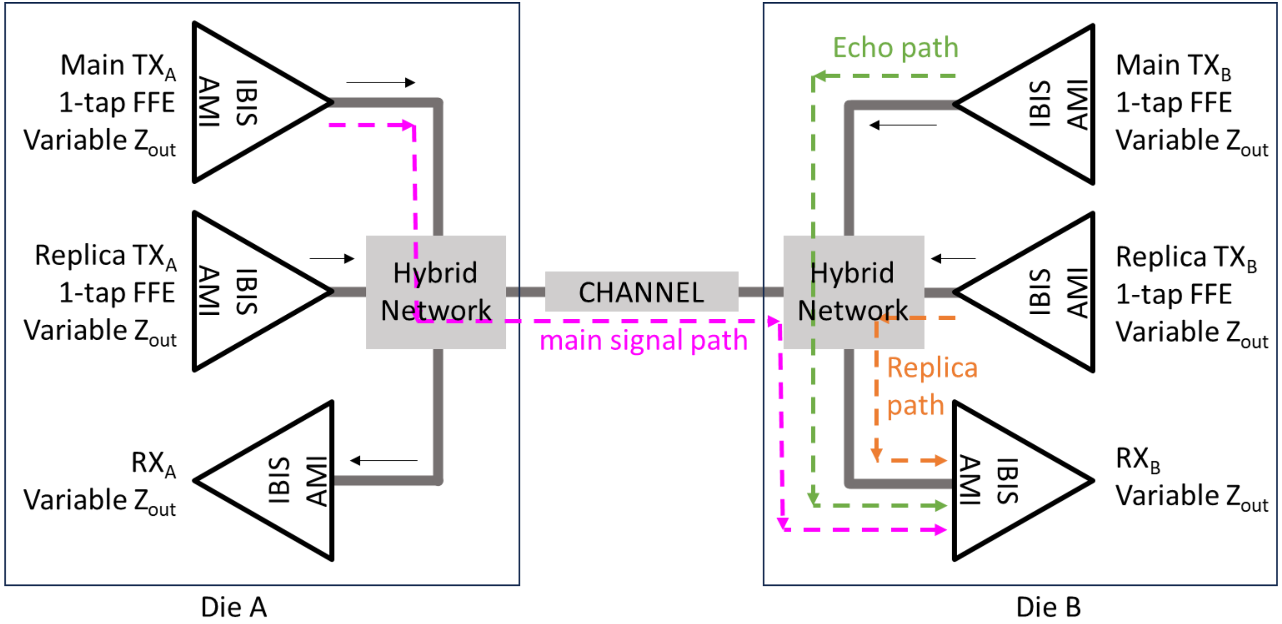
Three Paths:

- Path 1: Main Signal
  - TX_A → Channel → RX_B
  - Desired far-end signal
- Path 2: Echo
  - TX_B → Echo Path → RX_B
  - Local transmitter coupling
- Path 3: Echo Cancellation
  - Replica TX_B → the Replica Path → RX_B
  - Cancels the echo signal

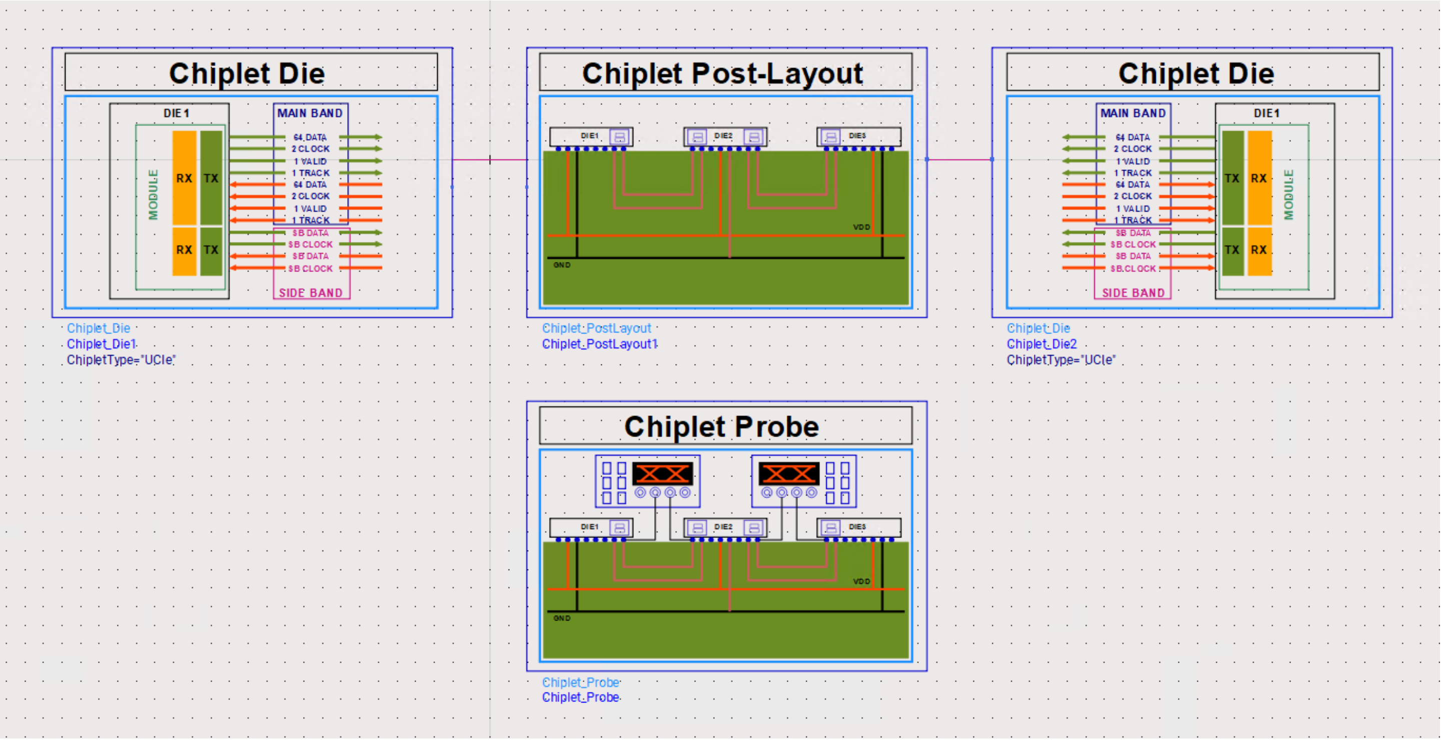


Simulation Workflow

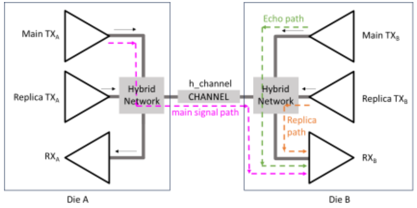
- **Step 1**: IBIS-AMI Model & Channel Extraction
- **Step 2**: Individual Path Simulations
- **Step 3**: Superposition & Tuning
- **Step 4**: Analysis



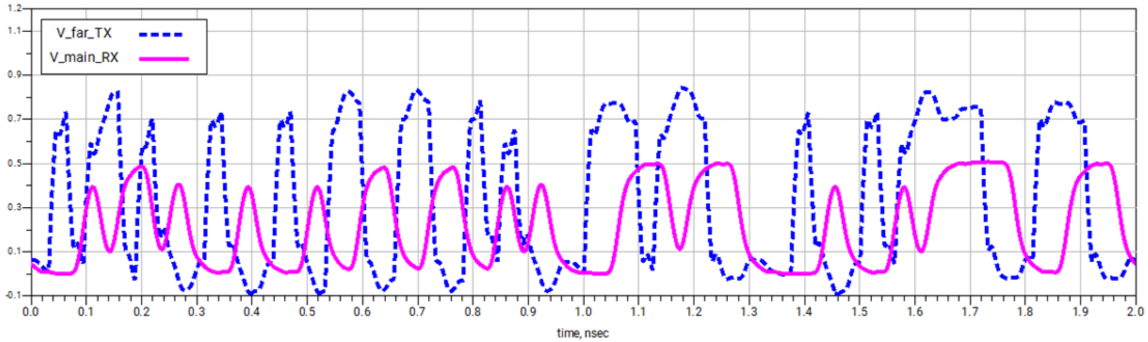
Schematic Setup in EDA Platform



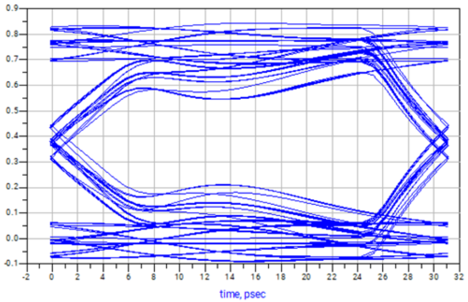
Individual Results – Main Path



- **Main Path** (TX_A to RX_B): Desired signal after channel propagation

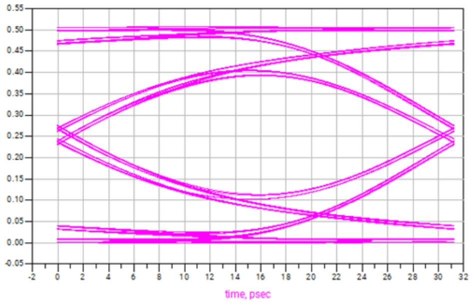


TX EYE

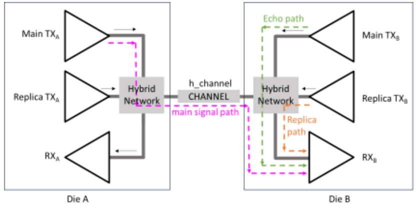


CHANNEL

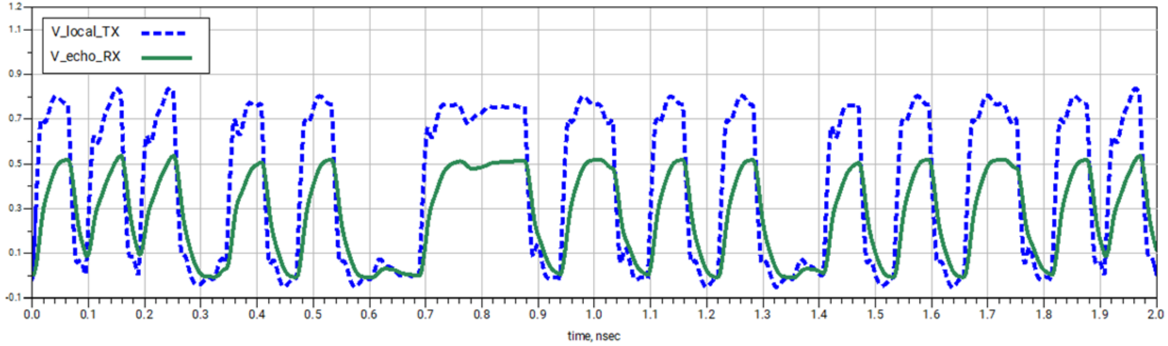
RX EYE

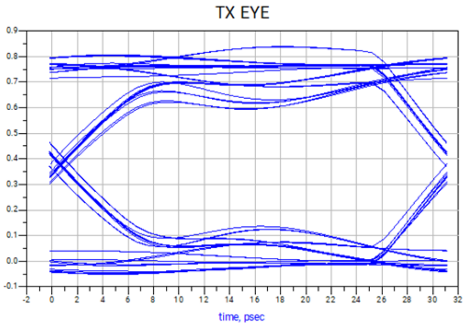


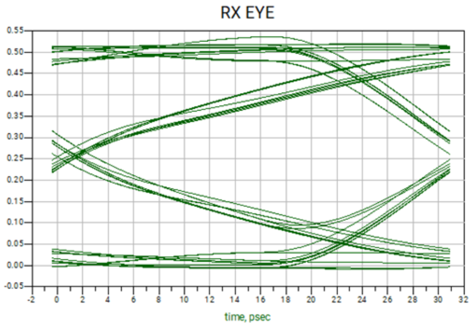
Individual Results – Echo Path



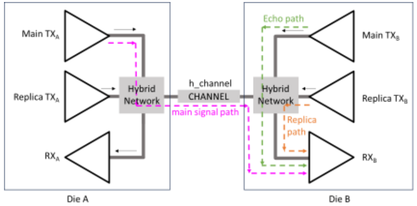
- **Echo Path** (TX$_B$ to RX$_B$): Strong local coupling - must be cancelled



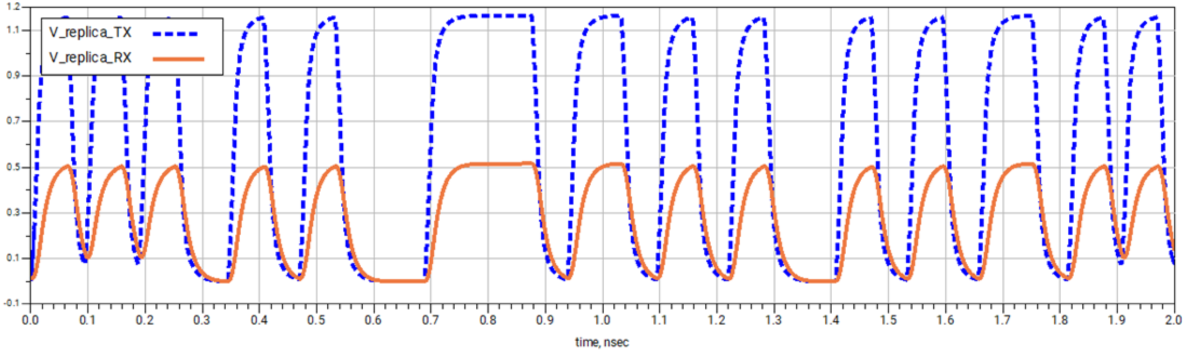


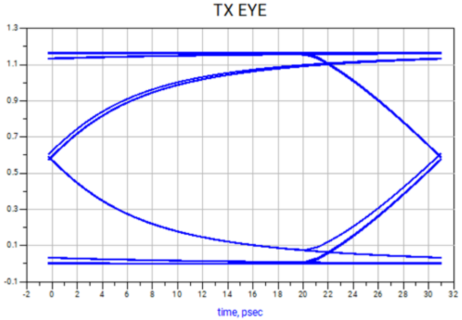


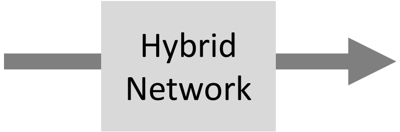
Individual Results – Replica Path

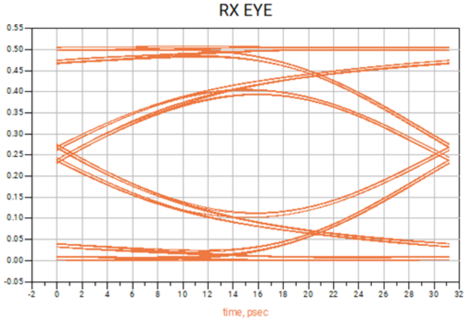


- **Replica Path:** Cancellation signal - matches the echo

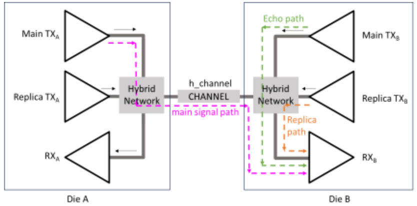




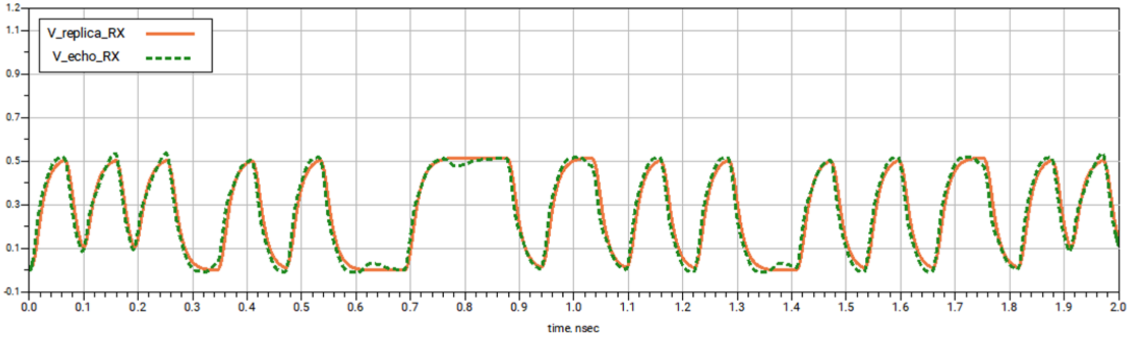




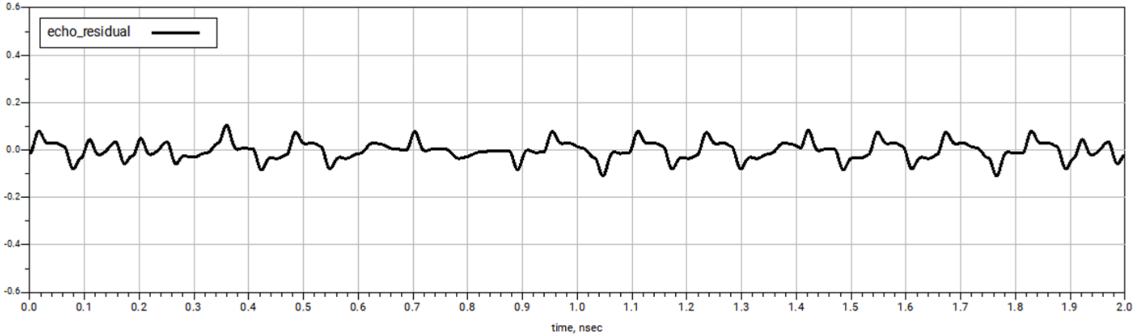
Individual Results – Replica vs Echo



- Replica and eco path waveforms compared at receiver RX$_B$

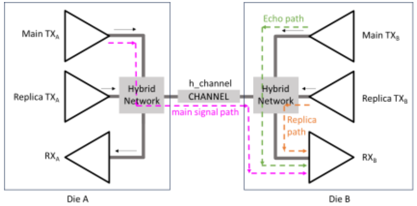


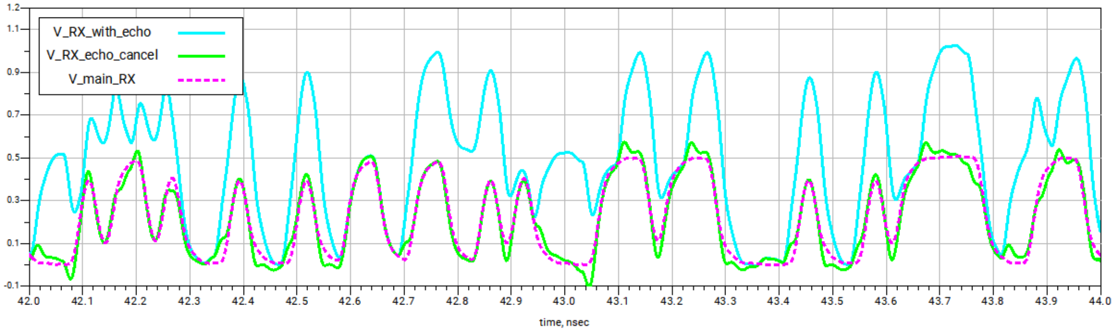
- Eco cancelation residual at the near end receiver RX$_B$

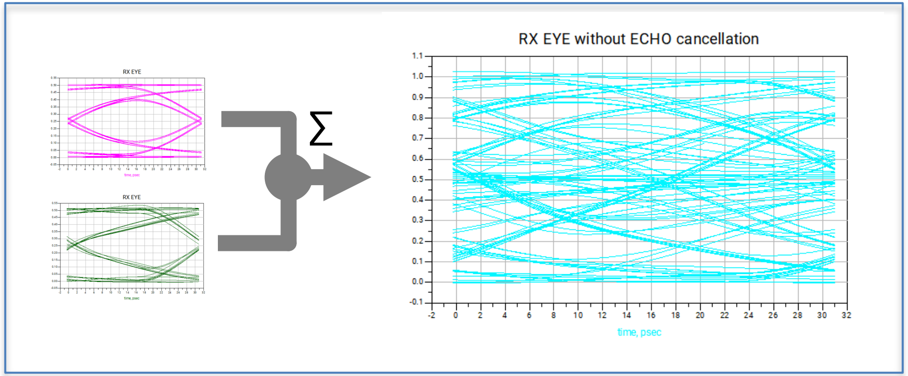


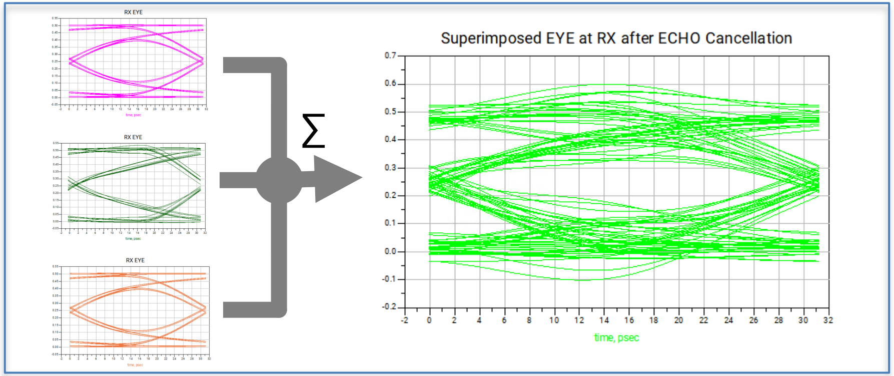
Superimposed Results

- **Post Echo Cancellation:** Signal at RX_B with leftover impairment









Conclusion

- **What We Achieved:**
  - First IBIS-AMI methodology for single-ended SBD links
  - Decomposition approach using signal superposition
  - Validated at 32 Gbps per direction
- **Why It Matters:**
  - SBD doubles bandwidth density for chiplet interconnects
  - IBIS-AMI is industry standard but couldn't handle SBD
  - Our methodology removes this barrier
  - Enables UCIe/BoW standards to adopt SBD signaling
- **Key Insight:**
  - Echo cancellation is the critical challenge in SBD - understanding and modeling it properly is essential for successful implementation
- **Future:**
  - Extends to crosstalk cancellation
  - Adaptation algorithm modeling
  - Multi-lane system analysis

Questions

Thank You!

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