Advances on the ICEM model for Emission of Integrated Circuits

Sébastien Calvet
sebastien.calvet@motorola.com
sebastien.calvet@insa-tlse.fr

http://intrage.insa-tlse.fr/~etienne
Contents

1. Context of the study
2. System design methodology for EMC
3. The IERSET project on EMC for ICs
4. Core emission model
5. Emission model with I/Os
6. Adaptation of emission model
7. Emission model in TEM cell
8. Implementation of ICEM in IBIS-ML
9. Perspectives
Conclusion
1. Context of the study

- 0.7μm, 2 metal layers
- Up to 100,000 devices on a chip
- CPU frequency 50MHz

- 0.12μm, 6 metal
- Up to 200,000,000 devices
- CPU frequency 1GHz

10 years of evolution

40 pins

1000 pins

January 20021 - IBIS Summit Santa Clara
1. Context of the study

- Voltage supply decreases
- Current amplitude keeps constant
- Faster switching

Increased EMC problems
1. Context of the study

Low parasitic emission is a key argument

- **Supplier A**: 40dB, Probably EMC compliant
- **Supplier B**: 10dB, Not EMC compliant

**Ultimate target**: dBuV
1. Context of the study

Example for automotive

Interference with local RF & Bluetooth links
433 MHz, 2.5GHz

Parasites internal devices (ABS)

Interference with mobile phone
900, 1800, 1900MHz

Similar EMC problems in aerospace
2. System Design Methodology for EMC

Obsolete Design Methodology

DESIGN

System on chip specification

Architectural Design

Design Entry Design Architect

FABRICATION

Version n°

EMC Measurements

Compliance ?

NO GO

GO

EMC compliant

+ 6 months

+ $$$$$$$$

January 20021 - IBIS Summit Santa Clara
2. System Design Methodology for EMC

Obsolete Design Methodology

PCB design
Prototype board
EMC scan

Electromagnetic incompatibility found too late
2. System Design Methodology for EMC

Target Design Methodology

- System on chip specification
- Training
- Architecture Guidelines
- Tools
- IC Models
- Architectural Design
- Design Entry Design Architect
- Design Guidelines
- EMC Simulations Compliance?
- EMC compliant

GO
2. System Design Methodology for EMC

Target Design Methodology

PCB design

- Wrong prediction of the radiated emission
- Good forecast of radiated emission

A core model is mandatory for accurate emission prediction

With IBIS

With IBIS and core model

A core model is mandatory for accurate emission prediction
3. The IERSET project

*European Research Centre on Electronics for Transportation*

identifies and co-ordinate co-operative research.

**Objectives**

- Definition and validation of a model to be used in PCB CAD tools to guarantee the EMC of electronic systems
- One model from 1MHz to 1GHz, for conducted *and* radiated emission
3. The IERSET project

ICEM (Integrated Circuit Electromagnetic Model)

Technical work at IERSET Toulouse, France

1997-2001

Draft standard
UTE
France

Draft standard
UTE
France

02/2001

ICEM Cookbook
version 1.c
aug. 2001

08/2001

Document on the UTE web www.ute-fr.com

UTE TEAM

Leader
PERRIN Jean Claude

HUET Claude

LEVANT Jean Luc

MAROT Christian

MAURICE Olivier

PERRAUD Richard

SAINTOT Pierre

SOUBEYRAN Amaury

SICARD Etienne

RAMDANI Mohamed

LUBINEAU Marc

TEXAS INSTRUMENTS

EADS AIRBUS

ATMEL

SIEMENS AUTOMOTIVE

VALEO

EADS CCR

ST MICROELECTRONICS

EADS MSI

INSA

ESEO

IERSET

Committee Draft for Voting at IEC

11/2001
3. The IERSET project

ICEM draft

Now draft technical report 93/146 CDV
3. The IERSET project

Presentations of ICEM

IBIS Munich 03/01
IBIS Mentor 09/01
IBIS DesignCon 01/02
IBIS Date Paris 04/02
IBIS East 10/02

Paper IEEE Pack

CEM Grenoble

EMC Europe

EMC compo Toulouse
4. Core Emission Model

Core noise of ICs: 3 modes of coupling

- **conducted**: Power lines, I/Os
- **radiated**: Direct

Origin of parasitic emission in CMOS: gate switching
4. Core Emission Model

ICEM includes a simple core model, not handled by IBIS

Basic parameters | Cd, Ib
---|---
Advanced param. | R,L,Cb
4. Core Emission Model

Parameter determination: several levels

- Simulations
- Measurements
- Estimation

Libraries
Tools
Measurement setup
Statistics
Standard technologies
Approximation

Before fabrication
After fabrication

\[ R \quad L \quad C \]

Equivalent
Current generator \( I_b \)
5. Emission Model with IOs

Add IBIS I/O data

Zsub: basically a 1-10Ω serial resistance
Cio : decoupling capacitance for IO supply
IO block: reuse of IBIS
5. Emission Model with IOs

Validation

IO modify the spectrum at high frequencies (>300MHz)
6. Adaptation of Emission Model

Case of multiple supply structure

Voltage Regulator

Separate supply for I/Os

Substrate impedance
7. Emission in TEM cell

Proposed model: capacitance & inductance coupling
7. Emission in TEM cell

Validation for the core alone

- Model fits correctly up to 400MHz
- At high frequencies, close from noise floor
7. Emission in TEM cell

Validation for the core & IOs

- Model fits correctly up to 800MHz
- At high frequencies, IO effects dominate
8. Implementation of ICEM in IBIS-ML

ICEM in IBIS-ML

- IBIS mark-up language (IBIS-X) makes ICEM implementation very easy
- IBIS-ML draft on the IBIS web site

```
[define model] ICEM
| on chip capa
| capacitor c_dec (vcc vss) C=5nF
| Serial supply resistor
| resistor r_vdd (vcc vcc_int) R=10
| resistor r_vss (vss vss_int) R=10
| current
Ib (vcc_int vss_int) I=It(TIME)
[It]
time I(typ)
0.0 0.3e-3
0.1e-9 0.3e-3
0.2e-9 0.5e-3
0.3e-9 0.8e-3
...
[end It]
[end define model] ICEM
```

Call of the user-defined model:

```
[begin header]
[ibis-ml version] 0.5
[filename] uC.ibs
[data] Nov 27, 2001
... 
```
9. Perspectives

- Interest in Susceptibility
- Extend model to higher frequencies (> 1 GHz)
Conclusion

- Technology scale down illustrated
- More complex chips increase parasitic emission
- An EMC model for ICs is mandatory
- A simple model has been proposed
- Satisfactory prediction of conducted emission
- Prediction of the core emission in TEM investigated
- Model proposal standardized by UTE (ICEM)
- Presentation and promotion to CAD & IC providers