The Bitter-Sweet Experiences of using IBIS Models
High-Speed Design Challenges

• On Board Data Rates
  - Commonly 133MHz - 500MHz; moving to 1GHz+

• Detailed Signal Integrity and Timing analysis required
  - Must simulate over Process, Voltage, and Temperature
  - Inter Symbol Interference
  - Simultaneous Switching Output Noise and Crosstalk
  - Pre-Layout Solution Space analysis
  - Post-Layout Verification

• Large number of simulations required
IBIS Benefits

• Performance
  – 10-100x faster than transistor level models

• Encapsulates large amount of information for
  – Waveform analysis
  – Timing Analysis
  – System Verification

• Can be as accurate as transistor level models

• No proprietary transistor level information
Generating good models is hard

- Requires significant effort
  - Correctly converting transistor level models to IBIS is a complicated process
  - Simulate transistor level and IBIS models into representative topologies
  - Review I-V and V-T data
  - Check results in different process corners
  - Various frequencies of operation

- Good models result in good correlation
Hspice vs. IBIS correlation

HSPICE vs. IBIS, data transition in first position.

HSPICE Result
IBIS Result

Stimulus

Time (lin) (TIME)
However...

- Effects not currently captured by IBIS models
  - Frequency dependent delays
  - Delay variation as a function of slew-rate
  - Signal amplitude delay variations
Delay Variations

IBIS
Rising vs. Falling Edge Delay Variation with Frequency

Frequency (MHz)

Delay (ns)

Rising
Falling
Delay Variations

HSPICE
Rising vs. Falling Edge Delay Variation with Frequency

Delay (ns)

500 250 166 125 100

Frequency (MHz)

Rising
Falling
Delay Variations, slow process

HSPICE vs. IBIS, data transition in fifth position.

- Stimulus
- HSPICE Result
- IBIS Result

Voltages (mV)
Time (ns)
Steps to Design Success using IBIS models

• I/O Characterization
  - Understand I/O behavior over operating conditions
• Model Qualification
• IBIS results need to be correlated to transistor level simulations
Conclusions

- Using IBIS models allows us to run a larger solution space analysis
- Creating good IBIS models requires significant effort
- Using IBIS for High-Speed Interfaces requires validated and correlated models
- In many cases IBIS models can be used for designing 600+ MHz interfaces