The Case Study of Board Simulation

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Digital Appliance of Panasonic

http://panasonic.jp/
AGENDA

1. The Status of JEITA EDA-WG
2. The Case Study of Board Simulation in Panasonic
3. The Issues of Board Simulation
4. Proposal to the IBIS-WG

Jan.27.2003
The Status of JEITA EDA-WG

JEITA is developing "EDA Standard Dictionary"

- Model circuit diagram, subcircuit node information, characteristics graph, verified simulator, ...
The Status of JEITA EDA-WG

Purpose of the "EDA Standard Dictionary"
- One category of ECALS dictionary (for EDI)
- Useful information for the components selection
- In order to perform simulation smoothly

EDA Standard Dict. → CAD tools → Simulator

Property → Simulation Model

.property_translation_byCadastroInterface
"EDA Standard Dictionary" is in a verification stage

- KYOCERA, Murata Manufacturing, TDK provided sample dictionaries
- Appliance maker evaluated and verified those dictionaries
- Feedback from appliance maker will be discussed at the EDA-WG
The Status of JEITA EDA-WG

"EDA Standard Dictionary" Development Schedule

- ECALS dict.
- EDA dict.
- Verification of the Property
- Discussion about verification feedback
- Confirmation
- Jan. 4.1 release
- Feb. Ver. 4.2 release
- Mar. or
- Apr. Ver. 5.1 release
- May
- June
- July
- Nov.

Jan. 27, 2003
Agenda

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Using Board Simulation for the Digital HDTV design

- **Aim:** Improvement of the picture quality
  Reduction of trial design
  Cost down

- **Approach:**
  - Direct connection of the digital picture stream data between the digital boards
    - Remove DAC/ADC from the board to board connection
  - Placement and route optimization of the LSI and RAMs
    - Smaller area, reduction of the trial
  - Improvement of the LSI

(http://panasonic.jp/tv/products/hi_vision/feature/picture.html)
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Summary of the simulation(1)
– Direct connection of the digital picture stream data

1. Extraction and Evaluation of the connector model
   - Extraction of the SPICE model
   - Evaluation of the design condition (trace length, impedance, series resistor, ...)
   - Crosstalk (connector pin assignment)

2. Floor Plan simulation by SPICE, IBIS

3. Evaluation of the simulation results
   - Evaluation of the accuracy
   - Power/GND Analysis

Next challenge

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Summary of the simulation (2)

- Placement and route optimization of the LSI and RAMs

- Optimization of the trace impedance
- Examination of the driver abilities
- Termination
- Crosstalk
- Signal Integrity

Expansion of the Rambus rules and make Panasonic rules

- 4 layers Rambus
- 6 layers smaller area (Achieve 60%)
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Background and issues

- Transient analysis is useful for the digital appliance
  - SI simulator or SPICE is useful
- S-parameter model is often supplied for High frequency (RF) components

Higher frequency digital = Using RF components

Time domain \( \xrightarrow{\times} \) Frequency domain

Freq. Domain model is not useful!
The Issues of Board Simulation

Approaches ... 2 types of approaches

− Using RF simulator
  ○ • S-parameter model can be used directly
  △ • Time domain module is often option (i.e. more cost)
  ✗ • IBIS, SPICE models cannot be used for ICs

− Translation S-parameter model to SPICE model
  ○ • Simulator can be used as it is (i.e. no more cost)
  ? • Translation accuracy Evaluation this time!
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Description of the translation

- Translation S-parameter to SPICE model
  - Using BroadBand Spice (Sigrity)

Read and check S-parameter → Extraction → Result Check

- Format checking
- Calculate DC value
- Choose types of export model
- Check waveforms
- Re-fitting if necessary

Execution of the extraction

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Extraction result (1)

Very good fitting result!
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Refinement example

Partial refinement is useful
(But need more study)
### HSPICE native format

* This is the subcircuit netlist generated by Broadband SPICE v1.0
* Port Number: 2.
* HSPICE compatible

```plaintext
.subckt L_Sample 1 2 ref
Rd1_1 3 ref 50
Rd1_2 4 ref 1
Vd1 1 3 0
F1 ref 4 Vd1 1.0
G1 ref 4 1 ref 0.02
Rd2_1 5 ref 50
Rd2_2 6 ref 1
Vd2 2 5 0
F2 ref 6 Vd2 1.0
G2 ref 6 2 ref 0.02

G3 ref 3 LAPLACE 4 ref
+ -4.21949495336101296e+016
+ -7.6924500349367864e+005
+ /
+ 8.0538254790796067e+019
+ 1.1053698816035342e+009
+ 1
```

### General SPICE format

* This is the subcircuit netlist generated by Broadband SPICE v1.0
* Port Number: 2.
* SPICE compatible

```plaintext
.subckt L_Sample 1 2 ref
Rd1_1 3 ref 50
Rd1_2 4 ref 1

L2_3_0 nl_1_2 nl_1_par0 2.61967344419533906e-008
C2_3_0 nl_1_par0 nl_1_0 4.7396975379644448e-013
R2_3_0 nl_1_par0 nl_1_0 1.9087178929704005e+003
L1_3_0 pl_1_2 pl_1_ser0 2.6735500391528587e+008
C1_3_0 pl_1_ser0 pl_1_ser0 4.644184516260152e-013
R1_3_0 pl_1_ser0 pl_1_0 2.9552616902395183e+001

L2_3_1 nl_1_2 nl_1_par1 2.4621677645809129e-007
C2_3_1 nl_1_par1 nl_1_0 6.6348538919814883e-014
R2_3_1 nl_1_par1 nl_1_0 4.8138425989128831e+004
L1_3_1 pl_1_2 pl_1_ser1 2.279066127104553e+007
C1_3_1 pl_1_ser1 pl_1_ser1 7.1679023177516205e-014
R1_3_1 pl_1_ser1 pl_1_0 7.1356522526650399e+001
```
Wrap up

- S-parameter model can be applied for time domain simulation

Expansion of the simulation case

- Examination of the accuracy would be necessary
  - S-parameter extracted conditions (frequency range, …)
  - Theoretical limitation
  - Characteristics of the components
The Case Study of Board Simulation

Next Step

- Expansion of the Model Extraction Environment
  - Although semiconductor component would be difficult, we would like to increase more types of passive components

- Construction of the simulation environment which can handle various model format
  - 1st step: Model translation … Simulate anyway!
  - 2nd step: More accuracy
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Requirement to the models (more accuracy)

- More useful 'variation' parameters
  - Min/Max is not for useful because those conditions are not likely on the board.
  - Practical 'variation' conditions, range (number of condition, e.g. typ1, typ2, or 10degree, 25degree, 40degree, 80degree, ...) would be necessary
  - 'variation' parameter of each production lot would be useful
Proposal to the IBIS-WG

Co-operation between IBIS-WG and JEITA EDA-WG to improve board simulation environment
- IBIS-WG: LSI, Package, module model accuracy
- JEITA EDA-WG: Feedback board simulation study result