Stacked Package Modeling with IBIS Version 4.1

Tom Dagostino and Bob Ross
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58 Pin IBIS Component Problem

• 58 pin 2 Gbit 128M X 16 SRAM memory consisting of eight stacked 54 pin TSOP 256 Mbit X 8 SRAM ICs addressed by layer-based chip selects

• 3-D metal interconnect strips (vertical, on 4 sides and horizontal layer routing) produce significant degradation
Photograph of Package
8 Stacked ICs, NC Pin Strips Bring Out 8 Chip-selected I/Os on 2 Pins

DQ4 DQ14
I/Os for Layer 8 (Red) Component and Layer 1 (Green) Component

DQ4

DQ14

Q NC

8
7
6
5
4
3
2
1

DQ4 DQ14
Ver. 4.1 Multi-lingual IBIS Model

- 8 – 58 pin [Component]s, one per active layer
  - I/Os and Inputs for that layer plus I/Os from layer +/- 4
  - Other inactive layer Inputs and I/Os hard coded as Terminators (so, one signal active per pin)
  - Choose [Component] for best and worst paths

- 240 node super-die interconnect structure to Inputs and I/O’s plus nodes to pins
  - Extracted lossy, coupled interconnect structure linked by [External Circuit] to SPICE & a [Circuit Call]

- Models set up as [External Circuit]s
  - But with vendor SPICE-based IBIS model links
Interconnect Extraction

- Vendor supplied bare package for T-lines
  - TDR for delays, impedances of strips
  - And measured dimensions
- Layout all buffers and layers in HyperLynx with T-lines and dimensions
- Export lossy, coupled interconnect into HSpice formatted subcircuit
IBIS Buffer Models

• Single IC supplied separately and fully modeled as an independent IBIS file with [Component] and [Model]s
  – I/O buffers
  – Input buffers
  – Package – (default package added to code for models)

• Construct huge multi-lingual IBIS model file
  – Passed Beta ibischk4 Version 4.1
  – Eight internal layer [Component]s
Results

• No tool can simulate multi-lingual model
  – Vendor-specific SPICE used (could have used Berkeley SPICE for interconnect)
  – [External Circuit] buffers with SPICE-based IBIS calls do not work (and direct table links not legal)
  – No Model_type information for automatic processing
  – Cannot bring in total simulation net

• HyperLynx simulation by hard coded buffer selection – cannot be used as component on larger board
  – But did simulate with expected interconnect degradation in about 20 seconds per buffer
Alternative Approaches

- **EBD**
  - No coupling (50% too fast), but Terminator stubs not needed
- **Vendor-specific pseudo board from electrical information**
  - Not tried because not acceptable to chip vendor
- **ICM**
  - No links to IBIS, no support and more complicated
- **No other vendor-specific solution worked**
  - [Circuit Call] to IBIS [Model] links – configuration issues
  - Spice-based net with IBIS calls – syntax issues
Multi-lingual Issues

- Multi-lingual for interconnect and *-AMS models
  - Solution for encoding IBIS models directly
  - Forces *-AMS code, but limited *-AMS tool support, plus vendor-specific configuration issues
  - Requires Bi-directional models with driving and receiving modes
Cannot be Solved by IBIS Unless …

- Direct IBIS table links to [Model] and [External Model]
  - Expanded [Circuit Call] or new [Model Call]?

- Some power-rail issues
  - Can Input or Terminator model have inactive $A_{\text{puref}}$ and $A_{\text{pdref}}$ nodes? (OK in standard IBIS)

- How to selectively bring in partial or full interconnect structure
  - EDA tool issue

- On-die chip select
  - Limitation overcome by using several [Component]s