BIRD95: Power Integrity Validation using HSPICE

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Agenda

- History of Power Integrity simulations with IBIS
- Summary of Problems with current IBIS Models in Power Integrity simulations
- **BIRD95** Proposal
- Implementation and correlation of BIRD95 using HSPICE
- Conclusions
The Challenge
DesignCon2004 PDN Panel

• **DesignCon2004 PDN Panel:**

  Sergio Camero (Cisco Systems, Inc) and Istvan Novak (SUN Microsystems) challenged the EDA / Modeling Industry to solve **Power Integrity Analysis** through accurate modeling and simulation

• **DesignCon2004 PDN Simulation Panel proceedings and materials**

  http://home.att.net/~istvan.novak/papers.html
Brief History

- **Goal:** leverage the good work already done by many experts within IBIS and IEC

- **BIRD42.3** was revisited in terms of IvsT tables
  
  **Many thanks to all those who had initiated this proposal**

- **ICEM (Integrated Circuits Electrical Model) – IEC62014-3**
  
  [http://www.ic-emc.org](http://www.ic-emc.org)
  
  “..I would be pleased to attend an IBIS committee meeting to illustrate and explain our work…”
  
  - Etienne SICARD, INSA, Jan25th 2005

- **Various discussion continued with IBIS forum.**
  

- **BIRD95** was proposed by Cisco Systems, Inc on Dec13th 2004

- **BIRD95.1** was revised Jan28th, 2005
The Proposal – **BIRD95**

- **BIRD95** - Power Integrity Analysis using IBIS
- Task#1
  
  Solve the SSN simulation challenge using lvsT
- Task#2
  
  Connect to the Core model using ICEM
Major components of BIRD95

- Core region
- I/O region
- Package

Components:
- ICEM
- ICM
- IvsT
- GND
- pwr

ICM or EBD or .pkg
Validation using HSPICE

- Part-II
Summary of Problems with Current IBIS Model in Power Integrity simulations

- Pre-drive current is completely ignored
- On-die parasitic capacitance between power and ground is not included
- X-bar current is completely ignored, or not correctly modeled
- Existing IBIS SSN simulation could either over- or under- estimate the power noise
**BIRD95 Proposal**

Note: Encrypted circuit model could include elements shown in the dashed box (black box). All info in BIRD95 is extracted from this black box through VDDQ, I/O and GND pins. Internal details are not needed.
Definition of IvsT and Z_VDDQ

- IvsT is the total current from the VDDQ which is connected to ideal DC voltage source
- There are total 6 IvsT tables (3 different I/O loadings associated with rising/falling edges)
- Z_VDDQ is the frequency-dependent impedance derived with the correct DC voltage applied at VDDQ pin and open-load condition
- Z_VDDQ information is proposed to be provided through ICM model
Implementation and Correlation of BIRD95 in HSPICE

- Simulation description
- Evidence of the problems with current IBIS model (Ideal Power Supply case)
- \textbf{BIRD95} implementation schematics
- Results with added \textit{IvsT} (I versus T)
- Results with added \textit{IvsT} and \textit{Z_Vddq}
Simulations description

- An impedance-controlled 1.8V HSTL output buffer is used as an example
- IBIS model is extracted from HSPICE transistor model
- Both Ideal and Non-ideal power supply cases are analyzed
- HSPICE B-element is used to simulate the IBIS model
- **BIRD95** lvsT info is implemented with ideal current source in parallel with B-element
- Both cases with and w/o Z_VDDQ are analyzed
Evidence of the Problems with Current IBIS Model: I/O Voltage (Ideal Power Supply)

R\textsubscript{fixture}=50, V\textsubscript{fixture}=1.8V, Rising

R\textsubscript{fixture}=50, V\textsubscript{fixture}=1.8V, Falling

- Pad Voltage from Transistor model
- Pad Voltage from IBIS model
Evidence of the Problems with Existing IBIS Model: Total Current from Power Pin (Ideal Power Supply) (1)
Evidence of the Problems with Existing IBIS Model:
Total Current from Power Pin (Ideal Power Supply) (2)

R_{fixure}=50, V_{fixure}=0V, Rising

Total Current from Transistor model
Total Current from IBIS model

R_{fixure}=50, V_{fixure}=0V, Falling

Total Current from Transistor model
Total Current from IBIS model
Evidence of the Problems with Existing IBIS Model: Total Current from Power Pin (Ideal Power Supply) (3)
**BIRD95** implementation schematics

Case 1: B-element only  
Case 2: B + IvsT*  
Case 3: B+IvsT*+Z_VDDQ

Note: IvsT* is different with IvsT table in BIRD95, but it is derived from IvsT table
lvsT* and parasitic components

- \( lvsT^* = lvsT \) (\textit{BIRD95} table) - \( lvsT^{**} \)
- \( lvsT^{**} \) is the total current from the VDDQ by using existing IBIS model with Z_VDDQ connected in parallel.
- All currents here are under ideal power supply and standard loading conditions.
- Two sets of \( lvsT^* \) associated with rising and falling edge were derived by averaging different loading conditions in our examples. More complicated model could be derived from 6 \( lvsT^* \) tables to compensate the load variation effects.
- ESR, ESL, C and R_dc can be extracted from Z_VDDQ to match the impedance in frequency domain.
- The ESR, ESL, C and R_dc is just one example of the possible circuits to match Z_VDDQ. It could cover majority I/O buffers’ on-die parasitic components.
Total Current from VDDQ pin

R\textsubscript{fixure}=50, V\textsubscript{fixure}=1.8V, Rising

- Total Current from Transistor model
- Total Current from IBIS model
- Total Current from IBIS+I\textupsilon\textsubscript{S}T model
- Total Current from IBIS+I\textupsilon\textsubscript{S}T+Z\_VDDQ

R\textsubscript{fixure}=50, V\textsubscript{fixure}=1.8V, Falling

- Total Current from Transistor model
- Total Current from IBIS model
- Total Current from IBIS+I\textupsilon\textsubscript{S}T model
- Total Current from IBIS+I\textupsilon\textsubscript{S}T+Z\_VDDQ
Total Current from VDDQ pin (cont’d)

- **R\textsubscript{fixture}=50, V\textsubscript{fixture}=0V, Rising**
  - Blue: Total Current from Transistor model
  - Black: Total Current from IBIS model
  - Green: Total Current from IBIS+IvsT model
  - Red: Total Current from IBIS+IvsT+Z\_VDDQ

- **R\textsubscript{fixture}=50, V\textsubscript{fixture}=0V, Falling**
  - Blue: Total Current from Transistor model
  - Black: Total Current from IBIS model
  - Green: Total Current from IBIS+IvsT model
  - Red: Total Current from IBIS+IvsT+Z\_VDDQ
Total Current from VDDQ pin (cont’d)
Voltage Noise at VDDQ Pin (cont’d)
Voltage Noise at VDDQ Pin (cont’d)
Voltage at Signal Pin

R\_fixture=50, V\_fixture=1.8V, Rising

R\_fixture=50, V\_fixture=1.8V, Falling

- Pad Voltage from Transistor model
- Pad Voltage from IBIS model
- Pad Voltage from IBIS+lvst model
- Pad Voltage from IBIS+lvst+Z\_VDDQ
Voltage at Signal Pin (cont’d)

R\textsubscript{_fixure}=50, V\textsubscript{_fixure}=0V, Rising

R\textsubscript{_fixure}=50, V\textsubscript{_fixure}=0V, Falling

- Pad Voltage from Transistor model
- Pad Voltage from IBIS model
- Pad Voltage from IBIS lvst model
- Pad Voltage from IBIS+lvst+Z\_VDDQ
Voltage at Signal Pin (cont’d)
Conclusions

- **BIRD95** can be easily implemented in HSPICE and other EDA tools.
- **BIRD95** can greatly improve the simulation accuracy of power noise in SSN and other non-ideal power supply simulations with IBIS models.
- On-die Impedance between the power and ground is very important in power related simulations.
- **BIRD95** provides a feasible solution to evaluate the power noise impact on signal timing.
Questions and Answers
Empowering the Internet Generation