IBIS Power/Ground Modeling of LSI Core Logic with High-Pin Count Package for EMI and PI

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Norio Matsui*, Hiroshi Wabuka**, Dileep Divekar*, Neven Orhanovic*

*Applied Simulation Technology, Inc.
**NEC Production Technology Laboratories
Outlines

1. Introduction
2. Modeling of Core Logic Power/Ground for EMI Simulation
3. Modeling of High-Pin Count Package
4. Conclusion
1. Introduction
Power Integrity

Electromagnetic Interference

## Two Types of LSIs

**LSI for Digital Consumer/Auto Mobile**

<table>
<thead>
<tr>
<th></th>
<th>Total Power/Current</th>
<th>Clock Freq</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core Logic</td>
<td>High</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>I/O</td>
<td>Low</td>
<td>Low</td>
<td>High</td>
</tr>
</tbody>
</table>

**Driver IC**

<table>
<thead>
<tr>
<th></th>
<th>Total Power/Current</th>
<th>Clock Freq</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core Logic</td>
<td>Low</td>
<td>Same/High</td>
<td>Low</td>
</tr>
<tr>
<td>I/O</td>
<td>High</td>
<td>Low</td>
<td>High</td>
</tr>
</tbody>
</table>
Dominant Currents

Core Logic

I/O

EMI

Power/Ground Bounce

SSO (Simultaneous Switching Output Noise)
EMC in Digital Consumer Electronics

- EMI by Core Logic
- ESD by Floating Ground
- SSO by I/O
- Power/Ground Coupling in Mixed Mode Modules
Non-Ideal Ground at Various Levels

- LSI (Core / IO)
- Package/Module
- Flexible/Rigid Printed Circuit Boards
- Connectors / Cables

Complex Power/Ground Phenomena

Simulators

Well-Balanced Model
2. Modeling of Core Logic Power/Ground for EMI Simulation
# System LSI for Digital Consumer Electronics

<table>
<thead>
<tr>
<th></th>
<th>Voltage</th>
<th>Current</th>
<th>Clock Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Core Logic</strong></td>
<td>1.2V</td>
<td>2.5A</td>
<td>96MHz</td>
</tr>
<tr>
<td></td>
<td>1.8V</td>
<td>0.2A</td>
<td>96MHz</td>
</tr>
<tr>
<td></td>
<td>2.5V</td>
<td>0.5A</td>
<td>96MHz</td>
</tr>
<tr>
<td><strong>I/O</strong></td>
<td>3.3V</td>
<td>0.3A</td>
<td>48MHz</td>
</tr>
</tbody>
</table>

Methods of Extraction of Core Logic Model for EMI

By Measurement

By CAD

Three Types of Core Logic Model for EMI

- Macro Model using Transistors (Time Domain)
- Current Waveforms (+ Nonlinear Admittance) Model (Time Domain)
- Complex Current Frequency Spectrum (+ Linearized Admittance) Model (Frequency Domain)
- + Power/Ground Pattern on Chip and Package Model
EMI Simulation using Frequency Domain Model

Equivalent Circuit in Frequency Domain

Core Logic Current

frequency

Power/Ground Pattern Impedance

frequency

Current Distribution

LSI Power Grid Model

<table>
<thead>
<tr>
<th>Freq</th>
<th>I(real)</th>
<th>I(imag)</th>
</tr>
</thead>
<tbody>
<tr>
<td>96MHz</td>
<td>40mA</td>
<td>-50uA</td>
</tr>
<tr>
<td>192MHz</td>
<td>80mA</td>
<td>200uA</td>
</tr>
<tr>
<td>288MHz</td>
<td>30mA</td>
<td>-5mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Electric Field

freq

freq

EMI Simulation using Time Domain Model

Equivalent Circuit in Time Domain
(Current waveforms are not necessary:
Just switch Model between Voltage Source)

Equivalent Circuit of Power and Ground Patterns in Time Domain
with Location Information of PCB

Current Distribution
(not current waveforms)
Accuracy

Simulation vs. Measurement

dBuA vs. MHz
3. Modeling of High-Pin Count Package
Advanced IC Packages

- BGA/CSP (Bonding Wire)
- BGA/CSP (Flip Chip)
- SIP

Bonding Wires and Balls

Reference Ground

Flip Chip/Ball Pad

Coupling

Reference Ground

Pad on a chip/substrate

Pad on a substrate/PCB

A Problem in IBIS IC Package Model

No Models of Power/Ground Pins

Only lead frame type package

Too Huge Model for Arbitrary Shape Power/Ground

Patterns with Many Pins
  Partial Models

Too complex to use for time domain analysis

Isolated Model from PCB and/or LSI chip
  (Some case needs to merge CAD DB)
Non-Ideal Power/Ground Needs ICM/IBIS 4.1

More than Two Terminals

Ball Pads

Bonding Pads

Ball Pads

Bonding Pads
Meshing Power and Ground
Three Types of Model Order Reduction (MOR)

Circuit Conversion

- Circuit Compression
- Frequency Fitting
- Frequency Table
• Three Types of Model Order Reduction (MOR)

Circuit
Direct
Compression

Frequency
Fitting

Frequency Table
(SPICE IFFT)
## Comparison of MOR

<table>
<thead>
<tr>
<th></th>
<th>Circuit Direct Compression</th>
<th>Frequency Fitting</th>
<th>Frequency Table</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Input Data</strong></td>
<td>Lumped Elements with no frequency dependency</td>
<td>N-port Parameters (by Measurement or Field Solver, Linear Elements with frequency dependency)</td>
<td></td>
</tr>
<tr>
<td><strong>Output Data</strong></td>
<td>G-element, Segmented Lumped Elements</td>
<td>G-element (Polynomial)</td>
<td>G-element (Frequency Table)</td>
</tr>
<tr>
<td><strong>Stability with Nonlinear Devices in Time Domain</strong></td>
<td>Stable Fast</td>
<td>Unstable/Stable Fast</td>
<td>Unstable / Slow Stable needs huge data points</td>
</tr>
<tr>
<td><strong>Applications</strong></td>
<td>Need Circuit Data</td>
<td>Short Structure Few Resonance</td>
<td>Long Structure Many Resonance</td>
</tr>
</tbody>
</table>
Needs Huge Computation to Make a Macro Model for High-Pin Count Power/Ground Patterns

Double step MOR

Cell (I, J)
Each Cell model by MOR by Parallel Processing
+ Whole model by MOR
## Double Step MOR

<table>
<thead>
<tr>
<th></th>
<th>Modeling</th>
<th>Model Size</th>
<th>Accuracy</th>
<th>Modeling Time</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Cell Level</td>
<td>PEEC</td>
<td>Too Large</td>
<td>highest</td>
<td>Memory Overflow</td>
</tr>
<tr>
<td>2</td>
<td>PEEC</td>
<td>Whole Level</td>
<td>Too Large</td>
<td>high</td>
<td>Medium</td>
</tr>
<tr>
<td>3</td>
<td>Circuit Compression</td>
<td>Whole Level</td>
<td>Large</td>
<td>high</td>
<td>Long</td>
</tr>
<tr>
<td>4</td>
<td>Circuit Compression</td>
<td>Circuit Compression</td>
<td>Small</td>
<td>low</td>
<td>Long</td>
</tr>
<tr>
<td>5</td>
<td>Circuit Compression</td>
<td>N-port Parameter Fitting</td>
<td>Small</td>
<td>medium</td>
<td>Long</td>
</tr>
</tbody>
</table>

Impedance between Power and Ground

Along the same net

Between the different nets
Still Needs a Smaller Model in Time Domain

- Power/Ground has many pins
- Individual Pin Model with coupling easily reaches MB in any format.

- Log Model Size
  - Accurate
  - Coupling
  - Bandwidth
  - Frequency
  - Stability
  - Separation from Signals

Log Number of Pin Counts
Grouping of closely located Pins may be needed

Original

Grouping

Rebuilt (Final)

Choice of Formats

**IBIS 4.1 / ICM 1.0 Formats**

- **S-parameters**
- **Lumped SPICE Networks**
- **Coupled Transmission Line Networks**

**Applications**

- **Time Domain**
- **Frequency Domain**
4. Conclusion

Simple is best / Well-balanced Model

Different Models for SSO/Bounce/EMI