IBIS Interconnect BIRD

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Overview

- IBIS Interconnect Task Group
- Models Represent Package and On-Die Interconnect
- On Die, Package, Supply and Signal Interconnect can be Combines or Kept Separate
- Similar Approach for Both IBIS and EBD
- Pre and Post Layout IBIS Files
- IBIS Interconnect Model Terminals
- Differential Signal (I/O) Model Terminals
- Supply Model Terminals
- Post Layout Combined Package and On-Die Models
- Post Layout Separate Package and On-Die Models
- Pre Layout Combined Package and On-Die Models
- Graphics Showing Model Terminals
- Corners
- Reconciling Legacy IBIS Models and [External Model]
- Other issue to discuss/resolve
- Next Steps
IBIS Interconnect Task Group

• Meets Wednesdays 8AM PDT
• http://www.eda.org/ibis/interconnect_wip/
• Major Contributors
  – Altera
  – Cadence Design Systems
  – Intel Corp
  – Keysight Technologies
  – Mentor Graphics
  – Micron Technology
  – Signal Integrity Software
  – Synopsys
  – Teraspeed Labs
  – David Banas
  – Bradley Brim
  – Michael Mirmak
  – Radek Biernacki
  – Arpad Muranyi
  – Justin Butterfield, Randy Wolff
  – Walter Katz
  – Rita Horner
  – Bob Ross
Models Represent Package and On-Die Interconnect

• Languages Supported
  – IBIS-ISS
  – Touchstone

• Model Terminals
  – Pins
  – Die Pads
  – Buffer Signals
  – Buffer Supplies
On Die, Package, Supply and Signal Interconnect can be Combined or Kept Separate

- Supports separate on-die and package interconnect models and combined on-die and package interconnect models
- Independent Supply and Signal Interconnect Models
- Coupled Supply and Signal Interconnect Models
- Singled Ended and Differential Interconnect Models
Similar Approach for Both IBIS and EBD

- IBIS (.ibs) Interconnect Model Terminals
  - Pins ([Pins])
  - Die Pads
  - Buffers
- EBD (.ebd) Interconnect Model Terminals
  - Pins ([Pin List])
  - reference_designator.pin
  - Enhancing EBD will be a separate BIRD based on the IBIS interconnect model BIRD when completed
  - May be a new section Electronic Module Description (EMD) instead of enhancing EBD
IBIS Interconnect Model Terminals

• Pins
• Die Pads
  – Signal (I/O)
  – Supply (POWER and GND)
• Buffers
  – Signal (I/O)
  – Supply
    • Pullup Reference
    • Pulldown Reference
    • Power Clamp Reference
    • Ground Clamp Reference
    • External Reference
Pre and Post Layout IBIS Files

- **Post Layout**
  - **Signal (I/O) Terminals**
    - Pin, Die Pad and Buffer terminals referenced by Pin_name
  - **Supply Terminals**
    - Pin terminals referenced by Pin_name or Signal_name
    - Die Pad terminals referenced by Die_Pad_name or Signal_name
    - Buffer terminals referenced by Pin_name or Signal_name

- **Pre Layout**
  - **Signal (I/O) Terminals**
    - Referenced by Model_name
  - **Supply Terminals**
    - Referenced by Signal_name
Interconnect Model Examples

[Interconnect Model]  A1  |  Post Layout Interconnect Model
File_TS  A1.s2p
Number_of_Terminals 3
Terminal 1 Pin_A_signal  A1
Terminal 2 A_signal  A1
[End Interconnect Model]

[Interconnect Model]  DQ  |  Pre Layout Interconnect Model
File_ISS  DQ.iss  DQ
Param Length .1 .05 .15
Number_of_Terminals 2
Terminal 1 Pin_A_signal  DQ Model_name
Terminal 2 A_signal  DQ Model_name
[End Interconnect Model]
Interconnect Model Terminals

- Terminal <terminal number> <At Pin|DiePad|Buffer> <ID> <What ID is>
- One line per terminal
- Supports both Pre and Post Layout
- Example Signal (I/O) Terminal records
  - Post Layout
    - Terminal 1 Pin_A_signal M8
    - Terminal 2 Pad_A_signal M8
    - Terminal 3 A_signal M8
  - Pre Layout
    - Terminal 1 Pin_A_signal DQ Model_name
    - Terminal 2 Pad_A_signal DQ Model_name
    - Terminal 3 A_signal DQ Model_name
Differential Signal (I/O) Model Terminals

- Post Layout
  - Terminal 1 Pin_A_signal  M8
  - Terminal 2 Pin_A_signal  M7
  - Terminal 3 Pad_A_signal  M8
  - Terminal 4 Pad_A_signal  M7
  - Terminal 5 A_signal  M8
  - Terminal 6 A_signal  M7

- Pre Layout
  - Terminal 1 Pin_A_signal_pos  DQS Model_name
  - Terminal 2 Pin_A_signal_neg  DQS Model_name
  - Terminal 3 Pad_A_signal_pos  DQS Model_name
  - Terminal 4 Pad_A_signal_neg  DQS Model_name
  - Terminal 5 A_signal_pos  DQS Model_name
  - Terminal 6 A_signal_neg  DQS Model_name
Supply Model Terminals

- Post Layout
  - Using Pins, Pads and Buffers
    • Terminal 1 Pin_A_Signal B1
    • Terminal 2 Pin_A_Signal B2
    • Terminal 4 A_puref M3
  - Using Signal_name and Buffers
    • Terminal 1 Pin_A_Signal VDD Signal_name
    • Terminal 3 A_puref M3

- Pre and Post Layout
  - Using Signal_name and “Pin mapping”
    • Terminal 1 Pin_A_Signal VDD Signal_name
    • Terminal 3 A_Signal VDD Signal_name
  - Using Signal_name and “Model_name”
    • Terminal 1 Pin_A_Signal VDD Signal_name
    • Terminal 3 A_puref DQ Model_name
Package Terminals
Post Layout

A_puref A1

Pullup

Power Clamp

A_pcref A1

A_gcref A1

A_pdref A1

Combined Package and On-Die Model

Pin_A_Signal B3

Pin_A_Signal B4

Pin_A_Signal A1

Pin_Signal_Name VSSQ

Pin_Signal_Name VSS
Package Terminals
Pre Layout

Combined Package and On-Die Model

- Pullup
- Power Clamp
- Pulldown
- Ground Clamp

A_Signal_name
VDD

A_Signal_name
VDDQ

A_Signal_name
DQ

A_Signal_name
VSSQ

A_Signal_name
VSS

Pin_Signal_name
VDD

Pin_Signal_name
VDDQ

Pin_A_signal
DQ

Pin_Signal_name
VSSQ

Pin_Signal_name
VSS
Parameters can have either a single value or three corner values

It is not clear if we will have a clear definition of the three corners Typ, Min, Max

- If a parameter is a length then Typ, Fast, Slow
- If a parameter is a delay then Typ, Slow, Fast
- If a parameter is an impedance then Typ, Min, Max

Expect it will inherit the existing usage of Typ, Min and Max and will be up to EDA tool on how to apply these corners.

Some “Corner” conditions (e.g. crosstalk) will be handled by [Interconnect Model Selector].
Reconciling Legacy IBIS Models and [External Model]

• [External Model] supports an A_extref terminal which has no analog in legacy models (models that use the IV).
• If a new interconnect models has a terminal to an [External Model] A_extref, how should the EDA tool terminate this terminal when using a legacy model?
Other issue to discuss/resolve

- Reconciling [External Circuit] with new interconnect models
- Reconciling global reference node “0”, “A_Gnd” and “Gnd” with both IBIS models and new interconnect models.
Next Steps

• The goal is to complete the new interconnect model BIRD and formally submit it to the Open Forum by mid Q2, 2015
• Shortly thereafter with a BIRD to enhance EBD to support IBIS-ISS subckts.