WHAT CAN’T IBIS DO?

Michael Mirmak, DCPAE (michael.mirmak@intel.com)
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Agenda

What IBIS Can Do (IBIS Coverage Today)

- The Three Areas of IBIS Coverage

Where Expansion is Needed

- Complex Impedances
- Feedback Support
- Improved Evaluation Criteria

Nice to Haves

- Executable Checking, or Golden Response to Golden Stimuli

Discussion
WHAT IBIS CAN DO
The Three Areas of IBIS Coverage

I/O buffers

- Traditional IBIS core: I-V, V-t, C_comp
- Multi-lingual code
- AMI

Packages

Evaluation criteria

- Input logic thresholds, etc.
WHAT IBIS CAN’T DO
Four Areas for Expansion

The major missing parts of IBIS:

- Advanced Packages – not discussed here, as was covered as part of Interconnect updates
- Complex Impedances
- Feedback Support
- Evaluation Criteria

Other advancements are under active development and not mentioned here:

- Improved references (GND treatment)
- Backchannel adaptive equalization
Complex Impedances

How do you represent an AC load (e.g., a complex impedance) in traditional IBIS?

- Behavior shows up in both memory (single-ended) and serial-differential buffers
- Needed for both drivers and receivers
- Ideally frequency- and voltage (state) dependent

Serial-differential buffer single-ended pad impedance plot of C (F) vs. F (Hz) and V (volts)
Model_Type Terminator Is Not Enough

For complex impedances, \([R_{ac}]\) and \([C_{ac}]\) are available, but require use of Model_type Terminator

Terminator limits the use of other IBIS features

- Input only, but with no input thresholds
- \([\text{Ramp}]\) and \([\ldots\ \text{Waveform}]\) are therefore prohibited
- Prohibited with [Algorithmic Model]

“When \([R_{gnd}], [R_{power}], \text{or } [R_{ac}] \text{ and } [C_{ac}]\) are specified, the Model_type must be Terminator.”
Proposals and Challenges

Randy Wolff summarized a proposed treatment from ATM and Interconnect

- "Improved C_comp Model Case Study", IBIS Summit at DesignCon 2015
- ISS-based subcircuit

Tricky points

- De-embedding for impedance in V-t, Ramp behaviors
- Separating “C_comp” from interconnect effects
- Accounting for state-dependence
- Measurement/correlation (separation from interconnect, rail effects)
Feedback

Traditional IBIS is a “snapshot”
- I-V data is non-transient, at a given state
- Ramp, V-t data cover state transitions, but with simplified relationship to I-V assumed (2EQ/2UK K-tables)

Approach breaks down if Miller capacitances are large
- Internal capacitance is sometimes added to deliberately slow down output edges for “fast” buffers used on “slow” interfaces

Problem part of 2EQ/2UK approach
- L. Giacotto, A. Muranyi, “A VHDL-AMS buffer model using IBIS v3.2 data” IBIS Summit at DAC 2003

Proposal for 3D surface macromodel treatment in:
- G. Signorini, “Enhanced Macromodels for I/O Buffers”, IBIS Summit at EPEPS 2015 (also EPEPS paper)

Can we update IBIS [Model] core to include 3D surface approach?

Additional capacitance is deliberate here – see notes
Miller capacitance also exists but is effectively ignored in 2EQ/2UK K-table approach
Evaluation Criteria
What is the “goodness” of a signal (at the pad, pin, etc.)?

Supported criteria include:

- Vih, Vil and variants to support hysteresis, DDR, etc.
- Included in [Model], [Model Spec], [Receiver Thresholds]

What’s missing? Serial-Differential Eye Support

- Eye height, width, shape requirements
- Eye contour as function of BER (e.g., eye mask at target BER)
- Bathtub curves?

Eye masks have been proposed several times in the past:


Need BER-based eye masks at various measurement points
A “Nice to Have”: Algorithmic Checking

The IBISCHK parser checks .ibs (and related) file syntax

No method exists to check algorithmic models in a standardized way

Proposal: “golden input” and “golden output” definitions, similar to [Test Data]

- Optional, additional keywords (and files)
- Golden input: waveform data and configuration information
- Golden output: modified waveform data and parameters

Initial DLL checks proposed in IBIS Quality

- M. LaBonte, *IBISCHK Checks for IBIS-AMI DLL Integrity*
- Covers basic architecture, return value, and symbol table checks

Parser DLL checks should be implemented with Golden Input/Output option
DISCUSSION
BACKUP
from L. Giacotto, A. Muranyi, “A VHDL-AMS buffer model using IBIS v3.2 data” IBIS Summit at DAC 2003

Vwfm1(t) and Vwfm2(t) are transitions in the same direction but using different V, R, loads