EMD Made Simple

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Key Points

- **Electrical Module Description (EMD) in BIRD202**
- **Interfaces (and pin_names)**
  - [EMD Pin List] Interface (external pin_name connections)
  - [Designator Pin List] Interfaces (pin_names for attached IBIS components or EMD modules)
- **Terminals and terminal lines**
  - Pin_I/O (pin_name)
  - Pin_Rail (pin_name, bus_label, signal_name)
  - Merged Pin_Rail terminals by bus_label or signal_name on ONE interface only
- **Pin_I/O association** by signal_name for different interfaces
- **Electrical connections** (IBIS-ISS and Touchstone formats)
- **[EMD Model], [EMD Set], [EMD Group] hierarchy**

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EMD Pin Interfaces

- [EMD Pin List]
  - External interface pins

- [Designator Pin List]
  - Component or Module interface pins

Red lines show physical (electrical) connections

- [EMD Designator Map]
  - Assigns designators (e.g., U1 ... U4)
  - Like [Reference Designator Map] in EBD

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## EMD Pin List

<table>
<thead>
<tr>
<th>[EMD Pin List]</th>
<th>signal_name</th>
<th>signal_type</th>
<th>bus_label</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O Pins</td>
<td></td>
<td>(NO signal_type bus_label)</td>
<td></td>
</tr>
<tr>
<td>C5</td>
<td>DQ0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C6</td>
<td>DQ1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>...</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rail (supply)</td>
<td>Pins</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A3</td>
<td>VSS</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>A4</td>
<td>VDD</td>
<td>POWER</td>
<td></td>
</tr>
<tr>
<td>A5</td>
<td>VSS</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>B3</td>
<td>VDD</td>
<td>POWER</td>
<td>VDDU1</td>
</tr>
<tr>
<td>B4</td>
<td>VDD</td>
<td>POWER</td>
<td>VDDU2</td>
</tr>
<tr>
<td>C4</td>
<td>VDD</td>
<td>POWER</td>
<td></td>
</tr>
<tr>
<td>...</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[End EMD Pin List]

*pin_name, signal_name entries match data sheet names*

*bus_label entries can be assigned based on physical layout*

*Missing bus_label entry defaults to signal_name entry*
### [EMD Designator Map]

<table>
<thead>
<tr>
<th>designator_name</th>
<th>file_reference</th>
<th>component/module</th>
</tr>
</thead>
<tbody>
<tr>
<td>U1</td>
<td>mem.ibs</td>
<td>memory</td>
</tr>
<tr>
<td>U2</td>
<td>mem.ibs</td>
<td>memory</td>
</tr>
<tr>
<td>U3</td>
<td>mem_mod_emd</td>
<td>memory_module</td>
</tr>
<tr>
<td>U4</td>
<td>mem_mod_emd</td>
<td>memory_module</td>
</tr>
</tbody>
</table>

[End EMD Designator Map]

**EBD files are not supported**

Similar format as [Reference Designator Map]
### Designator Pin List

#### (I/O Pins)

<table>
<thead>
<tr>
<th>I/O Pins</th>
<th>signal_name</th>
<th>signal_type</th>
<th>bus_label</th>
</tr>
</thead>
<tbody>
<tr>
<td>U1.11</td>
<td>DQ0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>U1.12</td>
<td>DQ1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>U2.11</td>
<td>DQ0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>U2.12</td>
<td>DQ1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>U3.5</td>
<td>DQ0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>U3.6</td>
<td>DQ1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>U4.5</td>
<td>DQ0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>U4.6</td>
<td>DQ1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Designator pin_names are `<designator>.<pin_name>`

Listed pin_names match those for the Uxy devices

signal_name entries entered for associated paths

(Interconnect Modeling format uses same pin_name entries)
### Designator Pin List
(Rails or Supply Pins)

<table>
<thead>
<tr>
<th>Designator Pin List</th>
<th>signal_name</th>
<th>signal_type</th>
<th>bus_label</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rail (Supply) Pins</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>U1.9</td>
<td>VSS</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>U1.10</td>
<td>VDD</td>
<td>POWER</td>
<td></td>
</tr>
<tr>
<td>U1.20</td>
<td>VDD</td>
<td>POWER</td>
<td>VDD_U1</td>
</tr>
<tr>
<td>U2.9</td>
<td>VSS</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>U2.10</td>
<td>VDD</td>
<td>POWER</td>
<td></td>
</tr>
<tr>
<td>U2.20</td>
<td>VDD</td>
<td>POWER</td>
<td>VDD_U2</td>
</tr>
<tr>
<td>U3.9</td>
<td>VSS</td>
<td>GND</td>
<td></td>
</tr>
</tbody>
</table>

| ... Etc. |

[End Designator Pin List]
Name Assignments

- **[EMD Pin List]**
  - *pin_names* and *signal_names*: data sheet values
  - *bus_labels*: from EMD modeler for physical subgroups of rails

- **[Designator Pin List]**
  - *pin_names*: data sheet for actual designator part (often the pinout is based on a JEDEC standard)
  - *signal_names*: from EMD modeler to show associations
    - *signal_names* can differ from those of the designator part
    - Identical *signal_names* on the designator part should be mapped to identical *signal_names* assigned by the EMD modeler
  - *bus_labels*: by EMD modeler as needed for rail *signal_name* physical grouping (e.g., U1, U2 groups for VDD)
Terminal_line and Terminal Type Associations for EMD Models

<Terminal_number> <Terminal_type> <Terminal_type_qualifier> <Qualifier_entry> [Aggressor_Only]

<table>
<thead>
<tr>
<th>Terminal_type</th>
<th>Terminal_type_qualifier</th>
<th>Aggressor_Only</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin_I/O</td>
<td>X</td>
<td>A</td>
</tr>
<tr>
<td>Pin_Rail</td>
<td>Y, Y, Y</td>
<td></td>
</tr>
<tr>
<td>A_gnd</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

X = Pin_I/O pin_name entry
Y = Pin_Rail pin_name entry or Pin_Rail signal_name entry or Pin_Rail bus_label entry
A = optional “Aggressor_Only”
Table applies for both [EMD Pin List] and [Designator Pin List]

Format for designator interface terminals:
<Terminal_type_qualifier> <designator>..<Qualifier entry>
[EMD Set] and [EMD Model]
Example with Terminal Lines

[EMD Set]  DQ0-DQ1_PDN  |  EMD, U1, U2 designators
[EMD Model]  DQ0-DQ1_U1_U2  |  Slides 4, 6, 7 terminals
File_IBIS-ISS  dq0-dq1.iss  |  DQ0_DQ1_U1_U2

[Number Of Terminals = 12]

1  Pin_I/O  pin_name  C5  |  DQ0
2  Pin_I/O  pin_name  C6  |  DQ1
3  Pin_Rail  signal_name  VDD
4  Pin_Rail  signal_name  VSS
5  Pin_I/O  pin_name  U1.11  |  DQ0
6  Pin_I/O  pin_name  U1.12  |  DQ1
7  Pin_Rail  signal_name  U1.VDD
8  Pin_Rail  signal_name  U1.VSS
9  Pin_I/O  pin_name  U2.11  |  DQ0
10  Pin_I/O  pin_name  U2.12  |  DQ1
11  Pin_Rail  signal_name  U2.VDD
12  Pin_Rail  signal_name  U2.VSS

[End EMD Model]
[End EMD Set]
[EMD Set] and [EMD Model] Hierarchy (for .ems files)

Header section for .ems file
One or more named [EMD Set]s
One or more named [EMD Model]s included

Param, File_TS, File_IBIS-ISS, Unused_port_termination, Number_of_terminals
[EMD Group] (only for .emd files)

Header section

One [Begin EMD]

One or more named [EMD Group]s

Zero or more named [EMD Set]s

[End]
**[EMD Group] Example**

```
[Begin EMD] DQ_Paths
| ... Other keywords

[EMD Group] DQ0_DQ1
| EMD_Set_Name File_Reference
DQ0_DQ1_U1_U4 NA | NA means that [EMD Set] is in .emd file

[End EMD Group]

[EMD Group] DQ0_DQ15
| EMD_Set_Name File_Reference
DQ0_DQ15_U1_U4 dq0_dq15.ems | EMS Set in separate file

[End EMD Group]

[EMD Group] DQ0_DQ15_PDN_U4_S2P
| EMD_Set_Name File_Reference
DQ0_U4 NA
DQ1_U4 NA
| ...
DQ15_U4 NA
PDN_EMD_U4 NA

[End EMD Group]

[End EMD]
| ...
| ... EMS Sets referenced by NA in .emd file
|
[End]
```
Interconnect Modeling Similarities

- Interconnect Modeling
  - Hierarchy: [Begin EMD]-[EMD Group] and [Component]-[Interconnect Model Group]
  - [EMD Group] and [Interconnect Model Group]
  - [EMD Set] and [Interconnect Model Set]
  - [EMD Model] and [Interconnect Model]
    - Same syntax for terminal lines
    - Terminal_type subset without Pad and Buffer names and die pad interface
    - Same File_IBIS-ISS and File_TS rules and subparameters for electrical connections
  - File Header Sections similar (.ems, .ims, .emd, .ibs)
  - .ems file and .ims file structures similar
Other Similarities

- **EBD**
  - [EMD Designator Map] and [Reference Designator Map]
  - Both EBD and EMD start at the top-level
  - EBD’s can reference .ibs and .ebd files
  - EMDs can reference .ibs and .emd files

- **Top-level file entry points**
  - .ibs: [Component] <name>
  - .ims: [Interconnect Model Set] <name>
  - .pkg: [Define Package Model] <name>
  - .ebd: [Begin Board Description] <name>
  - .emd: [Define Module] <name>
  - .ems: [EMD Set] <name>
Some Differences

• I/O terminals:
  o [EMD Model]s support one or more different pin interfaces
  o [Interconnect Model]s limited to only two interfaces out of pin, die pad, buffer
  o In EMD format, I/O terminal associations based on signal_name versus pin_name for Interconnect Modeling format

• Rail terminals:
  o Designator terminal syntax <designator>.<Qualifier_entry> supports pin_name, signal_pin and bus_label entries
Conclusion

- Brief introduction of BIRD202, a ~28 page document proposing two new sections in IBIS
- Many similarities with Interconnect Modeling
- More work planned
- Targeted for IBIS Version 7.1
- An ibischk7 Version 7.1.0 parser upgrade would follow