DesignCon 2020 IBIS Summit
Santa Clara, California
January 31st, 2020

The On Die De-cap Modeling Proposal (BIRD198)

JEITA

Semiconductor & System Design Technical Committee

Semiconductor Design Technology Subcommittee

Presenter : Genichi Tanaka (Renesas Electronics Corporation)

Co-Authors: Atsushi Tomishima (Toshiba Electronic Devices & Storage Corporation)

Megumi Ono (Socionext Inc.)

Agenda

- Background
- Proposal for On Die De-cap Model
- Feedback and Updating
- Conclusion

Agenda

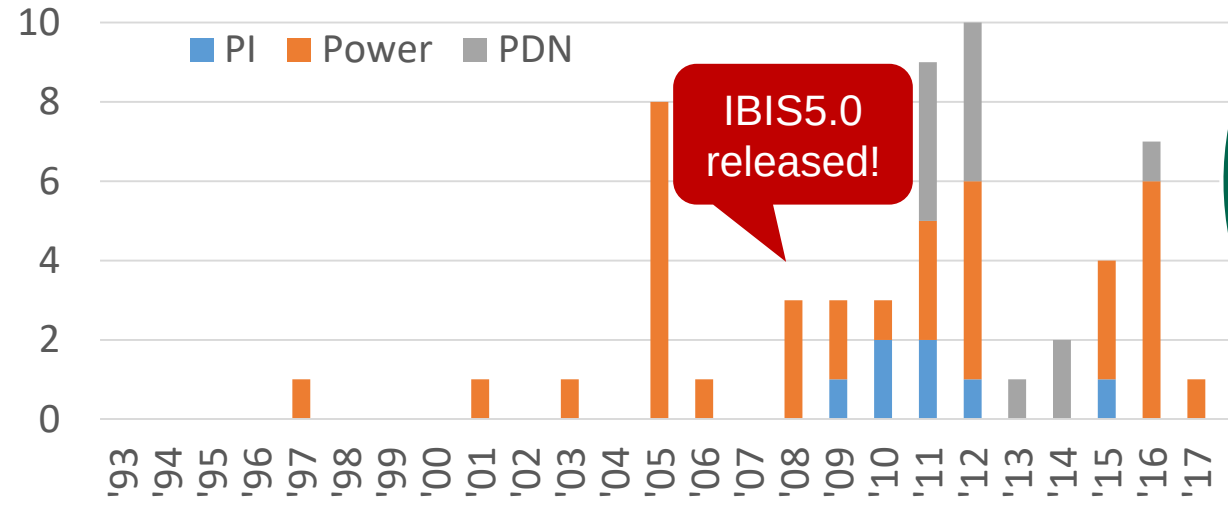
- **Background**
- Proposal for On Die De-cap Model
- Feedback and Updating
- Conclusion

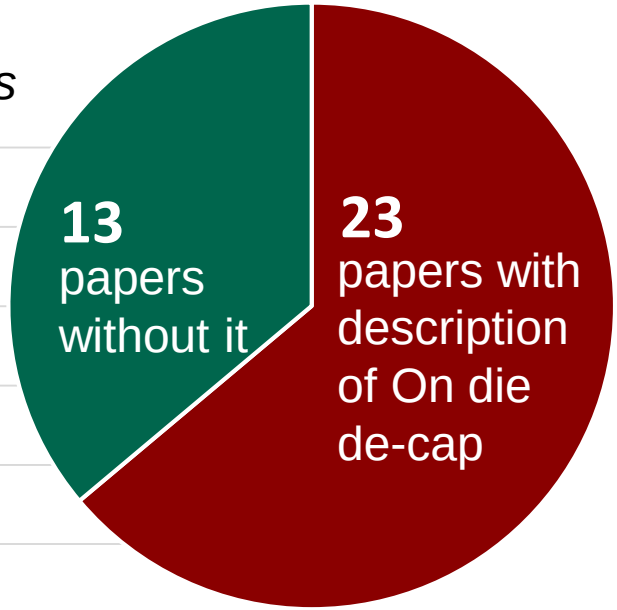
Chip PDN Characteristic

- Chip PDN characteristic
  - On die resistance affects IR-Drop and Q factor
  - On die de-cap affects high frequency power-supply noise

Many papers reported in IBIS Summit describe importance of On die de-cap, because it is one of the few solutions to reduce high frequency power-supply noise

The titles of IBIS Summit papers have the following words



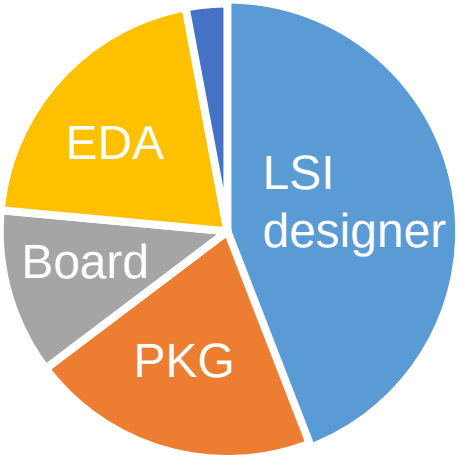


A Survey of On Die De-cap Model

- However, board and system designers can hardly obtain On die de-cap model

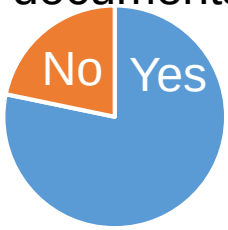
A Survey by JEITA LPB-SC MDL-WG @LPB developers workshop 2017.9.2

Respondents

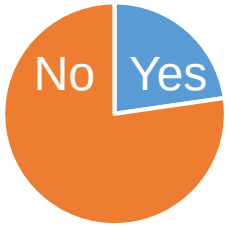


Q1. to All
"Can you obtain information about Chip PDN?"
Answer

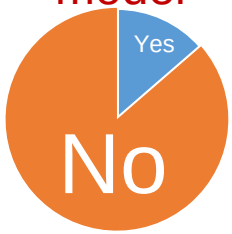
Guideline documents



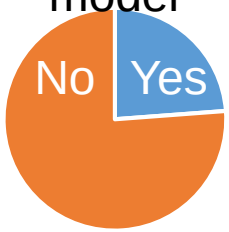
Target Z



On die de-cap model



PKG PDN model

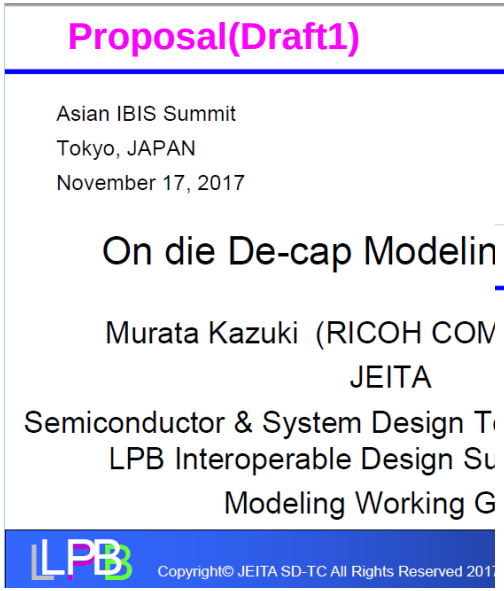


Q2. to LSI designer
"What are you concerned about when you offer PDN model"
Answer
"Which model format is suitable for our customer?"

History of Our Proposal

Nov. 17, 2017 Asian IBIS Summit Tokyo, JAPAN

Proposal(Draft1)


Asian IBIS Summit
Tokyo, JAPAN
November 17, 2017

On die De-cap Modelin

Murata Kazuki (RICOH COM
JEITA
Semiconductor & System Design T
LPB Interoperable Design Su
Modeling Working G

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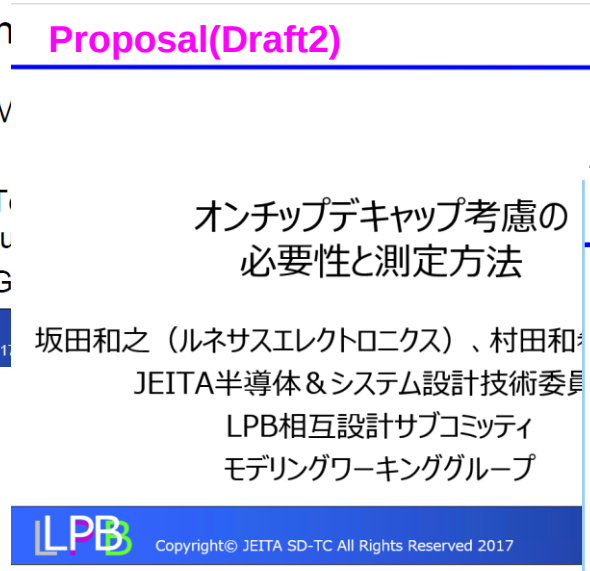
https://ibis.org/summits/nov17c/murata.pdf

Sep. 8, 2018 LPB workshop

Proposal(Draft2)


オンチップデキャップ考慮の
必要性と測定方法

坂田和之（ルネサスエレクトロニクス）、村田和
JEITA半導体＆システム設計技術委員
LPB相互設計サブコミッティ
モデリングワーキンググループ

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Feb. 1, 2019 DesignCon 2019 IBIS Summit

Proposal(Final)


DesignCon 2019 IBIS Summit
Santa Clara, CA
February 1, 2019

On Die De-cap Modeling Proposal

Kazuki Murata (Ricoh Co.,Ltd.), Megumi Ono (Socionext Inc.)
JEITA
Semiconductor & System Design Technical Committee
LPB Interoperable Design Sub-Committee
Modeling Working Group

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https://ibis.org/summits/feb19/murata.pdf

History of Our Proposal

March 11, 2019: Submitted https://ibis.org/birds/

Buffer Issue Resolution Documents (BIRD)

To submit a BIRD to the IBIS Open Forum, please use the BIRD Template, Rev. 1.3.

ID#	Issue Title	Requester	Date Submitted	Date Accepted	Supporting Version
200	C_comp Model Using IBIS-ISS or Touchstone	Randy Wolff, Micron Technology, Inc. Walter Katz, Signal Integrity Software, Inc.	July 9, 2019	September 27, 2019	
199	Fix Rx_Receiver_Sensitivity Inconsistencies	Arpad Muranyi, Mentor a Siemens Business	March 19, 2019	June 7, 2019	
198	Keyword additions for On Die PDN (Power Distribution Network) Modeling	Kazuki Murata; Ricoh Co., Ltd.; Miyoko Goto; Ricoh Co., Ltd.; Kazuyuki Sakata; Renesas Electronics Corporation; Kazunori Yamada; Renesas Electronics Corporation; Kouji Ichikawa; Denso Corporation; Atsushi Tomishima; Toshiba Electronic Devices & Storage Corporation; Takashi Hasegawa; Sony LSI Design Inc.; Koichi Seko, Panasonic Industrial Devices Systems and Technology Co., Ltd.; Toshiki Kanamoto; Hirosaki University Megumi Ono; Socionext Inc.	March 11, 2019		

IBIS Specification Change Template, Rev. 1.3

BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)

BIRD NUMBER: 198
ISSUE TITLE: Keyword additions for On Die PDN (Power Distribution Network) Modeling
REQUESTOR: Kazuki Murata; Ricoh Co., Ltd.; Miyoko Goto; Ricoh Co., Ltd.; Kazuyuki Sakata; Renesas Electronics Corporation; Kazunori Yamada; Renesas Electronics Corporation; Kouji Ichikawa; Denso Corporation; Atsushi Tomishima; Toshiba Electronic Devices & Storage Corporation; Takashi Hasegawa; Sony LSI Design Inc.; Koichi Seko, Panasonic Industrial Devices Systems and Technology Co., Ltd.; Toshiki Kanamoto; Hirosaki University Megumi Ono; Socionext Inc.
DATE SUBMITTED: March 11, 2019
DATE REVISED:
DATE ACCEPTED:

DEFINITION OF THE ISSUE:
To resolve the power-supply noise issue, especially high frequency range, on die decap should be taken account into the simulation. With current IBIS versions, "On Die PDN" can be defined by using the keyword [Series Pin Mapping] and "Model_type Series". However, this method seems not to be widely recognized, because the keyword [Series Pin Mapping] and "Model_type Series" don't make imagine to describe the on die PDNmodel. To ease usage of "On Die PDN" in the IBIS model, this BIRD proposes to add the new keywords [PDN Model Mapping], "Model_type PDN", [C pdn], [R pdn], [R leak], [C pdn corner], [R pdn corner] and [R leak corner] for PDN model only.

SOLUTION REQUIREMENTS:
The IBIS specification must meet these requirements:

Table 1: Solution Requirements

Requirement	Notes
1. A new keyword is defined under [Component]: [PDN Model Mapping]	
2. A new sub parameter is defined under [Model]: "Model_type PDN"	

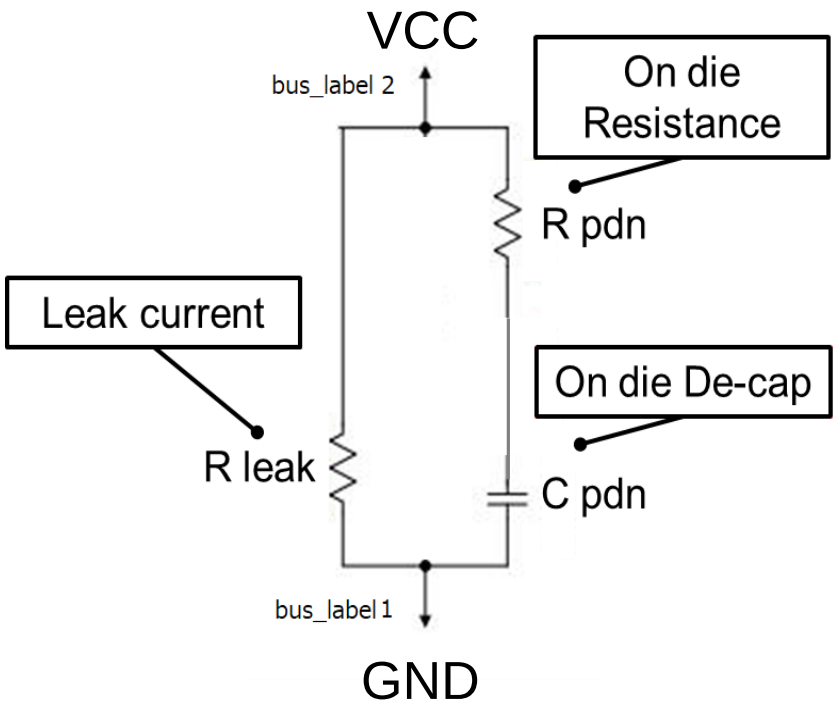
1

Agenda

- Background
- **Proposal for On Die De-cap Model**
- Feedback and Updating
- Conclusion

Proposal

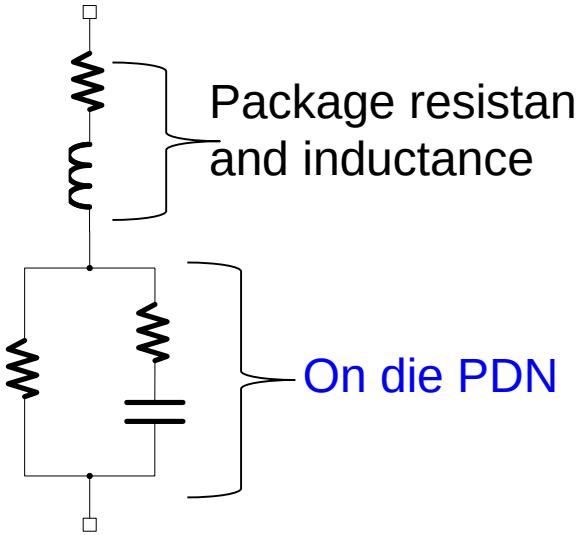
Model

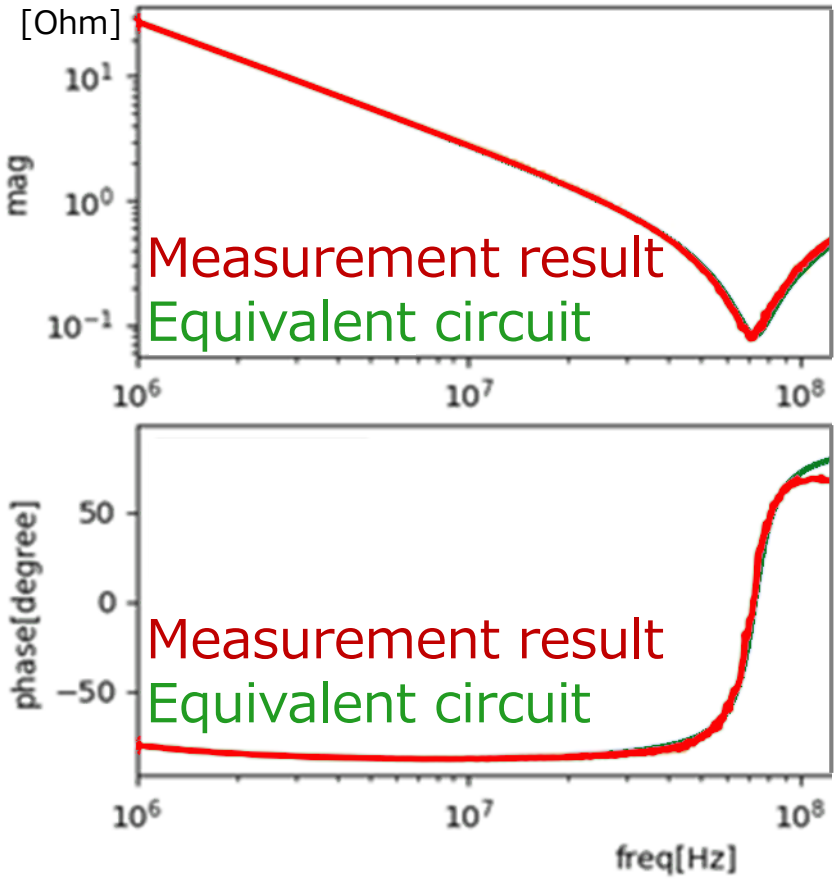


Correlation between Measurement and Model

- Our proposed model is correlated with the measurement results.

Equivalent circuit





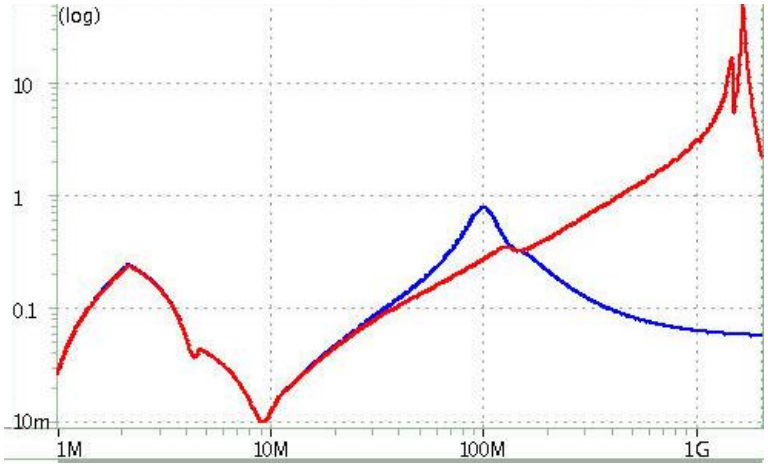
Simulation Results

- Simulation results using the proposed IBIS model

AC analysis result
= PDN input impedance

IBIS with PDN model
IBIS without PDN model

[Ω]

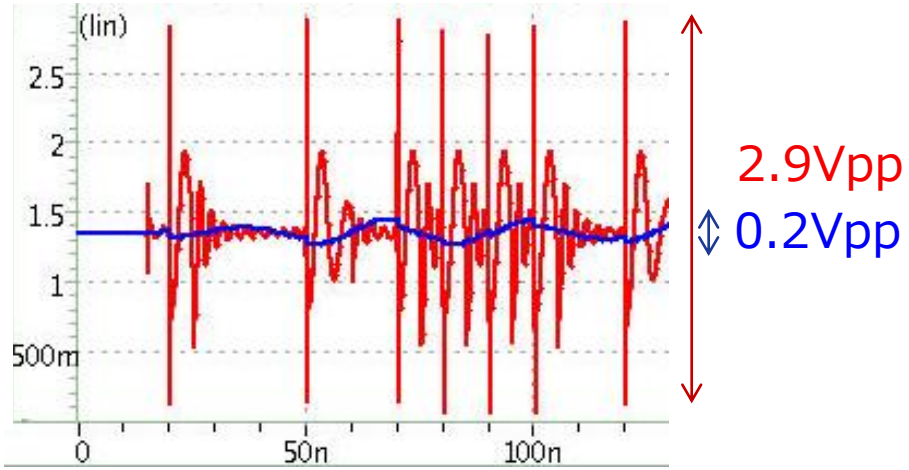


[Hz]

Transient analysis result
= IO switching VDD noise @DIE

IBIS with PDN model
IBIS without PDN model

[V]



[s]

- The expected result was obtained while using a simulator

Agenda

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Original vs. Latest

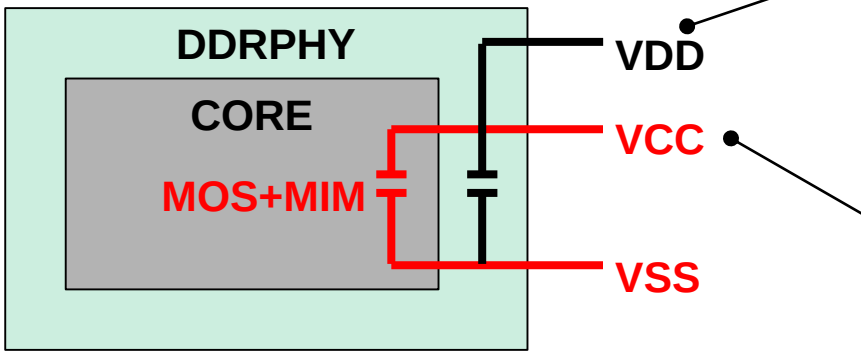
	BIRD198 Original	Latest proposal	Latest feedback from ATM task group
Connection	Pin	Bus_label	Bus_label or signal_name
Parent	[Model]	[Component]	[Component]
Model selecting Method	✓ [Model Selector]	✓ New method [PDN Domain]& [PDN Model]	✓ New method [PDN Domain]& [PDN Model]
Corner definition	✓ The order of the values is not related to magnitude	✓ The order of the values is not related to magnitude Naming Rule : C_pdn_case R_pdn_case R_leak_case	✓ The order of the values is not related to magnitude Naming Rule : C_pdn R_pdn R_leak
Base structure	Series Model	New syntax	New syntax
EDA Vendor	Difficult implementation	Easy implementation	Easy implementation

Latest Proposal

	BIRD198 Original	Latest proposal	Latest feedback from ATM task group
Connection	Pin	Bus_label	Bus_label or signal_name
Parent	[Model]	[Component]	[Component]
Model selecting Method	✓ [Model Selector]	✓ New method [PDN Domain]& [PDN Model]	✓ New method [PDN Domain]& [PDN Model]
Corner definition	✓ The order of the values is not related to magnitude	✓ The order of the values is not related to magnitude Naming Rule : C_pdn_case R_pdn_case R_leak_case	✓ The order of the values is not related to magnitude Naming Rule : C_pdn R_pdn R_leak
Base structure	Series Model	New syntax	New syntax
EDA Vendor	Difficult implementation	Easy implementation	Easy implementation

Case Study (VCC-VSS)

- Assuming that ‘Chip-A’ model has:
  - ✓ Core circuit and core supply voltage VCC-VSS with MIM capacitor.
    - Capacitor by MOS depends on voltage range
    - Capacitor by MIM does not depend on MOS process
  - ✓ DDR3/3L/4 combo PHY and PHY supply voltage VDD-VSS.
    - Capacitor by MOS depends on voltage range
    - Typical VDD voltage changes 1.5V, 1.35V or 1.2V due to mode.



Mode	Typ.	Min	Max
DDR3	1.5V	1.425V	1.575V
DDR3L	1.35V	1.283V	1.425V
DDR4	1.2V	1.14V	1.26V

Typ.	Min	Max
1.0V	0.95V	1.05V

Case Study (IBIS Syntax)

```
[PDN Domain] PDN_for_VCC
      Rail_Bus_Labels VCC VSS
|VCC Voltage                1.0       0.9
|Temp.                      25      125
|Mos                      TT      SS
      [PDN Model] With_Medium_MIM
         C_pdn_case         270n      220n          320n
         R_pdn_case         2.18m     2.67m         0.98m
         R_leak_case        5k        8k            2k
      [End PDN Model]
      [PDN Model] With_Large_MIM
         C_pdn_case         280n      230n          330n
         R_pdn_case         1.93m     2.30m         0.87m
         R_leak_case        5k        8k            2k
      [End PDN Model]
      [PDN Model] With_Small_MIM
         C_pdn_case         260n      210n          310n
         R_pdn_case         2.31m     2.86m         1.01m
         R_leak_case        5k        8k            2k
      [End PDN Model]
   [End PDN Domain]
```

The order of the columns do not matter at all.

Case Study (EDA Selects Value)

EDA example
.ibis syntax_a2
+ file = 'aaa.ibs'
+ component = 'ChipA'
*+ typ = min * or slow*
+ pdn_sel = 'PDN_for_VCC=With_Small_MIM, PDN_for_VDD=DDR3'

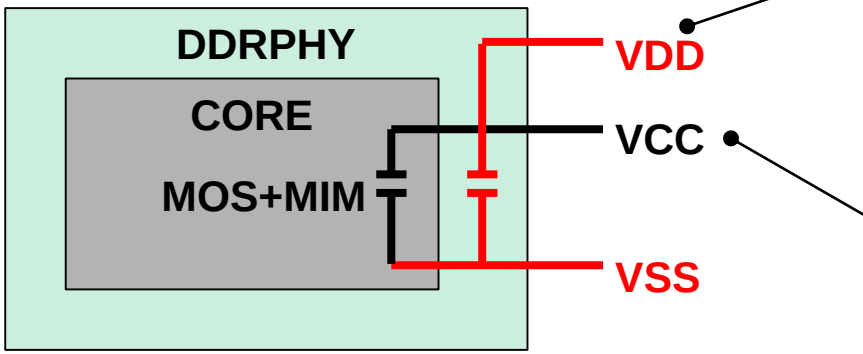
```
                                                    1.05
                                                    -40

                                                      320n
                                                      0.98m
                                                      2k
    [PDN Model] With_Large_MIM
       C_pdn_case          280n        230n
       R_pdn_case          1.93m       2.30m
       R_leak_case         5k          8k
    [End PDN Model]
    [PDN Model] With_Small_MIM
       C_pdn_case          260n        210n          310n
       R_pdn_case          2.31m       2.86m         1.01m
       R_leak_case         5k          8k            2k
    [End PDN Model]
[End PDN Domain]
```

EDA Selects the values

Case Study (VDD-VSS)

- Assuming that ‘Chip-A’ model has:
  - ✓ Core circuit and core supply voltage VCC-VSS with MIM capacitor.
    - Capacitor by MOS depends voltage range
    - Capacitor by MIM does not depend MOS process
  - ✓ DDR3/3L/4 combo PHY and PHY supply voltage VDD-VSS.
    - Capacitor by MOS depends on voltage range
    - Typical VDD voltage changes 1.5V, 1.35V or 1.2V due to mode.



Mode	Typ.	Min	Max
DDR3	1.5V	1.425V	1.575V
DDR3L	1.35V	1.283V	1.425V
DDR4	1.2V	1.14V	1.26V

Typ.	Min	Max
1.0V	0.95V	1.05V

Case Study (IBIS Syntax)

```
[PDN Domain] PDN_for_VDD
      Rail_Bus_Labels VDD VSS
|VDD Voltage                1.5       1.425     1.575
      [PDN Model] DDR3
         C_pdn_case      5n          4n          6n
         R_pdn_case      20m             30m             10m
         R_leak_case     15k             17k             11k
      [End PDN Model]
|VDD Voltage              1.35      1.283     1.425
      [PDN Model] DDR3L
         C_pdn_case      3n          2n          4.2n
         R_pdn_case      20m             30m             10m
         R_leak_case     15k             17k             11k
      [End PDN Model]
|VDD Voltage               1.2       1.14      1.26
      [PDN Model] DDR4
         C_pdn_case      1.5n        1n          1.8n
         R_pdn_case      20m             30m             10m
         R_leak_case     15k             17k             11k
      [End PDN Model]
   [End PDN Domain]
```

Case Study (EDA Selects Value)

```
[PDN Domain] PDN_for_VDD
      Rail_Bus_Labels VDD VSS
|VDD Voltage                1.5      1.425     1.575
      [PDN Model] DDR3
         C_pdn_case      5n          4n          6n
         R_pdn_case      20m         30m         10m
         R_leak_case     15k         17k         11k
      [End PDN Model]
```

EDA example
.ibis syntax_a2
+ file = 'aaa.ibs'
+ component = 'ChipA'
*+ typ = min * or slow*
+ pdn_sel = 'PDN_for_VCC=With_Small_MIM, PDN_for_VDD=DDR3'

EDA Selects the values

```
6

      1.8n
      10m
      11k
      [End PDN Model]
   [End PDN Domain]
```

Latest Feedback

	BIRD198 Original	Latest proposal	Latest feedback from ATM task group
Connection	Pin	Bus_label	Bus_label or **signal_name**
Parent	[Model]	[Component]	[Component]
Model selecting Method	✓ [Model Selector]	✓ New method [PDN Domain]& [PDN Model]	✓ New method [PDN Domain]& [PDN Model]
Corner definition	✓ The order of the values is not related on magnitude	✓ The order of the values is not related on magnitude Naming Rule : C_pdn_case R_pdn_case R_leak_case	✓ The order of the values is not related on magnitude Naming Rule : **C_pdn** **R_pdn** **R_leak**
Base structure	Series Model	New syntax	New syntax
EDA Vendor	Difficult implementation	Easy implementation	Easy implementation

Latest Feedback1 from ATM Task Group

Changes to consider:

1. The Rail_Bus_labels subparameter should be changed to allow for declaration by bus_label or signal_name. Still scoped under [PDN Domain], possible syntax is:

   Bus_label VCC1 | the beginning letter is upper case
   Signal_name VSS

   We could have separately as another set of terminals under a different [PDN Domain]:

   Signal_name VCC
   Signal_name VSS

   Note if VCC1 is a bus_label of VCC, than we have shorted all VCC terminals and there is no separate VCC1 terminal. All of this needs to be considered. Rules in Interconnect modeling may help describe this.

   Also, this would be illegal because one is a self-referencing subset of the other:

   Bus_label VCC1
   Signal_name VC

2. "_case" could be removed for the names of the "C_pdn, R_pdn, and R_leak" parameters for simplification.
3. The examples should show "1G" for R_leak, since only "G" is defined in Section 3.2 SYNTAX RULES as a valid scale factor. "g" is not defined as valid.
4. It is not necessary, but you might consider wrapping all [PDN Domain]/[End PDN Domain] sections within a [Begin PDN Domains]/[End PDN Domains] keyword pair. This simplifies scoping of the whole section under [Component]. Otherwise, you could write a rule requiring all [PDN Domain]/[End PDN Domain] sections be grouped together. Without a requirement, these sections could be spread out amongst other keyword sections under a [Component], making it difficult to read and parse.

Latest Feedback1 from ATM Task Group

Changes to consider:

1. **The Rail_Bus_labels** subparameter should be changed to allow for declaration by **bus_label or signal_name.**

   Still scoped under [PDN Domain], possible syntax is:

   Bus_label VCC1 | the beginning letter is upper case
   Signal_name VSS

   We could have separately as another set of terminals under a different [PDN Domain]:

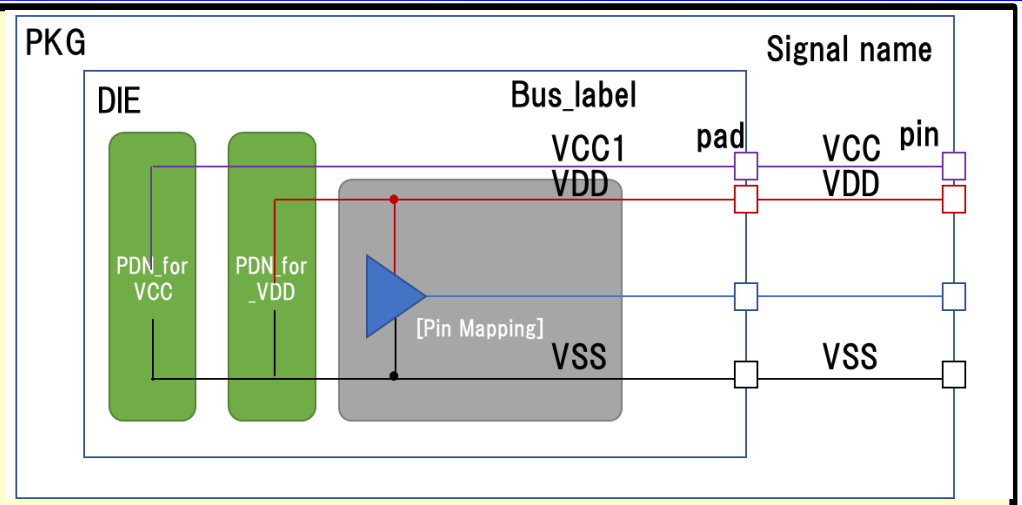
   Signal_name VCC
   Signal_name VSS

Case Study (IBIS Syntax)

```
[Component]   ChipA
   [Pin]
      pin_A VCC POWER
      pin_B VDD POWER
      pin_C VSS GND
   [Pin Mapping]
      pin_A   NC     VCC1
      pin_B   NC     VDD
      pin_C   VSS    NC

   [PDN Domain] PDN_for_VCC
| A rail must be either a bus_label or a signal_name
                     Signal_name  VCC
                     Signal_name  VSS

| Alternately, if bus_label VCC1 is defined in [Pin
Mapping]:
|                    Bus_label    VCC1
|                    Signal_name  VSS
```



Latest Feedback2 from ATM Task Group

Some rules to define with text and examples:

1. "NA" is allowed for slow/fast column values of C_pdn, R_pdn, and R_leak. This aligns with other parameters in IBIS. If the slow or fast column value is NA, then the EDA tool shall use the Typ value for simulation.
2. A PDN Model may contain:
   a. C_pdn, R_pdn, and R_leak parameters
   b. Only C_pdn and R_pdn parameters. R_leak is assumed to be a large value (e.g. 1G).
   c. Only C_pdn and R_leak parameters. R_pdn is assumed to be a small value (e.g. 0.0).
   d. Only C_pdn. R_pdn is assumed to be a small value (e.g. 0.0). R_leak is assumed to be a large value (e.g. 1G).
   e. Only R_leak.
3. Allowed values for C_pdn, R_pdn, and R_leak parameters should be defined:
   a. C_pdn shall be a non-negative number (positive or zero)
   b. R_pdn shall be a non-negative number (positive or zero)
   c. R_leak shall be a positive number (zero is not allowed)
4. [PDN Model] default selection rule should be defined. Example below mirrors the statement from [Model Selector]. The first [PDN Model] entry under the [PDN Domain] keyword shall be considered the default by the EDA tool.

Proposal from JEITA

We mostly agree「ATM Task Group Proposal」.

2. A PDN Model may contain:
   a. C_pdn, R_pdn, and R_leak parameters
   b. Only C_pdn and R_pdn parameters. R_leak is assumed to be a large value (e.g. 1G).
   c. Only C_pdn and R_leak parameters. R_pdn is assumed to be a small value (e.g. 0.0).
   d. Only C_pdn. R_pdn is assumed to be a small value (e.g. 0.0).
      R_leak is assumed to be a large value (e.g. 1G).
   e. Only R_leak.

Our proposal is

“All parameters(C_pdn, R_pdn, and R_leak) must be defined.”

“The purser and EDA tool will give the error in case of the lack of definition”

```
[PDN Model] Legal_PDN
C_pdn     280n   230n   330n
R_pdn     1.9m   2.3m   0.8m
R_leak    1G     1G     1G
[End PDN Model]
```

```
[PDN Model] Not_legal_PDN
C_pdn     280n   230n   330n
R_pdn     1.9m   2.3m   0.8m

[End PDN Model]
```

NOT LEGAL

Case Study (IBIS Syntax)

```
|R_leak = Open
[PDN Model] With_Large_MIM
            C_pdn      280n    230n    330n
            R_pdn      1.93m   2.30m   0.87m
            R_leak      1G      1G      1G
[End PDN Model]

|R_pdn = 0ohm
[PDN Model] With_Large_MIM
            C_pdn      280n    230n    330n
            R_pdn      0       0        0
            R_leak     5k      8k      2k
[End PDN Model]

|C_pdn = 0pF and R_pdn = 0ohm (Only R_leak)
| (parser might issue warning about C_pdn = 0)
[PDN Model] With_Large_MIM
            C_pdn      0       0        0
            R_pdn      0       0        0
            R_leak     5k      8k      2k
[End PDN Model]
```

Agenda

- Background
- Proposal for On Die De-cap Model
- Feedback and Updating
- **Conclusion**

Conclusion

Chip PDN model is still not widespread. Therefore, we proposed to add an explicit keyword of chip PDN to IBIS.

Our proposal was registered as BIRD198 and it has been discussed in IBIS Open Forum since this March 2019.

Thanks to the excellent discussion with the task group, the improved BIRD will be completed soon.

We plan to update BIRD198 to BIRD198.1 by March 13, 2020.

We expect that BIRD198.1 will be adopted and will be useful to many IBIS users.

Thank you!