The On Die De-cap Modeling Proposal (BIRD198)

JEITA

Semiconductor & System Design Technical Committee

Semiconductor Design Technology Subcommittee

Presenter: Genichi Tanaka (Renesas Electronics Corporation)
Co-Authors: Atsushi Tomishima (Toshiba Electronic Devices & Storage Corporation)
Megumi Ono (Socionext Inc.)
Agenda

- Background
- Proposal for On Die De-cap Model
- Feedback and Updating
- Conclusion
Agenda

- Background
- Proposal for On Die De-cap Model
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- Conclusion
Chip PDN Characteristic

- Chip PDN characteristic
  - On die resistance affects IR-Drop and Q factor
  - On die de-cap affects high frequency power-supply noise

Many papers reported in IBIS Summit describe importance of **On die de-cap**, because it is one of the few solutions to reduce high frequency power-supply noise

*The titles of IBIS Summit papers have the following words*

- IBIS5.0 released!
- 13 papers without it
- 23 papers with description of On die de-cap
However, board and system designers can hardly obtain the on die de-cap model.

A Survey by JEITA LPB-SC MDL-WG @LPB developers workshop 2017.9.2

Q1. to All
“Can you obtain information about Chip PDN?”
Answer
Yes
No

Guideline documents

Q2. to LSI designer
“What are you concerned about when you offer PDN model”
Answer
“No
Yes

On die de-cap model
Yes
No

PKG PDN model
No
Yes
History of Our Proposal

Nov. 17, 2017  Asian IBIS Summit Tokyo, JAPAN

Proposal (Draft1)
Asian IBIS Summit
Tokyo, JAPAN
November 17, 2017

Sep. 8, 2018  LPB workshop
On die De-cap Modelin
Proposal (Draft2)

Murata Kazuki (RICOH COMMUNICATION NETWORKS)
JEITA
Semiconductor & System Design Technical Committee
LPB Interoperable Design Subcommittee
Modeling Working Group

Feb. 1, 2019  DesignCon 2019 IBIS Summit

Proposal (Final)
DesignCon 2019 IBIS Summit
Santa Clara, CA
February 1, 2019

On Die De-cap Modeling Proposal
Kazuki Murata (Ricoh Co., Ltd.), Megumi Ono (Socionext Inc.)
JEITA
Semiconductor & System Design Technical Committee
LPB Interoperable Design Sub-Committee
Modeling Working Group

https://ibis.org/summits/nov17c/murata.pdf
https://ibis.org/summits/feb19/murata.pdf
History of Our Proposal

March 11, 2019: Submitted  https://ibis.org/birds/

Buffer Issue Resolution Documents (BIRD)

To submit a BIRD to the IBIS Open Forum, please use the BIRD Template, Rev. 1.3.

<table>
<thead>
<tr>
<th>ID#</th>
<th>Issue Title</th>
<th>Requester</th>
<th>Date Submitted</th>
<th>Date Accepted</th>
<th>Supporting Version</th>
</tr>
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<tbody>
<tr>
<td>199</td>
<td>Fix Rx Receiver Sensitivity Inconsistencies</td>
<td>Arpad Muranyi, Mentor a Siemens Business</td>
<td>March 19, 2019</td>
<td>June 7, 2019</td>
<td></td>
</tr>
<tr>
<td>198</td>
<td>Keyword additions for On Die PDN (Power Distribution Network) Modeling</td>
<td>Kazuki Murata; Ricoh Co., Ltd.; Miyoko Goto; Ricoh Co., Ltd.; Kazuyuki Sakata; Renesas Electronics Corporation; Kazunori Yamada; Renesas Electronics Corporation; Kouji Ichikawa; Denso Corporation; Atsushi Tomishima; Toshiba Electronic Devices &amp; Storage Corporation; Takashi Hasegawa; Sony LSI Design Inc.; Koichi Seko, Panasonic Industrial Devices Systems and Technology Co., Ltd.; Toshiki Kanamoto; Hirosuki University Megumi Ono; Socionext Inc.</td>
<td>March 11, 2019</td>
<td></td>
<td>188</td>
</tr>
</tbody>
</table>
Agenda

- Background
- Proposal for On Die De-cap Model
- Feedback and Updating
- Conclusion
Proposal

Model

![Model Diagram]

- **VCC**
- **GND**
- **Leak current**
- **R leak**
- **On die Resistance**
- **R pdn**
- **On die De-cap**
- **C pdn**

bus_label 1

bus_label 2
Correlation between Measurement and Model

- Our proposed model is correlated with the measurement results.

Equivalent circuit

Package resistance and inductance

On die PDN

Measurement result

Equivalent circuit

Measurement result

Equivalent circuit
Simulation Results

- Simulation results using the proposed IBIS model

**AC analysis result**
- = PDN input impedance

**IBIS with PDN model**
**IBIS without PDN model**

![AC analysis result graph]

**Transient analysis result**
- = IO switching VDD noise @DIE

**IBIS with PDN model**
**IBIS without PDN model**

![Transient analysis result graph]

- The expected result was obtained while using a simulator

2.9Vpp

0.2Vpp
Agenda

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## Original vs. Latest

<table>
<thead>
<tr>
<th>Connection</th>
<th>BIRD198 Original</th>
<th>Latest proposal</th>
<th>Latest feedback from ATM task group</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin</td>
<td>Bus_label</td>
<td>Bus_label or</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>signal_name</td>
<td></td>
</tr>
<tr>
<td>Parent</td>
<td>[Model]</td>
<td>[Component]</td>
<td>[Component]</td>
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<tr>
<td>Corner definition</td>
<td>✓ The order of the values is not related to magnitude</td>
<td>✓ The order of the values is not related to magnitude</td>
<td>✓ The order of the values is not related to magnitude</td>
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<tr>
<td></td>
<td></td>
<td>Naming Rule :</td>
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<tr>
<td></td>
<td></td>
<td>C_pdn_case</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>R_pdn_case</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>R_leak_case</td>
<td></td>
</tr>
<tr>
<td>Base structure</td>
<td>Series Model</td>
<td>New syntax</td>
<td>New syntax</td>
</tr>
<tr>
<td>EDA Vendor</td>
<td>Difficult implementation</td>
<td>Easy implementation</td>
<td>Easy implementation</td>
</tr>
</tbody>
</table>
## Latest Proposal

<table>
<thead>
<tr>
<th></th>
<th>BIRD198 Original</th>
<th>Latest proposal</th>
<th>Latest feedback from ATM task group</th>
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</thead>
<tbody>
<tr>
<td><strong>Connection</strong></td>
<td>Pin</td>
<td>Bus_label</td>
<td>Bus_label or signal_name</td>
</tr>
<tr>
<td><strong>Parent</strong></td>
<td>[Model]</td>
<td>[Component]</td>
<td>[Component]</td>
</tr>
<tr>
<td><strong>Corner definition</strong></td>
<td>✓ The order of the values is not related to magnitude</td>
<td>✓ The order of the values is not related to magnitude Naming Rule: C_pdn_case R_pdn_case R_leak_case</td>
<td>✓ The order of the values is not related to magnitude Naming Rule: C_pdn R_pdn R_leak</td>
</tr>
<tr>
<td><strong>Base structure</strong></td>
<td>Series Model</td>
<td>New syntax</td>
<td>New syntax</td>
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<td><strong>EDA Vendor</strong></td>
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</tr>
</tbody>
</table>
Case Study (VCC-VSS)

Assuming that ‘Chip-A’ model has:
✓ Core circuit and core supply voltage VCC-VSS with MIM capacitor.
  • Capacitor by MOS depends on voltage range
  • Capacitor by MIM does not depend on MOS process
✓ DDR3/3L/4 combo PHY and PHY supply voltage VDD-VSS.
  • Capacitor by MOS depends on voltage range
  • Typical VDD voltage changes 1.5V, 1.35V or 1.2V due to mode.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Typ.</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR3</td>
<td>1.5V</td>
<td>1.425V</td>
<td>1.575V</td>
</tr>
<tr>
<td>DDR3L</td>
<td>1.35V</td>
<td>1.283V</td>
<td>1.425V</td>
</tr>
<tr>
<td>DDR4</td>
<td>1.2V</td>
<td>1.14V</td>
<td>1.26V</td>
</tr>
</tbody>
</table>

Typ. | Min   | Max    |
-----|-------|--------|
1.0V | 0.95V | 1.05V  |
Case Study (IBIS Syntax)

<table>
<thead>
<tr>
<th>PDN Domain</th>
<th>PDN_for_VCC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rail_Bus_Labels</td>
<td>VCC VSS</td>
</tr>
<tr>
<td>VCC Voltage</td>
<td>1.0</td>
</tr>
<tr>
<td>Temp.</td>
<td>25</td>
</tr>
<tr>
<td>Mos</td>
<td>TT</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PDN Model</th>
<th>With_Medium_MIM</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_pdn_case</td>
<td>270n</td>
</tr>
<tr>
<td>R_pdn_case</td>
<td>2.18m</td>
</tr>
<tr>
<td>R_leak_case</td>
<td>5k</td>
</tr>
</tbody>
</table>

[End PDN Model]

<table>
<thead>
<tr>
<th>PDN Model</th>
<th>With_Large_MIM</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_pdn_case</td>
<td>280n</td>
</tr>
<tr>
<td>R_pdn_case</td>
<td>1.93m</td>
</tr>
<tr>
<td>R_leak_case</td>
<td>5k</td>
</tr>
</tbody>
</table>

[End PDN Model]

<table>
<thead>
<tr>
<th>PDN Model</th>
<th>With_Small_MIM</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_pdn_case</td>
<td>260n</td>
</tr>
<tr>
<td>R_pdn_case</td>
<td>2.31m</td>
</tr>
<tr>
<td>R_leak_case</td>
<td>5k</td>
</tr>
</tbody>
</table>

[End PDN Model]

[End PDN Domain]
Case Study (EDA Selects Value)

EDA example

```
.ibis syntax_a2
+ file = 'aaa.ibs'
+ component = 'ChipA'
+ typ = min * or slow
+ pdn_sel = 'PDN_for_VCC=With_Small_MIM, PDN_for_VDD=DDR3'
```

EDA Selects the values

<table>
<thead>
<tr>
<th>PDN Model</th>
<th>With_Small_MIM</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_pdn_case</td>
<td>280n 230n</td>
</tr>
<tr>
<td>R_pdn_case</td>
<td>1.93m 2.30m</td>
</tr>
<tr>
<td>R_leak_case</td>
<td>5k 8k</td>
</tr>
</tbody>
</table>

[End PDN Model]
Case Study (VDD-VSS)

- Assuming that ‘Chip-A’ model has:
  - Core circuit and core supply voltage VCC-VSS with MIM capacitor.
    - Capacitor by MOS depends voltage range
    - Capacitor by MIM does not depend MOS process
  - DDR3/3L/4 combo PHY and PHY supply voltage VDD-VSS.
    - Capacitor by MOS depends on voltage range
    - Typical VDD voltage changes 1.5V, 1.35V or 1.2V due to mode.

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<tr>
<td>DDR3</td>
<td>1.5V</td>
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<td>DDR3L</td>
<td>1.35V</td>
<td>1.283V</td>
<td>1.425V</td>
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<tr>
<td>DDR4</td>
<td>1.2V</td>
<td>1.14V</td>
<td>1.26V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Typ.</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0V</td>
<td>0.95V</td>
<td>1.05V</td>
</tr>
</tbody>
</table>
**Case Study (IBIS Syntax)**

```
[PDN Domain] PDN_for_VDD
   Rail_Bus_Labels VDD VSS
|VDD Voltage | 1.5   | 1.425 | 1.575 |
[PDN Model] DDR3
   C_pdn_case  5n   4n   6n
   R_pdn_case  20m  30m  10m
   R_leak_case 15k  17k  11k
[End PDN Model]
|VDD Voltage | 1.35  | 1.283 | 1.425 |
[PDN Model] DDR3L
   C_pdn_case  3n   2n   4.2n
   R_pdn_case  20m  30m  10m
   R_leak_case 15k  17k  11k
[End PDN Model]
|VDD Voltage | 1.2   | 1.14  | 1.26  |
[PDN Model] DDR4
   C_pdn_case  1.5n  1n   1.8n
   R_pdn_case  20m  30m  10m
   R_leak_case 15k  17k  11k
[End PDN Model]
[End PDN Domain]
```
## EDA example

```
+ file = 'aaa.ibs'
+ component = 'ChipA'
+ typ = min * or slow
+ pdn_sel = 'PDN_for_VCC=With_Small_MIM,
            PDN_for_VDD=DDR3'
```

**EDA Selects the values**

<table>
<thead>
<tr>
<th>VDD Voltage</th>
<th>1.5</th>
<th>1.425</th>
<th>1.575</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>[PDN Model] DDR3</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C_pdn_case</td>
<td>5n</td>
<td>4n</td>
<td>6n</td>
</tr>
<tr>
<td>R_pdn_case</td>
<td>20m</td>
<td>30m</td>
<td>10m</td>
</tr>
<tr>
<td>R_leak_case</td>
<td>15k</td>
<td>17k</td>
<td>11k</td>
</tr>
<tr>
<td><strong>[End PDN Model]</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VDD Voltage</th>
<th>1.35</th>
<th>1.283</th>
<th>1.425</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>[PDN Model] DDR3L</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C_pdn_case</td>
<td>3n</td>
<td>2n</td>
<td>4.2n</td>
</tr>
<tr>
<td>R_pdn_case</td>
<td>20m</td>
<td>30m</td>
<td>10m</td>
</tr>
<tr>
<td>R_leak_case</td>
<td>1</td>
<td>5k</td>
<td>17k</td>
</tr>
<tr>
<td><strong>[End PDN Model]</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VDD Voltage</th>
<th>1.2</th>
<th>1.14</th>
<th>1.26</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>[PDN Model] DDR4</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C_pdn_case</td>
<td>1.5n</td>
<td>1n</td>
<td>1.8n</td>
</tr>
<tr>
<td>R_pdn_case</td>
<td>20m</td>
<td>30m</td>
<td>10m</td>
</tr>
<tr>
<td>R_leak_case</td>
<td>1</td>
<td>5k</td>
<td>17k</td>
</tr>
<tr>
<td><strong>[End PDN Model]</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>[End PDN Domain]</strong></td>
<td></td>
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</table>
## Latest Feedback

<table>
<thead>
<tr>
<th></th>
<th>BIRD198 Original</th>
<th>Latest proposal</th>
<th>Latest feedback from ATM task group</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Connection</strong></td>
<td>Pin</td>
<td>Bus_label</td>
<td>Bus_label or signal_name</td>
</tr>
<tr>
<td><strong>Parent</strong></td>
<td>[Model]</td>
<td>[Component]</td>
<td>[Component]</td>
</tr>
<tr>
<td><strong>Corner definition</strong></td>
<td>✓  The order of the values is not related on magnitude</td>
<td>✓  The order of the values is not related on magnitude</td>
<td>✓  The order of the values is not related on magnitude</td>
</tr>
<tr>
<td><strong>Base structure</strong></td>
<td>Series Model</td>
<td>New syntax</td>
<td>New syntax</td>
</tr>
<tr>
<td><strong>EDA Vendor</strong></td>
<td>Difficult implementation</td>
<td>Easy implementation</td>
<td>Easy implementation</td>
</tr>
</tbody>
</table>
Latest Feedback1 from ATM Task Group

Changes to consider:

1. The Rail_Bus_labels subparameter should be changed to allow for declaration by bus_label or signal_name. Still scoped under [PDN Domain], possible syntax is:
   - Bus_label  VCC1  | the beginning letter is upper case
   - Signal_name VSS

   We could have separately as another set of terminals under a different [PDN Domain]:

   - Signal_name  VCC
   - Signal_name  VSS

   Note if VCC1 is a bus_label of VCC, than we have shorted all VCC terminals and there is no separate VCC1 terminal. All of this needs to be considered. Rules in Interconnect modeling may help describe this.

   Also, this would be illegal because one is a self-referencing subset of the other:

   - Bus_label  VCC1
   - Signal_name VC

2. “_case” could be removed for the names of the “C_pdn, R_pdn, and R_leak” parameters for simplification.

3. The examples should show “1G” for R_leak, since only “G” is defined in Section 3.2 SYNTAX RULES as a valid scale factor. “g” is not defined as valid.

4. It is not necessary, but you might consider wrapping all [PDN Domain]/[End PDN Domain] sections within a [Begin PDN Domains]/[End PDN Domains] keyword pair. This simplifies scoping of the whole section under [Component]. Otherwise, you could write a rule requiring all [PDN Domain]/[End PDN Domain] sections be grouped together. Without a requirement, these sections could be spread out amongst other keyword sections under a [Component], making it difficult to read and parse.
Changes to consider:

1. **The Rail_Bus_labels** subparameter should be changed to allow for declaration by **bus_label or signal_name**.

   Still scoped under [PDN Domain], possible syntax is:
   
   - **Bus_label** VCC1 | the beginning letter is upper case
   - **Signal_name** VSS

   We could have separately as another set of terminals under a different [PDN Domain]:

   - **Signal_name** VCC
   - **Signal_name** VSS
Case Study (IBIS Syntax)

[Component] ChipA

[Pin]
- pin_A VCC POWER
- pin_B VDD POWER
- pin_C VSS GND

[Pin Mapping]
- pin_A NC VCC1
- pin_B NC VDD
- pin_C VSS NC

[PDN Domain] PDN_for_VCC
| A rail must be either a bus_label or a signal_name
- Signal_name VCC
- Signal_name VSS

| Alternately, if bus_label VCC1 is defined in [Pin Mapping]:
| Bus_label VCC1
| Signal_name VSS
Some rules to define with text and examples:

1. “NA” is allowed for slow/fast column values of $C_{pdn}$, $R_{pdn}$, and $R_{leak}$. This aligns with other parameters in IBIS. If the slow or fast column value is NA, then the EDA tool shall use the Typ value for simulation.

2. A PDN Model may contain:
   a. $C_{pdn}$, $R_{pdn}$, and $R_{leak}$ parameters
   b. Only $C_{pdn}$ and $R_{pdn}$ parameters. $R_{leak}$ is assumed to be a large value (e.g. 1G).
   c. Only $C_{pdn}$ and $R_{leak}$ parameters. $R_{pdn}$ is assumed to be a small value (e.g. 0.0).
   d. Only $C_{pdn}$. $R_{pdn}$ is assumed to be a small value (e.g. 0.0). $R_{leak}$ is assumed to be a large value (e.g. 1G).
   e. Only $R_{leak}$.

3. Allowed values for $C_{pdn}$, $R_{pdn}$, and $R_{leak}$ parameters should be defined:
   a. $C_{pdn}$ shall be a non-negative number (positive or zero)
   b. $R_{pdn}$ shall be a non-negative number (positive or zero)
   c. $R_{leak}$ shall be a positive number (zero is not allowed)

4. [PDN Model] default selection rule should be defined. Example below mirrors the statement from [Model Selector]. The first [PDN Model] entry under the [PDN Domain] keyword shall be considered the default by the EDA tool.
Proposal from JEITA

We mostly agree 「ATM Task Group Proposal」.

2. A PDN Model may contain:
   a. \(C_{pdn}, R_{pdn}, \) and \(R_{leak}\) parameters
   b. Only \(C_{pdn}\) and \(R_{pdn}\) parameters. \(R_{leak}\) is assumed to be a large value (e.g. 1G).
   c. Only \(C_{pdn}\) and \(R_{leak}\) parameters. \(R_{pdn}\) is assumed to be a small value (e.g. 0.0).
   d. Only \(C_{pdn}\). \(R_{pdn}\) is assumed to be a small value (e.g. 0.0). \(R_{leak}\) is assumed to be a large value (e.g. 1G).
   e. Only \(R_{leak}\).

Our proposal is

“All parameters\((C_{pdn}, R_{pdn}, \text{and } R_{leak})\) must be defined.”

“The purser and EDA tool will give the error in case of the lack of definition”

<table>
<thead>
<tr>
<th>PDN Model</th>
<th>Legal_PDN</th>
<th>Not_legal_PDN</th>
</tr>
</thead>
<tbody>
<tr>
<td>(C_{pdn})</td>
<td>280n 230n 330n</td>
<td>280n 230n 330n</td>
</tr>
<tr>
<td>(R_{pdn})</td>
<td>1.9m 2.3m 0.8m</td>
<td>1.9m 2.3m 0.8m</td>
</tr>
<tr>
<td>(R_{leak})</td>
<td>1G 1G 1G</td>
<td>1G 1G 1G</td>
</tr>
</tbody>
</table>

[End PDN Model] [End PDN Model] NOT LEGAL
Case Study (IBIS Syntax)

$R_{\text{leak}} = \text{Open}$

[PDN Model] With Large MIM

\[
\begin{array}{c|c|c|c}
C_{\text{pdn}} & 280n & 230n & 330n \\
R_{\text{pdn}} & 1.93m & 2.30m & 0.87m \\
R_{\text{leak}} & 1G & 1G & 1G \\
\end{array}
\]

[End PDN Model]

$R_{\text{pdn}} = 0 \text{ohm}$

[PDN Model] With Large MIM

\[
\begin{array}{c|c|c|c}
C_{\text{pdn}} & 280n & 230n & 330n \\
R_{\text{pdn}} & 0 & 0 & 0 \\
R_{\text{leak}} & 5k & 8k & 2k \\
\end{array}
\]

[End PDN Model]

$C_{\text{pdn}} = 0 \text{pF and } R_{\text{pdn}} = 0 \text{ohm} \text{ (Only } R_{\text{leak}})$

(\text{parser might issue warning about } C_{\text{pdn}} = 0)

[PDN Model] With Large MIM

\[
\begin{array}{c|c|c|c}
C_{\text{pdn}} & 0 & 0 & 0 \\
R_{\text{pdn}} & 0 & 0 & 0 \\
R_{\text{leak}} & 5k & 8k & 2k \\
\end{array}
\]

[End PDN Model]
Agenda

- Background
- Proposal for On Die De-cap Model
- Feedback and Updating
- Conclusion
Chip PDN model is still not widespread. Therefore, we proposed to add an explicit keyword of chip PDN to IBIS.

Our proposal was registered as BIRD198 and it has been discussed in IBIS Open Forum since this March 2019.
Thanks to the excellent discussion with the task group, the improved BIRD will be completed soon.
We plan to update BIRD198 to BIRD198.1 by March 13, 2020.

We expect that BIRD198.1 will be adopted and will be useful to many IBIS users.

Thank you!