IBIS Based Buck Converter DC Modeling

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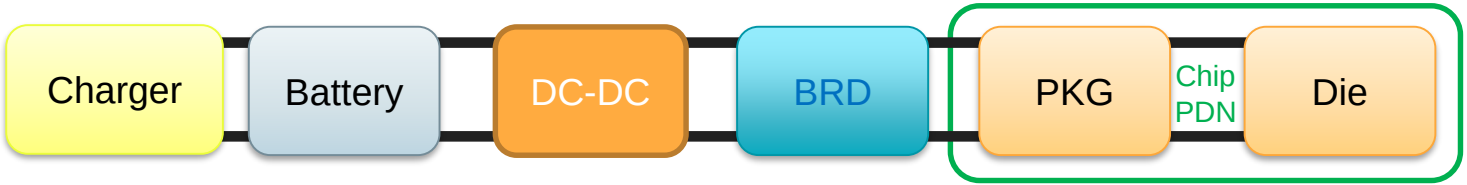
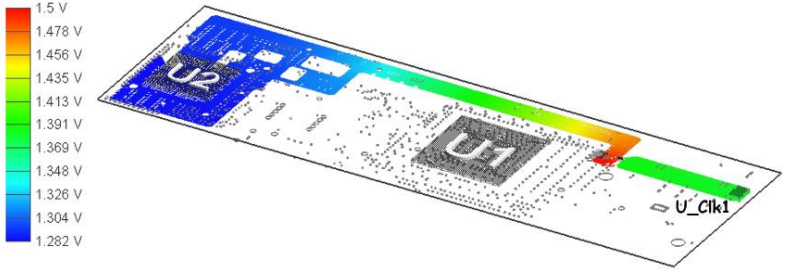
DC Simulation Common Methodology



- Charger & Battery not modeled. Model from DC-DC to Die IR drop.
- DC-DC model as voltage source
- BRD & all the passive components on board as a resistance network
- PKG resistance network
- Die as current sink/load



Common DC Simulation Shortcomings and Proposal

- Shortcomings
  - No DC-DC converter information. No power consumption or power efficiency information.
  - Have to readout and key in current load and voltage source values for all the rails manually. Easy to make a fault.
- Proposal
  - **DC-DC converter vendor to provide detailed chip model in IBIS format to model switching and conduction power loss**.
- Advantage
  - System power consumption and efficiency can be evaluated.
  - With the DC-DC converter IBIS model available, DC simulation for all power rails can be set up automatically.
  - Efficient to optimize the PCB layout.

Proposed Buck Converter IBIS Model Standard Format

The proposed IBIS model includes the following key parameters.

Device physical parameters (from vendor)

Inductor

1) Inductance: L
2) Inductor ESR: R_{L_ESR}

High side switch

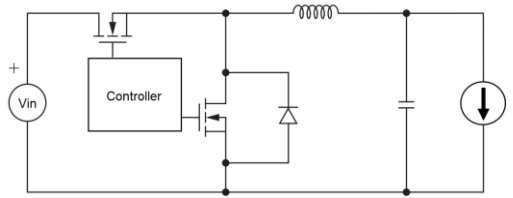
1) Resistance when high side MOSFET is on: R_{on_HS}
2) Rising time and falling time of high side MOSFET: t_{on_HS} and t_{off_HS}
3) FET gate charge on high side MOSFET: $Q_{FET\_G\_HS}$
4) MOSFET output capacitance on high side: C_{oss_HS}

Low side switch

1) Resistance when low side MOSFET is on: R_{on_LS}
2) FET gate charge on low side MOSFET: $Q_{FET\_G\_LS}$
3) Low side body diode charge: $Q_{body\_diode\_LS}$
4) Low side body diode threshold voltage: V_{th}
5) MOSFET output capacitance on low side: C_{oss_LS}

System controlled parameters (from designer)

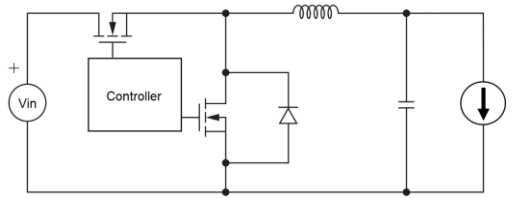
1) Input voltage: V_{in}
2) Output voltage: V_o
3) Output current: I_o
4) Switching frequency: freq
5) Gate drive voltage: V_{GS}
6) Dead time for rising and falling: t_{r_dead} and t_{f_dead}; the dead time is the time to turn off both FETs to avoid shunt through current from power directly to ground.



Referenced Power Consumption Calculation

- The proposed IBIS model parameters are shown in the previous slide. The simulation tool defines how to use these parameters to calculate the power consumption in their own solver. The referenced equations to calculate buck converter power consumption in CCM are shown in the following pages.

- The buck converter power loss mainly comes from three parts: inductor conduction loss, FET conduction loss and FET switching loss. The loss from capacitors are relatively small and are not included. The PCB DCR loss can be obtained from the EDA tool.

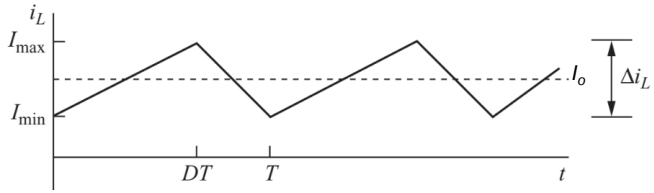


Non-ideal Lossy Buck Converter DC Modeling (1)

The following formulas are for the CCM mode.

- **Inductor conduction loss**: $P_{L\_ESR} = I_{L\_rms}^2 * R_{L\_ESR}$

where $I_{L\_rms} = \text{sqrt}(I_o^2 + I_{L\_delta}^2/12)$ and R_{L_ESR} is the inductor ESR;



I_o is the load current;

$I_{L\_delta} = (V_{in} - V_o) * D / freq / L$;

V_{in} and V_o are input and output voltage for the buck converter, respectively;

D is duty cycle equal to V_o/V_{in};

freq is the switching frequency;

L is the inductance.

Non-ideal Lossy Buck Converter DC Modeling (2)

- **High side MOSFET conduction Loss**: $P_{CL\_HS} = I_{rms\_HS}^2 * R_{on\_HS}$

where R_{on_LS} is conduction resistance on high side FET.

- **High side switching loss**: $P_{SL\_HS} = 0.5 * V_{in} * (I_{L\_min} * t_{on\_HS} + I_{L\_max} * t_{off\_HS}) * freq$

where V_{in} is input voltage; I_{L_min} and I_{L_max} are minimum inductor current ($I_o - 0.5 * I_{delta}$) and maximum inductor current($I_o + 0.5 * I_{delta}$), respectively; t_{on_HS} and t_{off_HS} are rising time and falling time, respectively.

- **High side Gate Drive Loss**: $P_{GDL\_HS} = V_{GS} * Q_{FET\_G\_HS} * freq$

where V_{GS} is the gate drive voltage; $Q_{FET\_G\_HS}$ is the high side MOSFET gate charge.

- **High side FET Coss Loss**: $P_{CL\_HS} = 0.5 * C_{oss\_HS} * V_{in}^2 * freq$

where C_{oss_HS} is the high side MOSFET output capacitance. C_{oss_HS} is equal to $C_{DS} + C_{GD}$.

Non-ideal Lossy Buck Converter DC Modeling (3)

- **Low side MOSFET conduction Loss**: $P_{CL\_LS} = I_{rms\_LS}^2 * R_{on\_LS}$

where $I_{rms\_HS} = sqrt(D) * I_{L\_rms}$;

$I_{rms\_LS} = sqrt(1-D) * I_{L\_rms}$;

I_{L_rms} is the inductor rms current;

R_{on_LS} is conduction resistance on low side FET.

Non-ideal Lossy Buck Converter DC Modeling (4)

- **Low side body diode reverse recovery loss**: $P_{BDRRL\_LS}=V_{in}*Q_{body\_diode\_LS}*freq$

where $Q_{body\_diode\_LS}$ is reverse distributed charge when high side MOSFET is on and reverse bias is applied.

- **Low side body diode conduction loss**: $P_{BDCL\_LS}=V_{th}*(I_{L\_min}*t_{r\_dead}+I_{L\_max}*t_{f\_dead})*freq$

where V_{th} is the diode threshold voltage, 0.7V. t_{r_dead} and t_{f_dead} are the dead time for rising and falling, respectively.

- **Low side gate drive loss**: $P_{GDL\_LS}=V_{GS}*Q_{FET\_G\_LS}*freq$

where $Q_{FET\_G\_LS}$ is the low side MOSFET gate charge.

- **Low side FET Coss loss**: $P_{CL\_LS}=0.5*C_{oss\_LS}*freq*V_{in}^2$

where C_{oss_HS} is the low side MOSFET output capacitance.

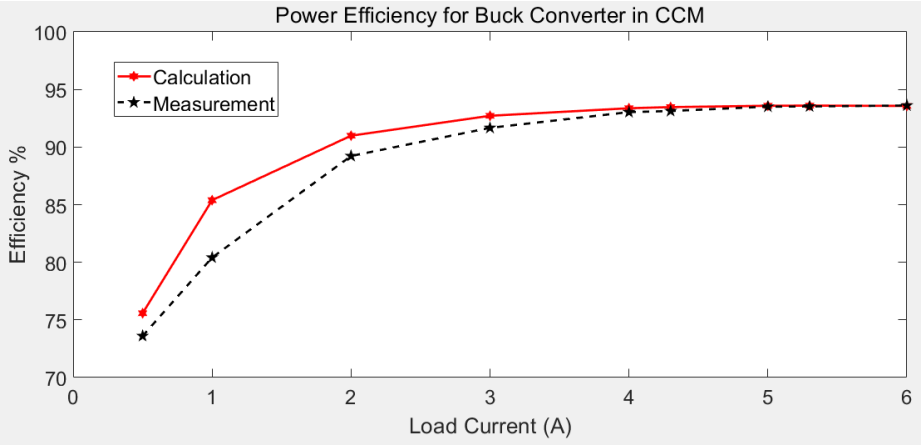
Summary of Buck Converter Power Consumption

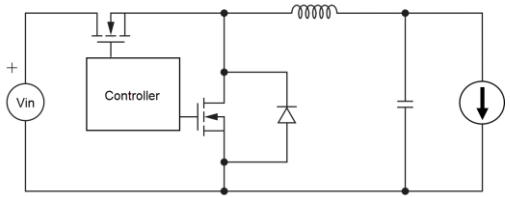
The total power loss is the summation of the inductor DCR loss, the FET conduction loss and the FET switching loss.

Inductor conduction loss	$P_{L\_ESR} = I_{L\_rms}^2 * R_{L\_ESR}$
High side MOSFET conduction loss	$P_{CL\_HS} = I_{rms\_HS}^2 * R_{on\_HS}$
High side switching loss	$P_{SL\_HS} = 0.5 * V_{in} * (I_{L\_min} * t_{on\_HS} + I_{L\_max} * t_{off\_HS}) * freq$
High side Gate Drive Loss	$P_{GDL\_HS} = V_{GS} * Q_{FET\_G\_HS} * freq$
High side FET Coss Loss	$P_{CL\_HS} = 0.5 * C_{oss\_HS} * V_{in}^2 * freq$
Low side MOSFET conduction loss	$P_{CL\_LS} = I_{rms\_LS}^2 * R_{on\_LS}$
Low side body diode reverse recovery loss	$P_{BDRRL\_LS} = V_{in} * Q_{body\_diode\_LS} * freq$
Low side body diode conduction loss	$P_{BDCL\_LS} = V_{th} * (I_{L\_min} * t_{r\_dead} + I_{L\_max} * t_{f\_dead}) * freq$
Low side gate drive loss	$P_{GDL\_LS} = V_{GS} * Q_{FET\_G\_LS} * freq$
Low side FET Coss loss	$P_{CL\_LS} = 0.5 * C_{oss\_LS} * freq * V_{in}^2$

Example: Power Consumption of a Buck Converter

The calculated power loss matches with the measurement.





Device Parameters		Value
Inductor	L	2.2 uH
	R_{L_ESR}	21 mohm
High side switch	R_{on_HS}	7 mohm
	t_{on_HS}	3.4 ns
	t_{off_HS}	2.4 ns
	$Q_{FET\_G\_HS}$	8.9 nQ
	C_{oss_HS}	300 pF
Low side switch	R_{on_LS}	2.1 mohm
	$Q_{FET\_G\_LS}$	33 nQ
	$Q_{body\_diode\_LS}$	5 nC
	V_{th}	0.7 V
	C_{oss_LS}	1100 pF

System Parameters	Value
V_{in}	20 V
V_o	7.7 V
I_o	1 A
freq	1000 kHz
t_{r_dead}	20 ns
t_{f_dead}	20 ns

Other parameters on the board	Value
R_{before_buck}	66 mohm
R_{after_buck}	6 mohm
$I_{controler\_quiescent}$	30 mA

Future Plan

- DCM buck converter DC modeling
- Boost converter DC modeling

Approved IBIS BIRDs related to Power - 1

BIRD #	Title	Status	Statement	Value for this proposal
28.3	Enhancement To The Package Model (.pak file) Specification	Accepted	“The current package model specification describes each pin on a package using lumped L/R/C parameters. Coupling between pins also assumes lumped electrical parameters. However, these description are inadequate when the electrical length of the package elements are greater than ~1/6 of the I/O buffers' rise time. This bird enhances the package description by allowing package elements to be described in terms of length and L, R and C per unit length; i.e. a transmission line representation.”	Can be used for package model format.
38	Maximum Voltage	Rejected	“IBIS can be extended to allow a component supplier specify maximum positive and negative voltages (or currents) that can safely be applied to an I/O buffer”.	Can be extended to all power device current profile format.

Approved IBIS BIRDs related to Power - 2

BIRD #	Title	Status	Statement	Value for this proposal
42.3	Modeling Current Waveforms	Rejected	“Current into the power and ground rails are needed to give a more accurate analysis for ground and power bounce analysis associated with simultaneous switching”.	A similar format can be used to give current profile.
95.6	Power Integrity Analysis using IBIS	Accepted	“Power Integrity Analysis which includes Current switching profile of the Core as well as Simultaneous Switching Noise (SSN) of states of a buffer is to be analyzed through IBIS.”	Can be extended to core power rails too.
125.1	Make IBIS-ISS Available for IBIS Package Modeling	Rejected	“Package modeling in IBIS has numerous serious limitations which make it practically useless for simulations involving modern devices and signaling technologies. However, the IBIS-ISS specification defines useful and much-needed features through a standardized SPICE language. These features would enhance the current package modeling capabilities of IBIS significantly with minimal changes in the specification and little implementation effort in EDA tools.”	Can use IBIS-ISS format for package modeling

Approved IBIS BIRDs related to Power - 3

BIRD #	Title	Status	Statement	Value for this proposal
176	Power Pin Package Modeling	Accepted	“This BIRD enhances IBIS with interconnect modeling features to support broadband, coupled package, and on-die interconnect using IBIS-ISS and Touchstone data. The BIRD also adds a keyword for buffer rail mapping, to link to new terminal definitions defined for buffers”.	Similar interconnect model idea can be applied to system-level modeling.
189.7	Interconnect Modeling Using IBIS-ISS and Touchstone	Accepted	“Under the [Package] keyword, the IBIS specification defines a set of rules on the hierarchy of the various package modeling options. It is clearly stated that when present, the package information under the [Pin] keyword will override the package information in the [Package] keyword, and if present, the information in the [Package Model] and [Define Package Model] keywords will override the information in the [Pin] and [Package] keywords. The Usage Rules of the [Pin Numbers] keyword in the [Define Package Model] keyword section do not prohibit a “partial package model”, i.e., a model which only describes a subset of a Component’s pins. The problem is that there are no rules under the [Pin Numbers] keyword to describe what the EDA tool should do when the keyword doesn't contain the name of a pin that is listed in the component's [Pin] keyword. In the absence of rules, model makers and EDA tool vendors may make different assumptions which may lead to incorrect simulation results. For example, when a pin name is missing under the [Pin Numbers] keyword one EDA tool might make use of the RLC values in the [Pin] or [Package] keyword, while others might implement an open or short instead.”.	Same pin rule can be used as well.

The END