Timing and Electrical Measurement of DDR2 Memory with IBIS 4.1 and AMS

Gary L. Pratt, P.E.
Product Manager
gary_pratt@mentor.com
In the beginning …

- There was SPICE … and it was sssllloooowwv but nobody cared, because hey … time didn’t exist yet
- Then, there was time …
  - But, never quite enough
- Then, there was IBIS
  - and, it was good, and simple to use, and saved much precious time
- Then, came new technology
  - which brought a plague of new keywords across the land
- Then, IBIS grew large and unwieldy
  - and slow to respond to new technologies
- Then, the IBIS wise-men … errrr …wise-people said
  - let there be AMS
- And, then there was AMS
  - and it was very good
- Then, the masses rejoiced & created multitudes of innovation
  - some of which not even the wise-people had foretold …
Behold …

AMS

for

DDR2 Electrical

and

Timing Measurement
DDR2 Electrical and Timing Measurement Requirements

- absolute overshoot
- overshoot area
- slew rate
- monotonicity
- crossing zone
- runt pulse
- min pulse width
- undershoot area
- absolute undershoot

- absolute overshoot
- overshoot area
- pos set runt pulse
- undershoot area
- pos setup tangent
- absolute undershoot
- pos hold tangent
- neg setup tangent
- neg hold tangent
- neg hld runt pulse
- pos derated setup
- pos derated hold
- neg derated setup
- neg derated hold
- undershoot area
- absolute undershoot

V_{DDQ}

V_{IH(ac)} min

V_{IH(dc)} min

V_{REF} to ac region

nominal line

tangent line

tangent line

Delta TF

Delta TR

DDC Measurement with IBIS 4.1 and AMS

LIFE FUNCTIONS CRITICAL
IBIS 4.1 Measurement Model

*But, where do violation messages go?
IBIS 4.1 Measurement Model

*But, where do violation messages go?
Measurement Model in IBIS 4.1 Functional SI

IBIS 4.1 CPU Model

- CPU Digital HLD Model
- IBIS 3.2 Model

... DQS ... DQ0 ... Analog Simulation

Printed Circuit Board

Digital Simulation

IBIS 4.1 Memory Model

- DDR2 Measurement Model
- IBIS 3.2 Model
- DDR2 Memory Digital HLD Model

Msgs * But, where do violation messages go?

DDR2 Measurement with IBIS 4.1 and AMS

*But, where do violation messages go?
IBIS 4.1 Memory Model

**How to deal with single-clock, multiple data?**

<table>
<thead>
<tr>
<th>Pin</th>
<th>signal_name</th>
<th>model_name</th>
<th>R_pin</th>
<th>L_pin</th>
<th>C_pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DQ0</td>
<td>NC</td>
<td>0.043</td>
<td>5.22nH</td>
<td>1.26pF</td>
</tr>
<tr>
<td>2</td>
<td>CK</td>
<td>NC</td>
<td>0.030</td>
<td>2.76nH</td>
<td>0.91pF</td>
</tr>
<tr>
<td>3</td>
<td>CK#</td>
<td>NC</td>
<td>0.029</td>
<td>2.73nH</td>
<td>0.86pF</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Diff_pin</th>
<th>inv_pin</th>
<th>vdiff</th>
<th>tdelay_typ</th>
<th>tdelay_min</th>
<th>tdelay_max</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>3</td>
<td>.360V</td>
<td>0ns</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

[EXTERNAL MODEL]

**node declarations**
DQ0 CLK CLK_N GND VDD

[circuit call] dq_full_input
Port_map A_signal 1
Port_map D_receive DQ0
...
[end circuit call]

[EXTERNAL MODEL]

**node declarations**

[circuit call] clk_input
Port_map A_signal 2
Port_map D_receive CLK
...
[end circuit call]

[circuit call] clk_input
Port_map A_signal 3
Port_map D_receive CLK_N
...
[end circuit call]

[EXTERNAL MODEL]

**node declarations**

[circuit call] DQS_DQ_CHECK
Port_map DQ 1
Port_map DQS_p 2
Port_map DQS_n 3
...
[end circuit call]

[EXTERNAL MODEL]

**node declarations**

[circuit call] DQS_DQ_CHECK
Port_map DQ 1
Port_map DQS_p 2
Port_map DQS_n 3
...
[end circuit call]

*How to deal with single-clock, multiple data?*
*How to deal with multiple speed grades?
**TANGENT MEASUREMENT**

Wait for vref crossing
Store data points
Wait for vix_ac cross
Calculate the slope from each point to the vix_ac crossing point
Return the maximum slope
Wait for vix_dc crossing
Calculate the slope from each subsequent point back to the vix_dc crossing
Wait for vref crossing
Return the max slope

*But, “ASP” isn’t an IEEE-1076.1 standard.*

(error and exception handling removed for clarity)
Absolute and Area Over/Undershoot

Create events on crossings
Wait for a crossing into the overshoot or undershoot area
While in the over/undershoot area, integrate the area under the curve
At any time, if the maximum area is exceeded, generate an violation message
Notice: “REF” is included in each message
Error if absolute limit is exceeded

*But, how to get “REF” into the model?

begin
vdd_cross <= vin'above(VDDQ);
vss_cross <= vin'above(0.0);
max_cross <= vin'above(VDDQ+MAXOVERSHOOT);
min_cross <= vin'above(0.0-MAXUNDERSHOOT);
process
  variable area : real := 0.0;
  variable last_asp : real;
begin
  wait until vdd_cross or not vss_cross; 
  area := 0.0; last_asp := now;
  while vdd_cross or not vss_cross loop
    wait on ASP;
    if vin < 0.0 then area := area + (0.0-vin)*(now-last_AsP); end if;
    if vin > VDDQ then area := area + (vin-VDDQ)*(now-last_AsP); end if;
    if area > MAXOVERSHOOTAREA or area < MAXUNDERSHOOTAREA then
      REPORT REF"Violation - Exceeded Overshoot or Undershoot Area";
      exit;
    end if;
    last_asp := now;
  end loop;
end process;
process (max_cross, min_cross) begin
  if max_cross or not min_cross then
    REPORT REF"Violation - MAXOVERSHOOT or MAXUNDERSHOOT Level Exceeded";
  end if;
end process;
end architecture;
Setup Violation Check

-- Check the setup timing
check_setup: process (dqs_slope'transaction)
  variable derating : time := 0*sec;
  variable expected, actual : line;
begin
  derating := interp_derating_table(dqs_slope, setup_slope, SETUP, REF);
  if setup_time = 0.0*sec then
    REPORT REF"Setup Violation -- DQ transition in progress during DQS event";
  elsif derating /= time'left then
    if (now-dqs'last_event) - setup_time < tDS_base+derating then
      write(expected,tDS_base+derating,left); write(actual,(now-dqs'last_event)-setup_time,left);
      REPORT REF"Setup Violation, Expected: "&expected.all". Actual: "&actual.all;
    end if;
  end if;
end process;

Trigger the process after each DQS slope is determined (VIXACMAX-0.50*VDDQ)
Read and interpolate the derating chart according to DQ and DQS slew rate
If DQ is in transition (setup_time=0), report a violation
If derating is valid, check the setup time
If actual setup time is less than derated setup specification, report violation

(error and exception handling removed for clarity)
Timing Analysis with IBIS 3.2 Models
(adjusting pin-to-pin specs to die-to-die timing)

Adjustments to Digital Output Timing:
\[ t_{QSQ}(actual) = t_{QSQ}(spec) + (\Delta t_1 - \Delta t_4) \]

Adjustments to Digital Input Timing:
\[ t_{DS}(actual) = t_{DS}(spec) + (\Delta t_2 - \Delta t_3) \]
\[ t_{DH}(actual) = t_{DH}(spec) + (\Delta t_3 - \Delta t_2) \]

Rising and falling \( \Delta t \) measured with databook load for each process corner.

*Can \( \Delta t \) be made standard between models and tool vendors?
Timing Analysis with IBIS 3.2 Models
(compensating for delay in IBIS 3.2-models)

Adjustments to Propagation Delay:
\[ t_{PCQ\ (actual)} = t_{PCQ\ (spec)} - (\Delta t_1 + \Delta t_4) \]

Adjustments to Setup and Hold:
\[ t_{SU\ (actual)} = t_{SU\ (spec)} + (\Delta t_3 - \Delta t_2) \]
\[ t_{H\ (actual)} = t_{H\ (spec)} + (\Delta t_2 - \Delta t_3) \]

*Can \( \Delta t \) be made standard between models and tool vendors?
Timing Analysis with IBIS 3.2 Models

No adjustment needed when measuring at pins

IBIS 3.2 Model

DQS

IBIS 3.2 Model

DQ0

Printed Circuit Board

DDR2 Measurement Model

IBIS 3.2 Model

IBIS 3.2 Model

IBIS 3.2 Model
Trace Routing Budget

IBIS 4.1 Memory Model

DDR2 Measurement Model

Timing Slack Data *

IBIS 3.2 Model

IBIS 3.2 Model

IBIS 3.2 Model

IBIS 3.2 Model

*But, how to get slack data into layout tool?
*What slew value to use?
IBIS 4.1 and IEEE 1076.1

- Global -- Open Industry Standard
  - Portable between IBIS4.1-1076.1 simulators
- Complete Automation
  - No user intervention required
  - violation messages pinpoint problems
- Tests all connections in one simulation
  - All 180 cpu→mem and 128 mem→cpu nets in one step
- Modeling Engineer is in complete control
  - No need to involve the IBIS committee or EDA vendors to add new functions or features
Future Applications

- Automated PCI Express Test Suite?
- ????
Next Steps

- **EDA Vendors**
  - Support IBIS 4.1 AMS

- **Silicon Vendors**
  - Develop and Release IBIS 4.1 AMS models

- **PCB Engineers**
  - Demand the benefits of IBIS 4.1 AMS
    - Accept no substitutes

- **IBIS Committee**
  - Stay tuned for Ian’s presentation
Thanks to

- Randy Wolfe and his associates at Micron for advice on interpreting the JEDEC DDR2 specification and moral support in developing this measurement model.
- Todd Westerhoff for help using IBIS 3.2 models in timing analysis.