Buffers for Advanced SPICE to IBIS Testing

Bob Ross
IBIS Summit Meeting
Design Automation Conference 2006
San Francisco, California
July 25, 2006
Configurable CMOS & ECL Buffers

- Two buffers for all Model types, voltages, clamps and on-die terminators (ODTs)
- Berkeley SPICE to support all SPICEs
  - Level 2 CMOS, standard bipolar ECL & simple diodes
  - Numerical nodes
  - Syntax-neutral multiplier switched conductance
    - GPDSW 30 31 POLY(2) (30,31) (21,0) 0 0 0 0 1000
    - RPDSW 30 31 1G
      - Open: R = 1 GΩ
      - Closed: G = 1000 S (0.001 Ω)
- Externally set 0 and 1 voltage assignments
  - Could be parameterized
- Multiple cases through s2ibis and scripts
Diode Clamps, 50 Ω ODTs and configurations switches

Enable and Model_type configuration switches
CMOS Configuration Controls

.SUBCKT CMOSTEST

*****************************************************************************
* ON-OFF CONFIGURATION SWITCHES
* (1 OR ABOVE = ON, 0 = OFF)
*****************************************************************************

* VPD 1 PULLDOWN
* VPU 1 PULLUP
* VGC 1 GND CLAMP
* VPC 1 POWER CLAMP
* VGCR 0 INTERNAL GND CLAMP RESISTOR (50 ohm)
* VPCR 0 INTERNAL POWER CLAMP RESISTOR (50 ohm)

*****************************************************************************

<table>
<thead>
<tr>
<th>Model_type plus Enable Control</th>
</tr>
</thead>
</table>

Diode Clamps and 50 Ω ODTs

Enable with Model_type

*****************************************************************************

| Control | Voltage References | Configuration Switches (1 = ON) |
| I/O, Input and Enable | I/O, IN, EN | PD, PU, GC, PC |

Model_type, Clamps and ODT Config.
Switches (Berkeley SPICE)

* CONFIGURATION CONTROL SWITCHES---|
  * Pulldown and Pullup
  GPDSW  30  31  POLY(2)  (30,31)  (21,0)  0 0 0 0 1000
  RPDSW  30  31  1G
  GPUSW  32  30  POLY(2)  (32,30)  (22,0)  0 0 0 0 1000
  RPUSW  32  30  1G
  * Gnd Clamp and Power Clamp
  GGCSW    1  33  POLY(2)  (1,33)  (23,0)  0 0 0 0 1000
  RGCSW    1  33  1G
  GPCS W   34   1  POLY(2)  (34,1)  (24,0)  0 0 0 0 1000
  RPCS W   34   1  1G
  * Gnd Clamp Resistor and Power Clamp Resistor
  GGCRS W   1  35  POLY(2)  (1,35)  (25,0)  0 0 0 0 1000
  RGCRSW   1  35  1G
  GPCRS W  36   1  POLY(2)  (36,1)  (26,0)  0 0 0 0 1000
  RPCRSW  36   1  1G
  * Enable
  GENS W   30   1  POLY(2)  (30,1)  (3,0)  0 0 0 0 1000
  RENS W   30   1  1G
[Pulldown]s for Several Model_types

Power and Gnd Clamps

I/O and OD

Output

Extra substrate diode in PMOS for I/O and Output versus Open_drain (OD)
Diode and ODT – Test I-V Processing and SPICE to IBIS Methods

One method based on chopping the I-V tables

Better tables based on “DEC” (Deviate, Extrapolate, Calculate)
Diode and ODT – Corresponding IBIS Model Plots

“DEC” IBIS plots show extended range

Chopped – can cause double counting of ODT currents in some EDA tools
DEC and Some Other Choices from Ross, 9/2005 ODT Presentation

Clip and Extend
52.8 Ω

Default DEC
94.2 Ω and 120 Ω

[Gnd Clamp] Shape

[Power Clamp] Shape
ECL (PECL) Buffer

[Diagram of an ECL (PECL) Buffer with labels and connections]
**ECL (PECL) Configuration Control**

قود: ECLTEST

<table>
<thead>
<tr>
<th>Control</th>
<th>Voltage</th>
<th>Configuration</th>
<th>Switches (1 = ON)</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O</td>
<td>Inputs</td>
<td>References</td>
<td>23 24 25 26 27</td>
</tr>
<tr>
<td>IN</td>
<td>EN</td>
<td>PU GC PC</td>
<td>GC PC GCR PCR R50</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3K 2K 50_2V</td>
<td></td>
</tr>
</tbody>
</table>

- **ON-OFF CONFIGURATION SWITCHES**
  - (1 OR ABOVE = ON, 0 = OFF)

- **VGC** 1 GND CLAMP
- **VPC** 1 POWER CLAMP
- **VGCR** 0 INTERNAL GND CLAMP RESISTOR (3K ohm)
- **VPCR** 0 INTERNAL POWER CLAMP RESISTOR (2K ohm)
- **VTERM** 0 INTERNAL 50 OHM TERMINATOR TO VCC - 2

**Diode Clamps, 2 kΩ and 3 kΩ ODTs, and 50 Ω Internal Terminator**

Enable (ECL/PECL voltage levels require EN voltage shifts so that “0” is off)
Extraction Tests

- CMOSTEST and ECLTEST for advanced extraction testing
  - All Model_type configurations
  - Voltage reference settings
  - Clamps and internal ODT
    - Double counting
    - Truncation of tables
  - Differential models though subcircuit calls
  - Typ-Min-Max alignment
- Does any s2ibis tool consider all these cases??
  - Otherwise need several passes and hand calculations
- Not covered
  - Submodel modes (for example: DDR2 ODT)
  - Pre-emphasis - [Driver Schedule] partitioning