

Serdes Introduction and AMS modelling

Richard Ward
Serdes Engineering (ASIC)
25-July-2006



Outline

- Serdes Introduction
- AMS Model Approach

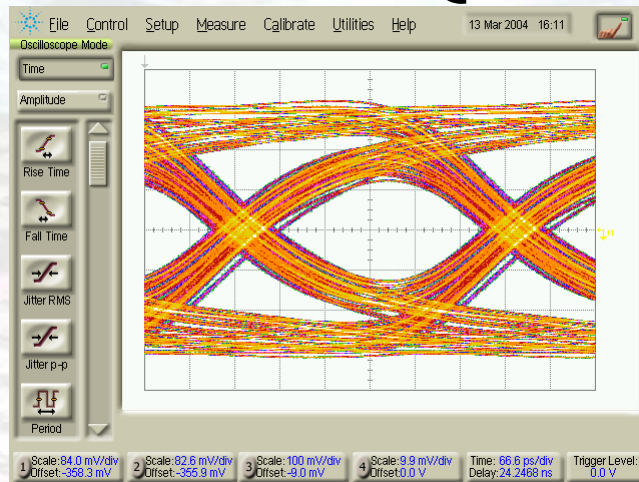
- **Which Standard would you like to follow?**
 - 802.3ap (10G Ethernet over backplane)
 - OIF CEI 6G (short and long reach)
 - OIF CEI 11G (short and long reach)
 - PCI-Express (2.5G gen1, 5G gen2)
 - XAUI (3.125G)
 - Serial ATA (3.125G)
 - FBDIMM/2 (4.8/6.4/8/9.6G)
 - SerialRapidIO, (1.25/2.5/3.125G)
 - Infiniband
 - FibreChannel
 - ...



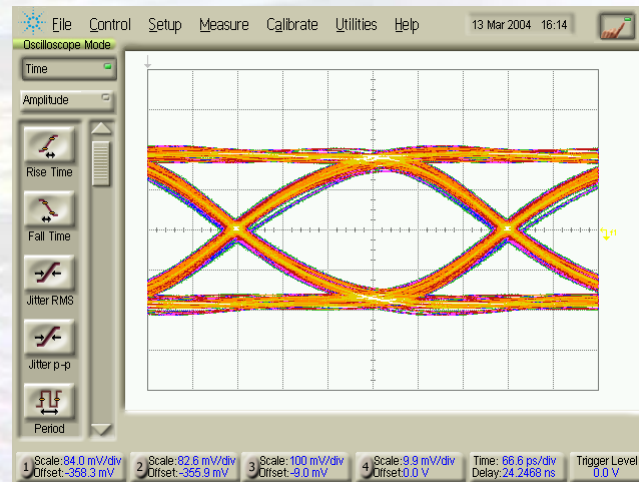
What is the problem to solve?

- 3.125Gbps

No EQ

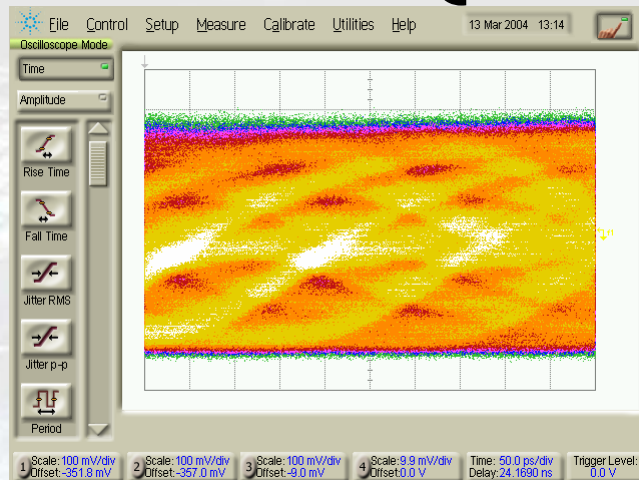


Tx FIR

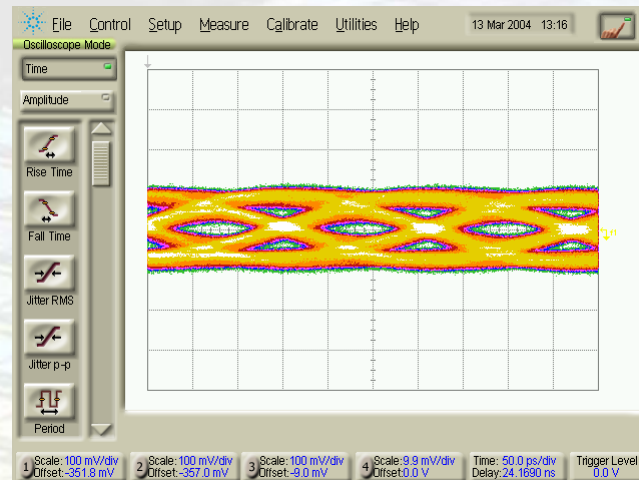


- 6.25Gbps

No EQ



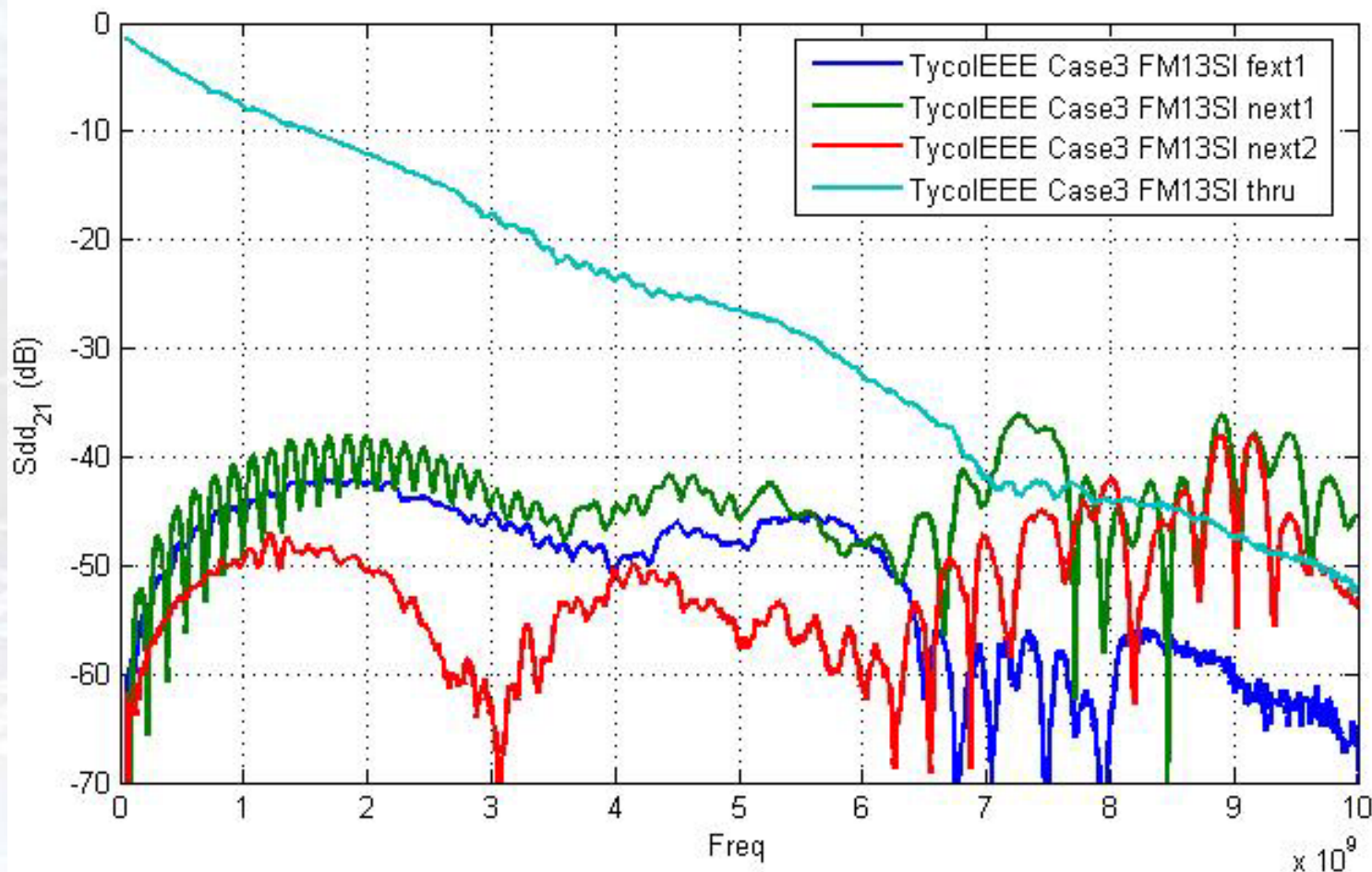
Tx FIR



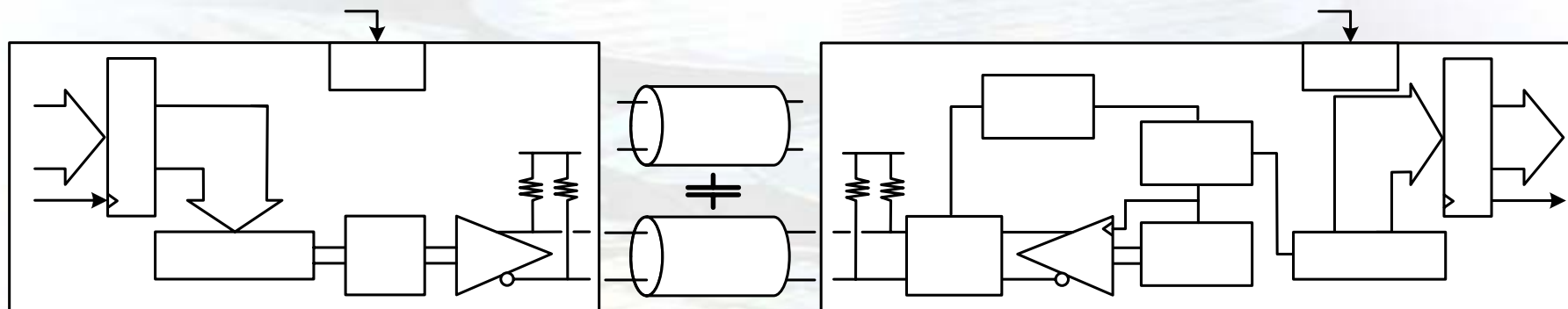
~40" FR4 o/p

Example Channel

- Typical channel for 5 to 10Gbps (~40" FR4)



Typical SerDes Block Diagram



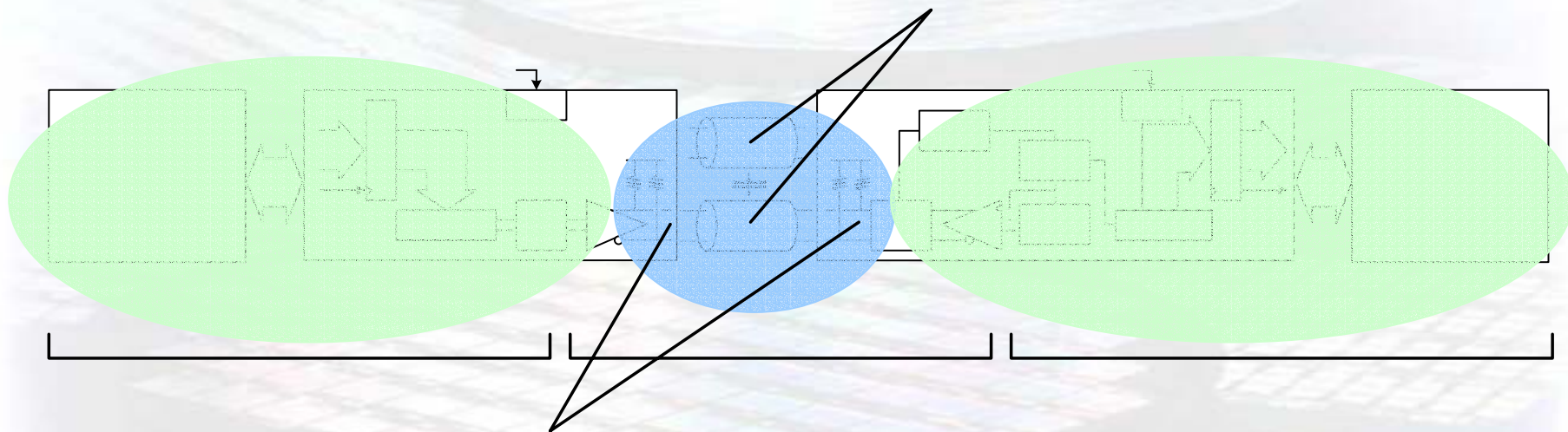
- Differential data has Clock and Data embedded into a serial stream. Most are NRZ/binary.
- Keys parameters are:
 - Jitter generation (Tx) and jitter tolerance (Rx)
 - Equalization ability (both Tx and Rx sides) and adaption
 - Asynchronous tracking rate of Rx
 - PLL jitter rejection (from Refclk and chip/system noise)
- Most higher rate systems are Rx DFE (analog or digital)

Refclk

PLL

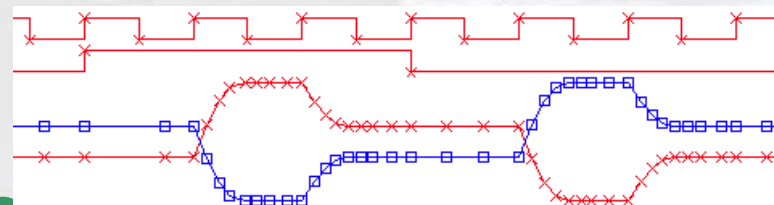
Data

How would an AMS model fit?



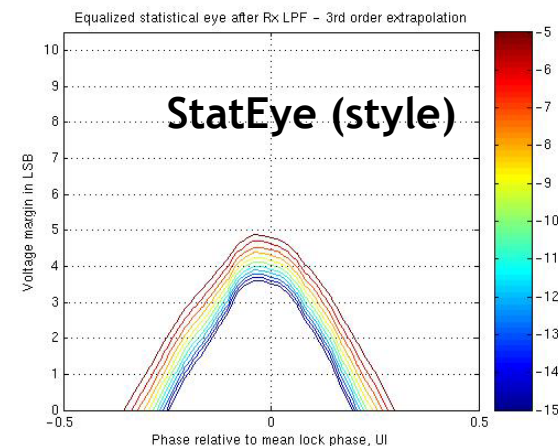
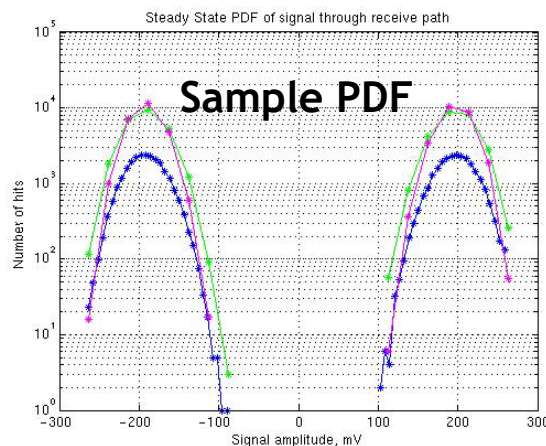
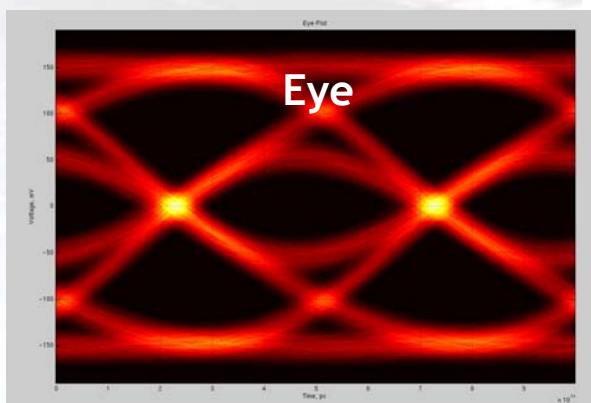
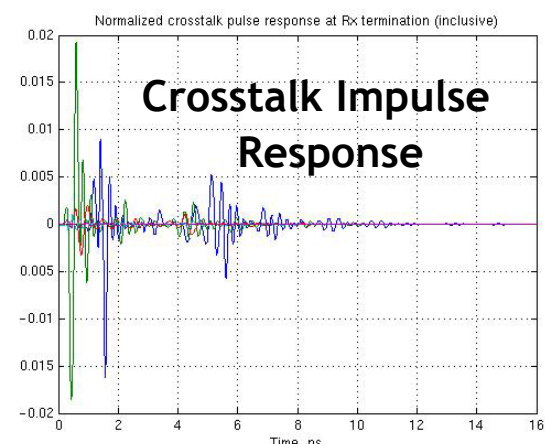
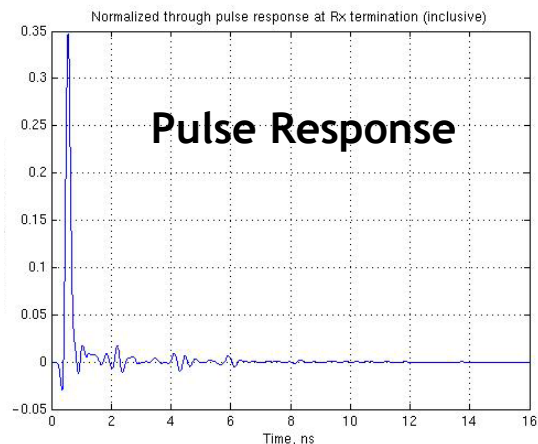
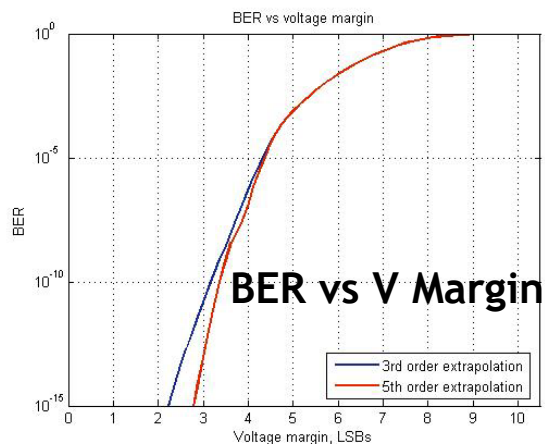
Different model requirements:

- Architectural analysis
- Customer SI and Interoperability
- Steady-state performance sims
- Higher levels of system integration than previously needed (AMS extending into the RTL/packet processing world)



Logical Level

Performance Metrics





AMS Model Approach

- **Benefits**

- Electrically aware
- Integration with chip and board design systems
- RTL level simulation interface
- Standard EDA toolset/languages

- **Drawbacks**

- Performance!
 - we believe this is the technical problem to solve
- Framework of statistical extrapolation from the time domain
- CAD license tie-up