IBIS Algorithms Revisited

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Previous Work

• Based on early prototype work
• Updated from hand-drawn foils given in June 1997 and presentation in Oct. 1998
• Presented at SPI 2003 in Siena, Italy
IBIS Algorithms

• IBIS data AND how processed
  – Older approaches give different solutions
  – Two-waveform algorithm gives good solutions

• Other algorithms
  – Multiple tables and dynamic interpolation
  – I/O Interface Model for Integrated Circuit (IMIC) for transistor multiple I-V and capacitance-V table interpolation
  – Radial based functions (RBF)
General IBIS Buffer Model

Drivers

- [Pullup]
- [Pullup Reference]
- [Pulldown]
- [Pulldown Reference]
- Rise & Fall Transitions

Fixed Clamps and C_comp

- [Power Clamp Reference]
- [Gnd Clamp Reference]
- [Power Clamp]
- [Gnd Clamp]
- C_comp
- GND

Package

- L_pin
- R_pin
- Pin
- C_pin
- GND
Example - Ideal CMOS Buffer

\[ v_0 = \frac{25t}{6} \]

- 5 V Open Swing
- \( R_H = 10 \Omega \)
- \( R_L = 50 \Omega \)
- 1 ns Output Ramp

50 \( \Omega \) Load to GND

50 \( \Omega \) Load

GND
Thevenin Linear Z Transitions

\[ v_0 = \frac{25t}{10 - 4t} \]

\[ v_0 = \frac{5t + 20t^2}{2 + 4t} \]

\[ R(t) = 50 - 40t \]
\[ G(t) = 0.02 + 0.08t \]
\[ v(t) = 5t \]
\[ v_0 = \frac{25}{6} \text{ V} \]
\[ G(t) \]
\[ 50 \Omega \]
\[ 0 \text{ V} \]
\[ 25/6 \text{ V} \]

\[ 0 \text{ ns} \]
\[ 1 \text{ ns} \]
Norton Linear Y Transitions

\[ v_0 = \frac{125t - 100t^2}{10 - 4t} \]
\[ v_0 = \frac{25t}{2 + 4t} \]

\[ R(t) = 50 - 40t \]
\[ G(t) = 0.02 + 0.08t \]
\[ i(t) = 0.5t \]

\[ v_0 = \frac{25}{6} \text{ V} \]
\[ R(t) = 50 \Omega \]
\[ G(t) = 0.02 + 0.08t \]
\[ i(t) = 0.5t \]
IBIS Linear Table Multipliers

\[ v_0 = \frac{25t}{2 + 4t} \]

\[ i_2 = t \frac{(5 - v_0)}{10} \]
\[ i_1 = (1 - t) \frac{v_0}{50} \]

Same as Norton:
\[ G(t) = 0.02 + 0.08t \]
\[ i(t) = 0.5t \]
\[ i_2(v_0) \]
\[ i_1(v_0) \]

\[ 5 \text{ V} \]
\[ 0 \text{ V} \]
\[ 25/6 \text{ V} \]
\[ 50 \Omega \]
Dual IBIS Linear Table Multipliers

\[ v_0 = \frac{25t}{10 - 4t} \]

\[ v_2 = t (5 - i_0 10) \]
\[ v_1 = -(1 - t) i_0 50 \]

Same as Thevenin:
\[ R(t) = 50 - 40t \]
\[ v(t) = 5t \]
Dependent IBIS Table Multipliers

\[ k_2 = \frac{t}{3 - 2t} \]

\[ v_0 = \frac{25t}{6} \]

\[ i_2(v_0) \]

\[ i_1(v_0) \]

\[ 1 - k_2(t) \]

\[ 50 \, \Omega \]

\[ GND \]

\[ 25/6 \, V \]

\[ 25t \]

\[ 6 \]

\[ 0 \, V \]

\[ 5 \, V \]

\[ 0 \, ns \]

\[ 1 \, ns \]
Independent IBIS Table Multipliers

\[ v_0 = \frac{25t}{6} \]

\( k_2, k_1 \) Independent from second waveform load and solution of two equations

\[ i_2(v_0) \quad k_2(t) \]

\[ i_1(v_0) \quad k_1(t) \]

\( 50 \Omega \)

\[ 25/6 \text{ V} \]

\[ 0 \text{ V} \]

\[ 0 \text{ ns} \quad 1 \text{ ns} \]
Actual Waveforms and Multipliers
Generalized Test Load

\[ V(t) \text{ and } I(t) \text{ can be calculated from load information} \]
Feedback Ku, Kd solutions using waveform errors

Load 1

Load 2

SPICE Prototype for Ku(t), Kd(t)
Feedback SPICE Circuit For Two Non-linear/Table Equations

* F E E D B A C K  T A B L E  A D J U S T M E N T  ..............................................
GDET  NDET  GND  CUR='(i (VDN2) *i (VUP1) -i (VDN1) *i (VUP2))/(1E7)'
VDET  NDET  GND  0
*  
GKUR  NKU  GND  
+  CUR='((v(IN2) -v(PIN2)) *i (VDN1) - (v(IN1) -v(PIN1)) *i (VDN2))/i (VDET)'
VKUR  NKU  GND  0
*  
GKDR  NKD  GND  
+  CUR='((v(IN1) -v(PIN1)) *i (VUP2) - (v(IN2) -v(PIN2)) *i (VUP1))/i (VDET)'
VKDR  NKD  GND  0
*  

- \( V1(t)/Z(t) = Ku(t)*i_u(V1(t)) + Kd(t)*i_d(V1(t)) \)
- \( V2(t)/Z(t) = Ku(t)*i_u(V2(t)) + Kd(t)*i_d(V2(t)) \)
Part of SPICE Encoded
IBIS Prototype

* HIGH SIDE
XUP    OUT1  VCC  NU1  PULLUP
VUP    NU1  VCC  0
GUP    OUT1  VCC  CUR=’-I(VUP)*(I(VKUR)*I(VON)+I(VKUF)*(1-I(VON)))’
XPC    OUT1  VCC  POWER_CLAMP
*

* LOW SIDE
XDN    OUT1  GRD  ND1  PULLDOWN
VDN    ND1  GRD  0
GDN    OUT1  GRD  CUR=’-I(VDN)*(I(VKDR)*I(VON)+I(VKDF)*(1-I(VON)))’
XGC    OUT1  GND  C_COMP
*

* C_COMP AND DUT PACKAGE
XCAP    OUT1  GRD  C_COMP
XPKG    OUT1  GRD  PIN1  PACKAGE
*

* LOAD
TLOAD  PIN1  GRD  PIN9  GRD  Z0=50  TD=1N
RLOAD  PIN9  GND  50G
*

* VOLTAGE CONTROL (AMPLITUDE (0 TO 1), PULSE WIDTH & PERIOD)
VPULSE STEP  GRD  0  PULSE (1 0 0P 1P 1P 5N 10N)
Recommended Test Load, Industrial usage

Recommended Loads:
- 50 Ω to Vcc
- 50 Ω to Gnd
Problems and Limitations

• Ground, power currents a function of the model, may not be accurate
  – Gate modulation effects
  – Could be fixed with more tables or parameters

• Timing to internal buffer nodes

• Frequency dependent impedance models

• Delay timing errors with over-clocking - shown next
Over-clocking Problem with IBIS, No Simple Solution for Delays
Conclusions

• Well constructed IBIS models and good algorithms yield accurate results
• However, there are limitations