Case study of IBIS V4.1
by
JEITA EDA-WG

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JEITA ; Japan Electronics and Information Technology Industries Association

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Outlines

1. JEITA EDA-WG Activities
2. Case study of IBIS V4.1
3. EMI Model
1. JEITA EDA-WG Activities
Objectives of JEITA EDA

EDA Model for

Digital Consumer Electronics
Cellular Phone, LCD TV, Digital Camera/Video, DVD Recorder
(Digital, RF, and Analog circuits)

Auto Mobile Electronics?
(Motor Drive, EMC)

< Applicability of IBIS V4.1 >
EDA Model for SI, PI and EMI Simulation

- PCB
- FPC
- RF Modules
- Passive Component (LCR, Filter)
- Connectors
- Display device
- Discreet Semicon
- Cables
- LSI Model
  - IC Chip
  - IC Package
- Crystal Oscillator

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ICs
IC Package
Discrete Semiconductors
Crystal Oscillator
RF Modules
Connectors
Cables
Passive Components (LCR, Filter)
PCB
FPC
EDA Models
For
Digital Consumer electronics
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2. Case study of IBIS V4.1
## Summary of investigation of IBIS V4.1

<table>
<thead>
<tr>
<th>Component</th>
<th>IBIS V3.2</th>
<th>IBIS V4.1 SPICE</th>
<th>IBIS V4.1 *AMS</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ASIC/SOC for EMI/SSO</strong></td>
<td>✓</td>
<td>✓</td>
<td>(✓)</td>
<td>Accurate models need the internal gates for EMI/SSO. IBIS V4.1 SPICE discloses process parameters.</td>
</tr>
<tr>
<td><strong>Power Semiconductor OpAMP</strong></td>
<td>✓</td>
<td>✓</td>
<td>(✓)</td>
<td>IBIS V4.1 SPICE discloses process parameters.</td>
</tr>
<tr>
<td><strong>DSP, AD/DA, Xtal</strong></td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>I/O for SI can be described in V3.2. Inside needs *AMS.</td>
</tr>
<tr>
<td><strong>Passive Components</strong></td>
<td>✓</td>
<td>✓</td>
<td>(✓?)</td>
<td>Can describe LCRK models ICM describes S-parameters</td>
</tr>
<tr>
<td><strong>Package, Module, PCB</strong></td>
<td>✓</td>
<td>✓</td>
<td>(✓?)</td>
<td>IBIS 4.1 SPICE can’t describe S-parameters or lossy coupled transmission line. ICM can’t include discrete components. SiP and PWRGND modeling.</td>
</tr>
<tr>
<td><strong>Connector, Cable, FPC</strong></td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>ICM can’t include discrete components.</td>
</tr>
</tbody>
</table>

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Understanding of IBIS V4.1

IBIS excludes IMIC

IBIS excludes IMIC

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How to describe SPICE transistor model in IBIS 4.1 without disclosing proprietary information

Models described in SPICE transistors have flexibility.

Net List → Equivalent Circuit (Macro Model) using Transistor Models

Transistor Parameters → IBIS V4.1 allows to use SPICE3 but discloses process parameters

IMIC (Table_SPICE) allows to hide the transistor parameters, but IBIS V4.1 excludes IMIC.
How to hide transistor model parameters in IBIS V4.1 SPICE description without losing accuracy

IMIC (Table_SPICE) allows to hide the transistor parameters, but IBIS V4.1 excludes IMIC.

Need to have a bridge from IMIC to IBIS V4.1 SPICE 3 without disclosing the original SPICE transistor parameters.
3. EMI Model (NEC/APSIM)
RF Current of LSI

1. Measurement; IEC61967-6. Magnetic Probe Method
2. Simulation Model; EMI Model for LSI
EMI simulation needs the internal gates power/ground model with loading effects in time/frequency domain.

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Current Waveforms of 32-bit LSI

Output

Internal

Total

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Measurement

IEC61967-6. Magnetic Probe Method

- Spectrum analyzer
- Pre-amplifier (option)
- Magnetic probe
- Magnetic field
- LSI
- IC test board
- Decoupling capacitor
- Current
- Power supply

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Simulation VS Measurement

![Graph showing comparison between Simulation and Measurement]
Current/Magnetic Field Distribution

Simulation

Measurement

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EMI Simulation Model for LSI

Power and Ground Model of Core Logics (internal gates)

IBIS 4.1

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Developed IMIC to IBIS V4.1 Converter

Any SPICE

Table_SPICE Generator

Table_SPICE

Any SPICE ↔ Table_SPICE Generator

Table_SPICE to SPICE 3 MODEL3 Converter

SPICE 3 LEVEL=3

IMIC

The parameters of LEVEL=3 can’t disclose those of the original SPICE.

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Full chip power/ground current models in time/frequency domain for EMI Simulation
Example of LSI Power/Ground Model (IBIS V 4.1)

Apsim LSI Power and Ground model ckt file
* Command: ApsimLPG 1.400.5
* File: big.ckt
* Pre - Driver Model
  xPREDRY.in PreVDD PreVSS PreIN PreMID PRDRV.in
  xPREDRV.out PreVDD PreVSS PreMID PreOUT PRDRV.out
  vzd1 PreVDD 0 dc 3.3
  vss1 PreVSS 0 dc 0.0
  xshort1 PreOUT D2P_N0039026 D2P_N0000004 D2P_N0000003 D2P_N0000002 D2P_N0000001 short1
* Clock - Driver Model
  cD2P_N0039026_1 D2P_N0039026 VDD 2.192774e-013
  cD2P_N0039026_2 D2P_N0039026 VSS 2.192774e-013
  xD2P_10033331.in VDD VSS D2P_N0039026 mid_D2P_10033331 F111.in
  xD2P_10033331.out VDD VSS mid_D2P_10033331 D2P_N0029114 F111.out
  cD2P_10029114_1 D2P_10029114 VDD 5.332500e-013
  cD2P_10029114_2 D2P_10029114 VSS 5.332500e-013
  xD2P_10033330.in VDD VSS D2P_10029114 mid_D2P_10033330 F111.in
  xD2P_10033330.out VDD VSS mid_D2P_10033330 D2P_10029992 F111.out
  cD2P_10029992_1 D2P_10029992 VDD 3.680150e-015
  cD2P_10029992_2 D2P_10029992 VSS 3.680150e-015
  xD2P_10033329.in VDD VSS D2P_10029992 mid_D2P_10033329 F111.in
  xD2P_10033329.out VDD VSS mid_D2P_10033329 D2P_10028891 F111.out
  cD2P_10028891_1 D2P_10028891 VDD 8.436000e-016
  cD2P_10028891_2 D2P_10028891 VSS 8.436000e-016

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Example of LSI Power/Ground Model (IBIS V 4.1)

1. Original SPICE MOS parameters

```
.model NENH NMOS
+ LEVEL       =
+ LMIN        =
+ VFB         =
+ VDOP        =
+ TCX         =
+ PHI         =
+ GAMMA       =
+ GDOP        =
```

2. Table_SPICE MOS V-I-C data

```
.model NENH nmos model=table
+ I=0.25u w=2u pd=5e-6 ps=5e-6 ad=0.5e-12 as=0.5e-12
+ nolimiting
+ data=channel
+ points=1200
+ grid=1000
+ vbs=0.000e+00

<table>
<thead>
<tr>
<th>Vgs</th>
<th>Vds</th>
<th>Ids</th>
<th>Cgs</th>
<th>Cgd</th>
<th>Cgb</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.000e+00</td>
<td>0.000e+00</td>
<td>0.000e+00</td>
<td>2.003e-16</td>
<td>2.003e-16</td>
<td>2.783e-16</td>
</tr>
<tr>
<td>0.000e+00</td>
<td>1.000e-01</td>
<td>1.821e-12</td>
<td>2.003e-16</td>
<td>2.003e-16</td>
<td>2.749e-16</td>
</tr>
<tr>
<td>0.000e+00</td>
<td>2.000e-01</td>
<td>2.003e-12</td>
<td>2.003e-16</td>
<td>2.003e-16</td>
<td>2.744e-16</td>
</tr>
<tr>
<td>0.000e+00</td>
<td>3.000e-01</td>
<td>2.204e-12</td>
<td>2.003e-16</td>
<td>2.003e-16</td>
<td>2.720e-16</td>
</tr>
<tr>
<td>0.000e+00</td>
<td>4.000e-01</td>
<td>2.400e-12</td>
<td>2.003e-16</td>
<td>2.003e-16</td>
<td>2.706e-16</td>
</tr>
<tr>
<td>0.000e+00</td>
<td>5.000e-01</td>
<td>2.704e-12</td>
<td>2.003e-16</td>
<td>2.003e-16</td>
<td>2.681e-16</td>
</tr>
<tr>
<td>0.000e+00</td>
<td>6.000e-01</td>
<td>2.973e-12</td>
<td>2.003e-16</td>
<td>2.003e-16</td>
<td>2.677e-16</td>
</tr>
</tbody>
</table>
```

3. SPICE 3 Level=3 MOS minimum parameters

```
.model NENH nmos level = 3 tox = 1.11102e-08 phi = 0.6
+ vt0 = 0.631419 kp = 1.31264e+09 theta = 8.18536e+12
+ vmax = 196589 u0 = 4.22341e+15
+ js = 2.0364e-06
```

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