Multi-buffer SSN Simulation using BIRD95

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• Implementation Steps
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Review of the key points in BIRD95.5

• Added [Composite Current] keyword to represent the total current flow through buffer VDDQ node

• Used Series Model Type keywords for On-die parasitic associated with VDDQ (possibly ICM model can be used in the future)

• Gate Modulation will be address by BIRD97

• X-bar current could possibly be addressed by another BIRD
BIRD95 Implementation Schematics

Case 1: B-element only
Case 2: B + IvsT*
Case 3: B+IvsT*+Z_VDDQ

Note: IvsT* is different with IvsT table in BIRD95, but it is derived from IvsT table.
Definition of IvsT and Z_VDDQ

- IvsT is the total current from the VDDQ which is connected to ideal DC voltage source
- Six IvsT tables (3 different I/O loadings associated with rising/falling edges) are not required, but recommended
- Z_VDDQ is the frequency-dependent impedance derived with the correct DC voltage applied at VDDQ pin and open-load condition
- Z_VDDQ information is proposed to be provided through ICM model
IvsT* and parasitic components

- IvsT*=IvsT (BIRD95 table)-IvsT**
- IvsT** is the total current from the VDDQ by using existing IBIS model with Z_VDDQ connected in parallel.
- All currents here are under ideal power supply and standard loading conditions.
- Two sets of IvsT* associated with rising and falling edge were derived by averaging different loading conditions in our examples. More complicated model could be derived from 6 IvsT* tables to compensate the load variation effects.
- ESR, ESL, C and R_dc can be extracted from Z_VDDQ to match the impedance in frequency domain.
- The ESR, ESL, C and R_dc is just one example of the possible circuits to match Z_VDDQ. It could cover majority I/O buffers’ on-die parasitic components.
Multi-buffer SSN Simulation

- An impedance-controlled 1.8V HSTL output buffer is used as an example
- IBIS model is extracted from HSPICE transistor model
- HSPICE B-element is used to simulate the IBIS model
- \textit{BIRD95} IvsT info is implemented with ideal current source in parallel with B-element
- 4 identical buffers are used to simulate the SSN noise
- 5 different switching modes are studied
- Non-standard load (6” 50Ohm transmission line with 5pF and 50Ohm resistor to VDDQ/2 at receiver) is used in simulations.
Simulation schematics

VDDQ & I_vddq

0.1Ohm
1nH

VDDQ

in3
B3

in2
B2

in1
B1

in0
B0

6” 50-Ohm T-line

Vpad

Vrcv

50Ohm

5pF

VDDQ/2

<table>
<thead>
<tr>
<th>Input date pattern</th>
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<tbody>
<tr>
<td>in3210</td>
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<tr>
<td>HHHH</td>
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<tr>
<td>HHHL</td>
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<tr>
<td>HHLL</td>
</tr>
<tr>
<td>HLLL</td>
</tr>
<tr>
<td>LLLL</td>
</tr>
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</table>
Case with input pattern of HHHH
Case with input pattern of HHHL
Case with input pattern of HHLL

VDDQ

Vpad

I_VDDQ

Vrcv

HSPICE
IBIS only
IBIS+BIRD95

HSPICE
IBIS only
IBIS+BIRD95

Presentation_ID
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Case with input pattern of HLLL

VDDQ

Vpad

I_VDDQ

Vrcv

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Case with input pattern of LLLL
Conclusions

- Multi-buffer SSN simulation can be handled by using BIRD95
- With BIRD95, the IBIS model matches the HSPICE model very well for all simulated cases
- No-ideal load can be handled well by BIRD95
Back up Slides

• \textit{IvsT, IvsT}^* \text{ and IvsT}^{**}
• What’s impact of external load on IvsT, IvsT^* \text{ and IvsT}^{**}
Transistor Spice Model Rising

- Pull-up Rising
- Pull-down Rising
- Open Rising

Transistor Spice Model Falling

- Pull-up Falling
- Pull-down Falling
- Open Falling
IvsT**

IBIS Model Rising

- Pull-up Rising
- Pull-down Rising
- Open Rising

IBIS Model Falling

- Pull-up Falling
- Pull-down Falling
- Open Falling
\[ l_{vsT^*} = l_{vsT} - l_{vsT^{**}} \]
Impact of external load on \( \text{lvsT, lvsT}^{*} \) and \( \text{lvsT}^{**} \)

- Under ideal power supply condition, the external load has impact on \( \text{lvsT, lvsT}^{*} \) and \( \text{lvsT}^{**} \).

- Since \( \text{lvsT}^{*} \) is the difference between \( \text{lvsT and lvsT}^{**} \), \text{BIRD95} can compensate missed current components in existing IBIS simulators. (\( \text{lvsT}^{*} \) and \( \text{lvsT}^{**} \) can be different among different EDA tools)

- Under nonideal power supply condition, \( \text{lvsT}^{*} \) can be adjust accordingly to model the first-order effects. (\( \text{RvsT, ZvsT, CvsT and similar proposal as BIRD98 can be used} \)

- Inaccurate loading dependent xbar current is the major reason behind the different \( \text{lvsT}^{*} \) under different load condition. This issue can be solved by future BIRD. The new BIRD and \text{BIRD95} will not conflict since the new bird will only improve the accuracy in \( \text{lvsT}^{**} \).
Questions and Answers