Next Generation I/O
Macromodeling

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Towards the Next Generation

- Proposal at National Science Foundation asking for support into investigation of new approaches to IBIS modeling and (some) support of infrastructure
  - Requesting support for one PhD student for three years
  - Industry involvement proposed (guidance and feedback)
  - NSF success rate < 10%
  - ~October start date if supported
  - Thanks for letters, though more would have been useful
  - Will modify and submit again next year if unsuccessful
Elements of Proposal

Background
- Use of IBIS will diminish without influx of new technology
- Accuracy and availability issues forcing designers back to encrypted Spice models

Proposed Activities
- Develop templates for macromodels that improve accuracy and utility
  - Initially in Verilog-AMS and/or VHDL-AMS
  - Later determine approach to implementation of a “B-model” like element in a Spice-like simulator
- Distribute templates and knowledge about “B-model” like element implementation
- Develop tools to support automated or semi-automatic conversion
Accuracy Issues

Black Box Correction Factors

– Inspired by BIRD95 and BIRD97
Implementation Issues

• **Verilog –AMS and VHDL – AMS**
  – Preliminary results of two-tap pre-emphasis driver implemented in AMS

• **Binary (Spice-like) simulator issues and elements**
  – KCL enforcement does not work for small currents. Instead match voltage and currents.
  – Quasi-Newton iteration to improve convergence
Concluding Remarks

Questionnaire