Case Study of Scheduled Single-Ended Driver Featuring [Test Data]

Michael Mirmak
with Priya Vartak and Ted Ballou
Intel Corporation
Chair, EIA IBIS Open Forum
michael.mirmak@intel.com

IBIS Summit at DAC 2008
Anaheim, California
June 10, 2008
Legal Disclaimer

THIS DOCUMENT AND RELATED MATERIALS AND INFORMATION ARE PROVIDED "AS IS" WITH NO WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS, OR ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATION, OR SAMPLE. INTEL ASSUMES NO RESPONSIBILITY FOR ANY ERRORS CONTAINED IN THIS DOCUMENT AND HAS NO LIABILITIES OR OBLIGATIONS FOR ANY DAMAGES ARISING FROM OR IN CONNECTION WITH THE USE OF THIS DOCUMENT.

Performance tests and ratings are measured using specific computer systems and/or components and reflect the approximate performance as measured by those tests. Any difference in system hardware or software design or configuration may affect actual performance.

Intel may make changes to specifications, product descriptions, dates and plans at any time, without notice.

Copyright © 2008, Intel Corporation. All rights reserved.

*Other names and brands may be claimed as the property of others
An Additional Disclaimer

• The following information is presented as the opinion of one person at Intel. This presentation does not necessarily represent Intel policy, commitments or preferences.

• This is not presented on behalf of the IBIS Open Forum and does not represent the official IBIS Open Forum direction.
Agenda

• Introducing an Unusual Design
  – “Buffer X” on “Interface X”
• Describing the Design with IBIS
  – [Driver Schedule]
• Hurdles to Cross-tool Operation
  – [Driver Schedule] Implementation
• Applying [Test Data] to Aid Correlation
• Tool Correlation
• Comments and Recommendations
• Q & A

*Other names and brands may be claimed as the property of others
An Unusual Design

“Buffer X” for “Interface X”

• A real interface, in use on real systems

• Many familiar aspects, making IBIS a good modeling approach
  – Interface is single-ended and multi-drop
  – Buffers are complementary (pullup/pulldown) or open-source
  – Edge rates in (low) nanoseconds, with MHz switching rates

• But... several bizarre features confound simple model-making
  – Device contention: multiple components drive simultaneously
  – Logic is both time-and voltage-based
    • “1” and “0” defined by percent duty cycle at high or low voltages
  – At least one device uses staged buffer turn-on/turn-off
Example of Timings and Logic

Device B has staged turn-on/turn-off in this case study.
Describing Buffer X with Traditional IBIS

- Contention poses no issue for IBIS per-se
  - Buffer description does not “care” about other buffer states
  - Most tools support multiple-driver topologies

- Unusual logic is a minor hurdle
  - Device A duty cycle for logic “1” or “0” is 25% high V / 75% low V
  - Device B is in high-impedance (high-Z) state for logic “0”
  - Device B duty cycle for logic “1” is ~ 75% high V / 25% high-Z
  - Contention (and buffer impedances) creates final interface states
  - Can handle logic at tool level, without special IBIS considerations

- Describing Device B requires only a few IBIS features
  - Open-source, using traditional I-V and V-t tables, plus C_comp
  - Buffer uses stages of different impedances
  - Stages are driven by a fixed internal clock, unrelated to interface switching speed

*Other names and brands may be claimed as the property of others
[Driver Schedule] Refresher (IBIS Cookbook)

- [Driver Schedule] describes buffer behavior using individual [Model]s controlled by timings given relative to the input stimulus.

“Some applications require that a buffer change its strength or transition speed characteristics at fixed times after input stimulus changes.”

<table>
<thead>
<tr>
<th>Model Name</th>
<th>Rise_on_dly</th>
<th>Rise_off_dly</th>
<th>Fall_on_dly</th>
<th>Fall_off_dly</th>
</tr>
</thead>
<tbody>
<tr>
<td>P0 stage</td>
<td>0.0000ns</td>
<td>5.0000ns</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>N0 stage</td>
<td>0.0000ns</td>
<td>NA</td>
<td>0.0000ns</td>
<td>NA</td>
</tr>
<tr>
<td>N1 stage</td>
<td>0.3006ns</td>
<td>NA</td>
<td>0.0549ns</td>
<td>NA</td>
</tr>
<tr>
<td>N2 stage</td>
<td>0.5481ns</td>
<td>NA</td>
<td>0.1163ns</td>
<td>NA</td>
</tr>
</tbody>
</table>

P0 on for 5 ns at/after rising input edge.

N0, N1 and N2 staggered after any input edge.

Inverter [Driver Schedule]
Rise_on_dly = NA
Rise_off_dly = 0 ns
Fall_on_dly = NA
Fall_off_dly = 0 ns

*Other names and brands may be claimed as the property of others*
Specific Implementation

- Device B IBIS Implementation
  - Five “legs” or stages, [Pullup] only
  - First stage turns on immediately
  - Following stages turn on at regular periods
  - Only Rise_on_dly and Fall_on_dly used
  - Stage impedances range from ~1500 ohms to ~100 ohms
  - “Top-level” buffer [Model] is a duplicate of leg 1, plus clamp data

*Other names and brands may be claimed as the property of others*
Hurdles to Cross-Tool Operation

• [Driver Schedule] has not been consistently supported in the past
  – Behavior under different tools varied widely (and may still)
  – BIRD88.3 written to ensure better signal initialization of [Driver Schedule]

• To build confidence, we need a way to verify tool output vs. transistor-level design performance and intent
  – Traditional IBIS models are created from transistor-level data
  – Correlation using same conditions produces the same IBIS I-V, V-t data
  – [Driver Schedule] combines several buffers, making correlation of tool interpretation of IBIS data critical

IBIS has such a feature: [Test Data], in Version 4.0
[Test Data] and [Test Load]

- [Test Data]
  - Contains simple rising and/or falling V-t tables (typical, minimum and maximum)
  - Supports single-ended and differential buffers
  - Links to a particular model by [Model] name
  - Links to a particular load by [Test Load] name
  - Not actually for use in simulations of the associated buffer – correlation only!

- [Test Load]
  - Describes the loading used for the [Test Data] waveform
  - Supports parallel and serial elements, plus at-driver and receiver measurement points

- Procedure for “Buffer X” Device B and [Test Data]/[Test Load]
  - Simply imported the transistor V-t data for a resistive at-pad load from a spreadsheet
    - 1 Rising Waveform and 1 Falling Waveform, “Near End”, single-ended
  - Specified [Test Load] as 330 ohms, 0 V, “Near End”
Testing “Buffer X”

“Buffer X” with Resistive Load

Tool A: External EDA SI Tool & IBIS [D. Schedule]

Tool B: External EDA SI Tool & IBIS [D. Schedule]

Raw Transistor-Level Waveform ([Test Data])

How do the tools “measure up?”
Correlation Overlays – Falling Edge

- Min corner, 330 ohm load to ground at pad

*Other names and brands may be claimed as the property of others
Correlation Overlays – Falling Edge Zoom

- Zoom reveals potential value of [Test Data]

![Graph showing falling edge overlay of Transistor, Tool A, and Tool B with annotations indicating shape features captured, due to manual time-shift, and test data would reveal this.](graph.png)
Correlation Overlays – Rising Edge

• Min corner, 330 ohm load to ground at pad

*Other names and brands may be claimed as the property of others
Correlation Overlays – Rising Edge Zoom

- Zoom reveals potential value of [Test Data]
Correlation Overlays – Rising Edge Zoom (2)

• Again, zoom reveals potential value of [Test Data]
Findings from [Driver Schedule] and [Test Data]

• First, the bad news...
  – Neither of the tools tested supported [Test Data]/[Test Load]
  – The keywords did not cause errors per se, but were simply ignored
  – Therefore, no automated means was available for comparing tool output to [Test Data] information

• Now the good news...
  – Manual comparison of tool to transistor-level data showed good correlation
  – Tools are therefore processing [Driver Schedule] (in this case) correctly
  – Comparisons using [Test Data] transistor-level waveforms vs. tool outputs can reveal tool usage and user setup issues
  – User must decide which differences are relevant to design targets

[Test Data] has value in correlation, particularly if comparisons could be automated

Extracting [Test Data] places no significant burden on design/simulation engineer

*Other names and brands may be claimed as the property of others
Comments

• [Test Data] can add value!
  – For tool vs. transistor or lab correlation, [Test Data] is a clear advantage
  – The keyword is very easy to implement, for simple loads

• Creating [Driver Schedule] models poses problems for model makers
  – Syntax is difficult to understand, even with examples
  – Data almost impossible to gather without:
    • Applying math to extracted tables
      – Buffer ends cycle with apparent impedance of leg 1 || leg 2 || leg 3...
      – We want each leg in its own [Model] section
      – Design may not enable single-leg transient V-t extraction
    • “Cutting” the schematic into pieces
    • Relying on design test modes (not always available)

• Annoyance: Vref, Cref, Rref, Vmeas required for individual leg [Model]s
  – Clearly Vref, etc. are only really are needed at the top-level
  – Individual legs may not even pass through Vmeas level
Recommendations

- **[Test Load]**
  - Support loss descriptions for transmission lines
  - Clarify whether load is at-pad or at-pin (intent seems to be at-pad)

- **[Test Data]**
  - Permit custom, defined data patterns (e.g., PRBS)
  - Clarify support of series devices
  - Clarify distinction between simulated and lab-captured data
  - Add Cookbook entries for both [Test Data] and [Test Load]

- **[Driver Schedule]**
  - Remove requirement for Vmeas, etc. in scheduled models (below top-level)
  - Add additional examples to Cookbook and specification
  - Permit “Combination [Model]” or additive model data, rather than require data for isolated legs individually
    - *Pushes math manipulation of driver data to tool rather than to maker*
    - *Would probably drive tool-to-tool divergence of results*

Thanks to the IBIS Quality Task Group for several of the suggestions above and their continuing [Test Data] analysis!
*Other names and brands may be claimed as the property of others