Multi-lingual Model Support within IBIS Update

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Benefits of Multi-lingual Support

- **Model advances beyond IBIS**
  - True differential buffers, current buffers
  - SCSI driver/terminator advances
  - More detailed over-clocked buffer detail
  - SSO effects and gate modulation
  - Code based modeling

- **Die interconnect advances**
  - Die interconnect and complex package modeling
  - External voltage rail, power integrity interactions
  - External buffer strength control

- **Closer digital and analog analysis (AMS)**
Complex Application within IBIS
Die (left) & Component (total)
Models, Die Circuit, Package Model
Diff., Single-ended, Controlled Buffers
Coupled Pins & Rails, Split Package
Why/How Multi-Lingual Modeling?

- Leverages existing IBIS, Spice, VHDL-AMS, Verilog-AMS
  - Still use IBIS where appropriate
  - Extension uses IBIS for Pinout, Pkg., Info. & Spec.
  - Executes external code files
- Multi-lingual EDA tools from many companies
  - Mentor, Cadence, Avanti, …
- Faster response to industry - IBIS & few keywords
  - [External Model]: Buffer level external models
  - [External Circuit]: Die circuitry
  - [Node Declarations], [Circuit Call]: Interconnects
Digital (logic) and Analog Ports and Reference Models for I/O Buffers

Reference Voltages:
A_puref, A_pcref, A_pdref, A_gcref, A_gnd
Existing IBIS or [External Model]s

- [External Model] under [Model] <model_name>

- [External Model]
  - Language <selection>
  - Corner <typ,min,max files and model names>
  - Ports <analog and digital port list>
  - D_to_A <digital signals to Spice ramps>
  - A_to_D <Spice thresholds to digital signals>

- Internal or external reference supplies
- Direct connection or interconnection syntax
Controlled Model & [External Circuit]

- [External Circuit] <circuit_name>
  - Language <selection>
  - Corner <typ, min, max files, names>
  - Ports <port list>

- [External Model] and [External Circuit] connected using internal and die nodes:

- [Node Declarations]
  - <internal node list>

- [Circuit Call] <model or circuit name>
  - Port_map <port to node mapping>
Advantages

- Fits in
  - Use IBIS completely or at least for pins, package, specification and information content
- Structural models
  - Berkeley Spice support, BSIM4, etc.
  - Simple RLC, diodes, interconnects, etc.
- Behavioral models for extended features
- IP protected models?
  - VHDL-AMS, etc. for behavioral modeling
  - Common standardized encryption possible for all text-based files
Issues

- Multi-lingual complication?
  - Already being done

- Support too many languages?
  - IBIS Committee should limit set to open, public, accepted formats (Berkeley Spice, VHDL-AMS, etc.)

- Model support to enable industry?
  - Cheap/free tools: Berkeley Spice, “student” Spices
  - http://www.vhdl-ams.com/ : SEAMS, spice2ams, JAVA VHDL-AMS front end, Analyzer, samples, etc.
What’s Next?

- Multi-lingual extensions - major additions above and more!
- BIRD7X to describe details are now being processed