Mπlog, Macromodeling via Parametric Identification of Logic Gates

F.G. Canavero, I.A. Maio, I.S. Stievano

Politecnico di Torino, Italy

igor.stievano@polito.it

http://www.eln.polito.it/research/emc
EMC Group @ POLITO

Staff

3 Prof.
4 PhD
2 Ass. Res.

Research

Modeling of devices, interconnects and discontinuities in high-speed information and communication systems.

Collaborations:

- IBM (USA+GE)
- INTEL (USA)
- CST (GE)
High Performance simulation requirements

- Very accurate timing
- Power-supply voltage variation effects
- Temperature effects

- Transistor-level models are not affordable (computation + structure disclosure)
- *Classic* IBIS models not always adequate

→ Complementary Approach
**Macromodeling via Parametric Identification (π) of Logic Gates**

**What is it?**

A *mathematical expression* reproducing the electrical behavior of the device

\[ i = F(v, \frac{d}{dt}) \]

Nonlinear dynamic relationship
**Mπlog (ii)**

How does it work?

- Real Device (or its physical model) is conveniently **stimulated**
- **Reaction** (port transient responses) is used to build the model
$\textbf{Mπlog: what is the output?}$

**Model structure:** $F$ is a $\sum$ nonlinear Gaussian Radial Basis Functions (RBF)

\[ i = -a_1 \exp\left\{ -\frac{v^2}{a_2} \right\} + a_3 \exp\left\{ -(\frac{dv}{dt})^2 \right\} \]

unknown parameters: amplitude, position, spreading
\[ i = -a_1 \exp\left\{ -v^2/a_2 \right\} + a_3 \exp\left\{ -(dv/dt)^2 \right\} \]

(a) DIRECT EQUATION DESCRIPTION/IMPLEMENTATION

(b) CIRCUIT INTERPRETATION & SPICE IMPLEMENTATION

(Compatible with IBIS MULTI-LINGUAL Model Support, BIRD #75.8)
**Mπlog applications**

- **Basic macromodels** of Input and Output ports
  
  
  - Inclusion of slowly-varying **device parameters** (eg, **temperature**)
  - Inclusion of the **power-supply voltage** variation
  - models of the **power supply port**
  - models of **tristate drivers**


Following examples are based on a high-speed IBM CMOS transceiver ($V_{dd} = 1.8$ V)
Example #1: basic devices

High-speed interconnection system with (Z-Series) IBM I/O ports

Setup

Models

- Reference (transistor-level)
- Macromodels ($M\pi log$)

**CPU TIME (PowerSPICE)**

<table>
<thead>
<tr>
<th>Model</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistor-level</td>
<td>6 min</td>
</tr>
<tr>
<td>$M\pi log$ model</td>
<td>5 s</td>
</tr>
</tbody>
</table>
Example #2: temperature effects

- Test Case

$$T_{\text{MIN}} = 10 ^\circ C, \ T_{\text{TYP}} = 40 ^\circ C, \ T_{\text{MAX}} = 80 ^\circ C$$

-10, 25, 60, 100 °C

- accuracy confirmed for realistic loads and a wide range of $T$ values
Integration of signal and power supply port behavior

\[ i = F(\Theta, v, v_{dd}) \]
\[ i_{dd} = F_{dd}(\Theta, v, v_{dd}) \]

Macromodels obtained for \( v_{dd} \) values within the range \( V_{dd} \pm 15 \% \)
Example #3: SSN analysis

20 x \[ \bigotimes \]

\[ \begin{align*}
&i_{dd} \\
&v \\
&v_{dd}
\end{align*} \]

\[ \begin{align*}
&50 \, \Omega, \, 0.5 \, \text{ns} \\
&1 \, \text{pF} \\
&1 \, \text{m} \Omega, \, 0.1 \, \text{nH}
\end{align*} \]

\[ \begin{align*}
&v_{dd} \\
&i_{dd}
\end{align*} \]

\[ \begin{align*}
&20 \, \text{mA} \\
&600 \, \text{mA}
\end{align*} \]

\[ \begin{align*}
&2 \, \text{V} \\
&1.5 \, \text{V} \\
&2 \, \text{V} \\
&1.5 \, \text{V}
\end{align*} \]

\[ \begin{align*}
&t \, \text{ns} \\
&t \, \text{ns}
\end{align*} \]
Example #4: tristate driver

• Test Case

ENABLE [0001100110010000]

INPUT [0011110011000000]

\[(50 \, \Omega, 0.4\text{ns})\]

1k\(\Omega\) // 1pF

\[v(t)\]
Conclusions

\textbf{Mπlog approach}

- Macromodels for I/O Buffers and Power Supply Ports of Digital ICs

- Advantages
  - PROTECTION OF IP
  - HIGH ACCURACY (timing errors $\sim 10$ ps @ 400 MHz)
  - LOW COMPLEXITY (a few Gaussian functions)
  - HIGH EFFICIENCY ($20\div100$ time faster than transistor-level models)

IBIS Compatibility via Multi-lingual description