IBIS QUALITY COMMITTEE UPDATE/ PRACTICAL USE OF IQ CHECKLIST

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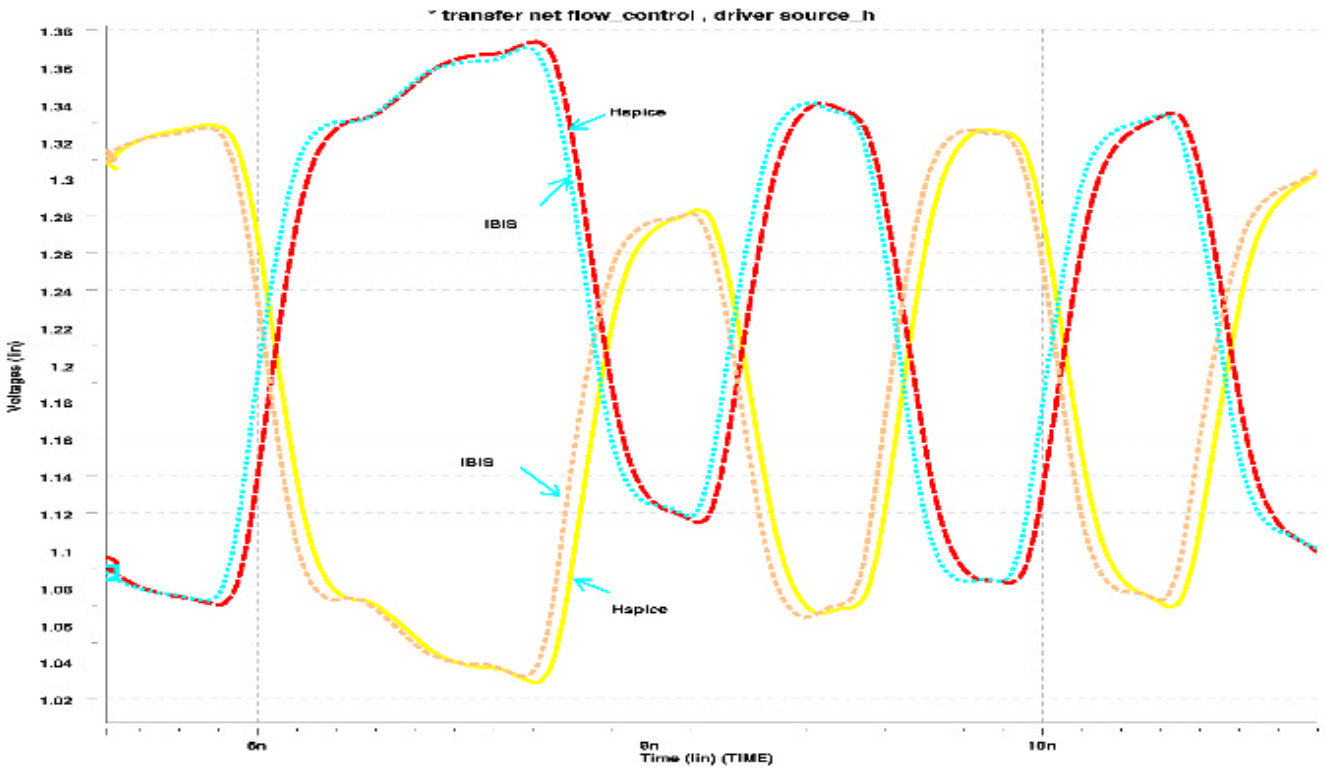
IBIS Models Can Be Awesome !

Accurate LVDS IBIS Model @ 1.25GHz



SPI4 interface: 1.25GHz, target pad, VDDQ=2.375

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But Generally IBIS Model Quality is Poor

ibis_qual.pdf

File Edit Document View Window Help

SiQual[SM] Inc.
A Critique of IBIS Models Available For Download On the Web – Part I

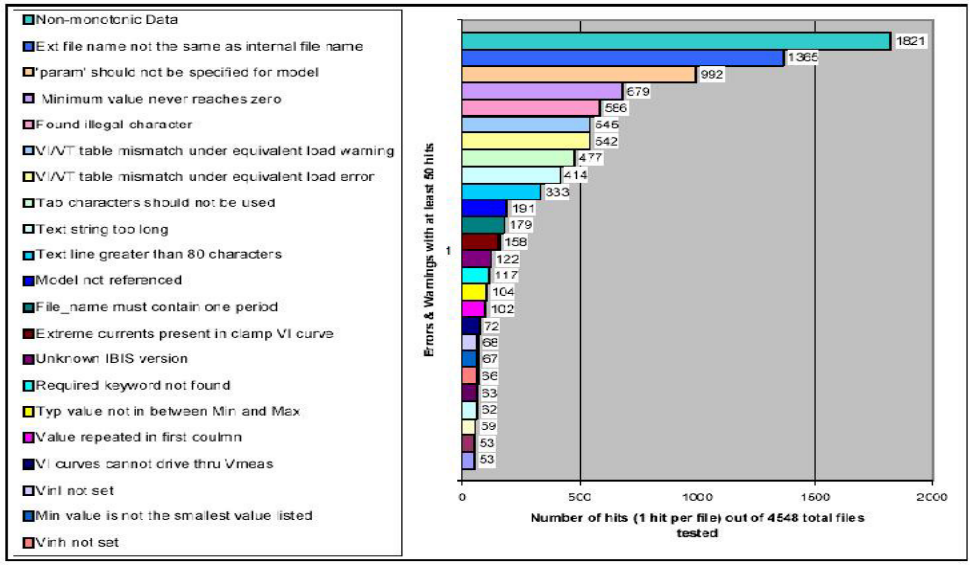

Figure 3-1: Total Number of Hits of the Errors or Warnings Reported by IBISCHK3

3.2 Analysis of Errors and Warnings By Category

8 of 24 8.5 x 11 in

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IBIS Quality Subcommittee

- Formed 3/02
- Charter
  - Develop a complete checklist
  - Establish levels of quality
  - This checklist should serve to be incorporated directly into procurement specs.
  - Suggest enhancements to IBISCHK
- Goals
  - Rating system that is easy to understand and adopt
  - Communicate to vendors/users.
  - Cover overall file, component, and model sections
  - Check for completeness, correctness, accuracy
  - Leverage of prior work

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IBIS Quality Subcommittee Active participants

- Committee is represented by semiconductor vendors, EDA vendors, and IBIS end-users.

SiSoft - Barry Katz (Chairman), Robert Haller, Eric Brock, Kevin Fisher
Siemens – Eckhard Lenski, Katja Koller
IBM – Greg Edlund
Cadence – Lynne Green
Apple – John Figueroa, Kim Helliwell
Mentor – Bob Ross, Hazem Hegazy, Sherif Hammad,
Cisco – Mike LaBonte, Todd Westerhoff
EMC – Brian Arsenault
Hitachi ULSI Systems – Shoji Kazuyoshi, Nonoyama Sadahiro
Leventhal Design & Communications – Roy Leventhal
Intel – Benjamin Silva
Teraspeed - Tom Dagostino
AMCC - Peter LaFlamme
Fairchild – Adam Tambone

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IBIS Quality Subcommittee

- Meets every 2 weeks (Tuesdays 9:00 EDT)
- Mailing list
  - Ibis-quality@freelists.org
  - http://www.freelists.org/archives/ibis-quality
- Important Web Sites
  - http://www.sisoft.com/ibis-quality
  - http://www.sisoft.com/ibis-quality/minutes
  - http://www.sisoft.com/ibis-quality/docs
  - http://www.vhdl.org/pub/ibis/bugs/ibischk
- Reviewing and updating documentation

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IBIS Quality Example Agenda

- Roll call
- Review of previous meeting minutes
- Announcements
  - EIA Call for patent disclosure
  - Upcoming conferences
- Action item (AR) review
- Open for new items
- Detailed documentation review
  - IQ_Quality_Summary
  - IQ_General_Header.txt
- Plans and schedule for next meeting

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Status Update

- Compiled and published IBIS Quality checklist
  - http://www.sisoft.com/ibis-quality/
- Defined quality levels
  - Level 0 – Passes IBISCHK
  - Level 1 – Complete and correct
  - Level 2a, 2b – Correlation: Simulation, Measurement
    - Leverage off of IBIS Accuracy Handbook (spec)
  - Level 3 – All of the above
- Submitted multiple IBISCHK enhancements
- Submitted IBIS Golden Parser open source proposal
- Created, indexed first pass of documentation
- Presently working through documentation

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IQ_Quality_Summary Example Documentation

- The IBIS Quality Summary comments must begin with the string '|IQ' (that is, the comment character followed by "IQ" for IBIS Quality).
  - ✓ …
  - ✓ IBISCHK must yield 0 Errors
  - ✓ IBISCHK warnings must be explained if they cannot be elimininated.
  - ✓ Vil/Vih must be defined on receivers
  - ✓ Standard Load/Vmeas must be specified on drivers
  - ✓ Overshoots must be defined for drivers and receivers
  - ✓ Checks for correctness and completeness
    - ✓ All pins defined and validated for correct
    - ✓ …

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IQ Documentation Index

1.0 IQ Header Section	Kim Helliwell
Summarizes quality for File,	
2.0 General File Characteristics	Todd Westerhoff
Passes and Document version of IBISCHK	
Goal zero errors and zero warnings	
3.0 Component Section	Barry Katz
4.0 Model Section	
4.1 General	Lynne Green
4.2 Pullup/Pulldown/Clamp IV curves	Robert Haller
4.3 VT Curves -	Barry Katz
4.4 Ramp Data, Waveform processing	Mike LaBonte
5.0 Possible Errors that should be checked -	Eckard Lenski
6.0 Correlation	Greg Edlund
6.1 SPICE correlation	
6.2 Lab Correlation	
7.0 Model Limitations -	Barry Katz

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IQ Summary

- Accurate IBIS models are achievable
- IBIS Quality subcommittee is driving the industry for improved IBIS model quality !
- Accomplished a lot
  - Checklist
  - Levels
  - IBISchk3 bug submissions/proposals
  - 1st Pass documentation and index
- To Do
  - Complete documentation
  - Industry acceptance

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SISOFT Practical Use of IQ Checklist

- SISOFT practices what it preaches
- Automatic IBIS model Generation
- Compare SPICE to IBIS
- Obtain and insert Model and Model Spec
  - Document IBISCHK issues
  - Document source data
- Generate Accurate Pin list
- Independent Double checks
- Complete Model Documentation

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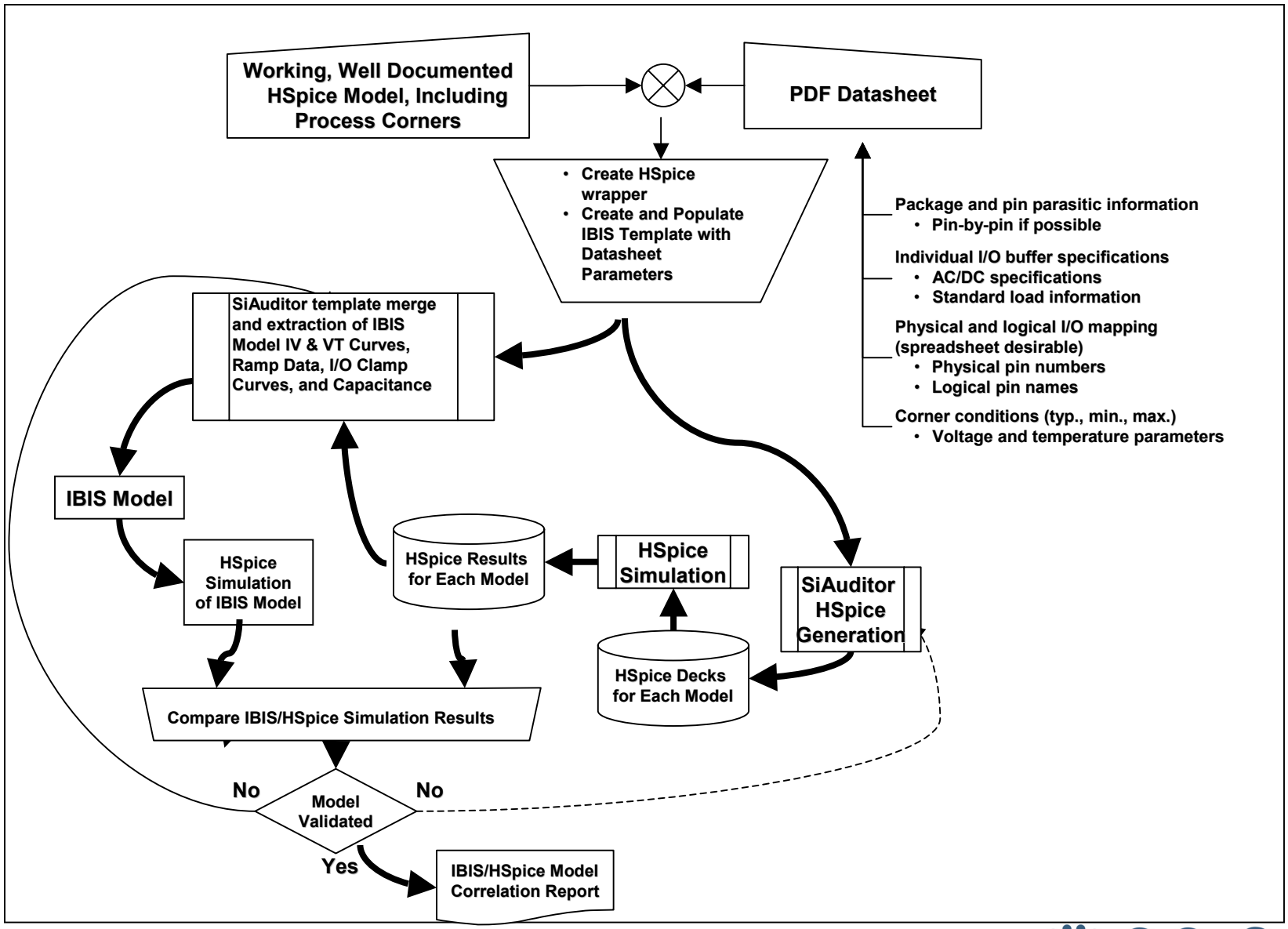
Utilize an Automatic process



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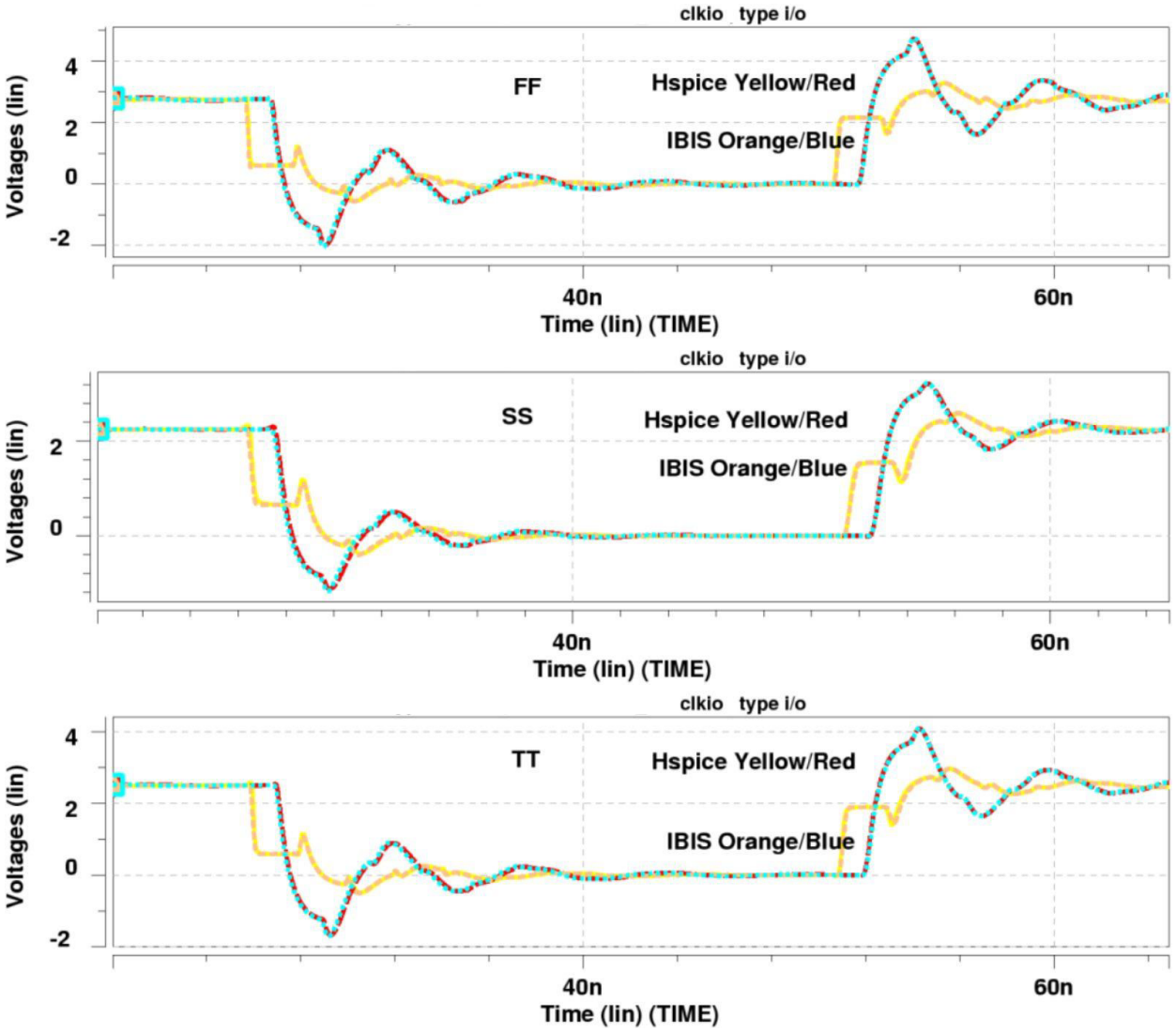
Compare SPICE to IBIS



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Example IBISCHK3 Issues Documented in .IBS File

- All I/O Models: When running through ibischk3, this file will contain 9 warnings about pullup and pulldown curves being non-monotonic. This is due to a bug in the ibischk parser. The IBIS Parser only looks at the pullup and pulldown, not at the combined curves, pullup and clamps or pulldown and clamps
- Running Latest verision of ibischk3 will yield 12 warnings
  - 9 pullup and pulldown Non-monotonic warnings (OK Parser Bug)
  - 1 C_comp min value is not the smallest value listed(OK by design)
  - 1 C_Comp max value is not the largest value listed(OK by design)
  - 1 Vmeas should not be specified for Model typ input(OK Parser Bug)
- Source data of IBIS Models
  - Pinlist data is from Spreadsheet dated 01/01/03 from XXX
  - SPICE MODELS dated 01/01/2003 from YYY
  - PDF specifications dated 11/28/2001 from YYY
  - Package Parameter are from SI report 11/15/02 from YYY

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Double Checks

- Cross check of consistency between library elements, such as:
  - IBIS models
  - Timing models
  - Net lists
- IBISCHK3
- IBIS Simulations Run
- Independent check of IV,VT Pin list Model Specs
- We call it – Validation
  - Automated checking with SiAuditor
  - Manual check by experienced engineers

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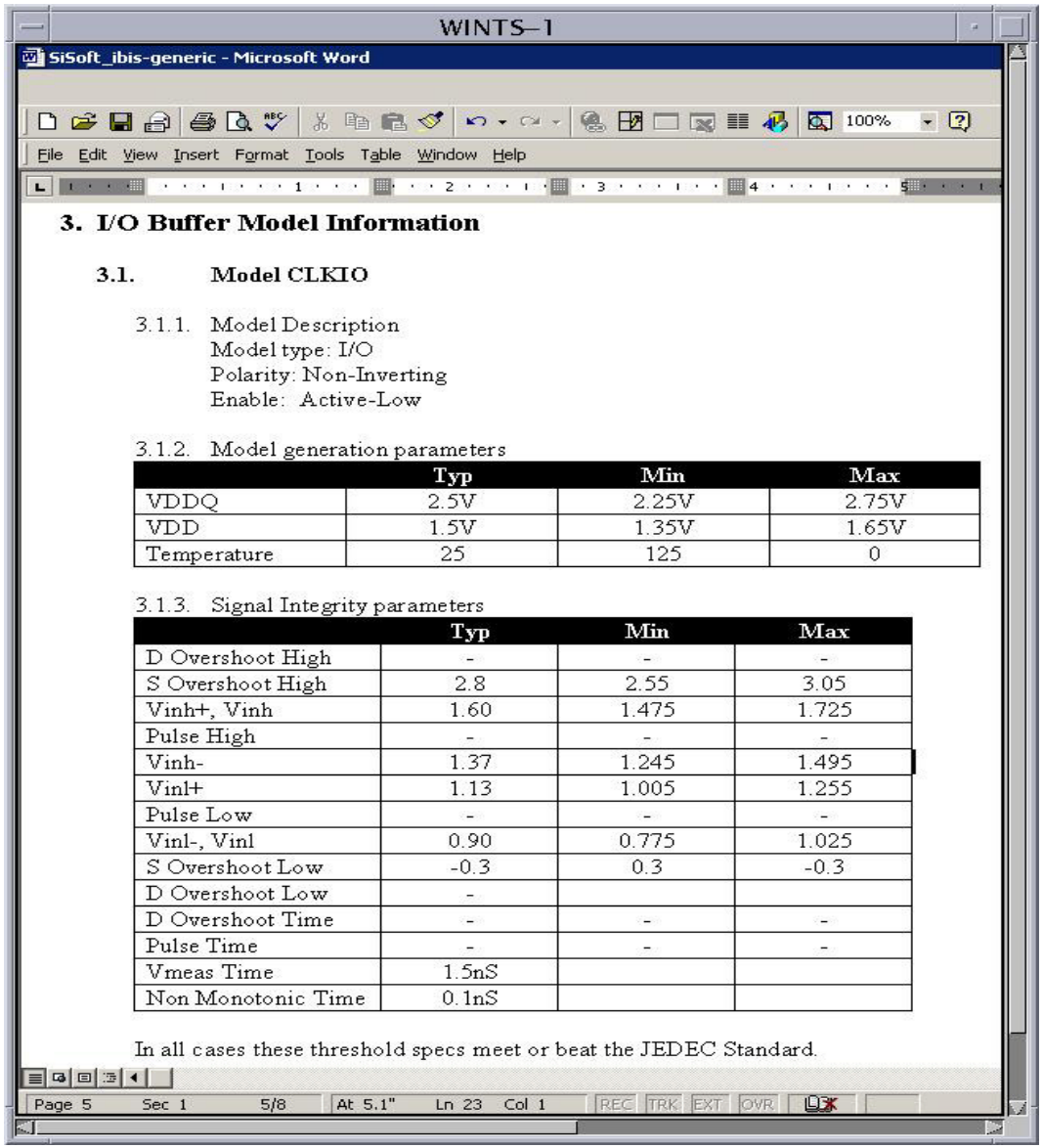
Document Results



3. I/O Buffer Model Information

3.1. Model CLKIO

3.1.1. Model Description
Model type: I/O
Polarity: Non-Inverting
Enable: Active-Low

3.1.2. Model generation parameters

	Typ	Min	Max
VDDQ	2.5V	2.25V	2.75V
VDD	1.5V	1.35V	1.65V
Temperature	25	125	0

3.1.3. Signal Integrity parameters

	Typ	Min	Max
D Overshoot High	-	-	-
S Overshoot High	2.8	2.55	3.05
Vinh+, Vinh	1.60	1.475	1.725
Pulse High	-	-	-
Vinh-	1.37	1.245	1.495
Vinl+	1.13	1.005	1.255
Pulse Low	-	-	-
Vinl-, Vinl	0.90	0.775	1.025
S Overshoot Low	-0.3	0.3	-0.3
D Overshoot Low	-		
D Overshoot Time	-	-	-
Pulse Time	-	-	-
Vmeas Time	1.5nS		
Non Monotonic Time	0.1nS		

In all cases these threshold specs meet or beat the JEDEC Standard.

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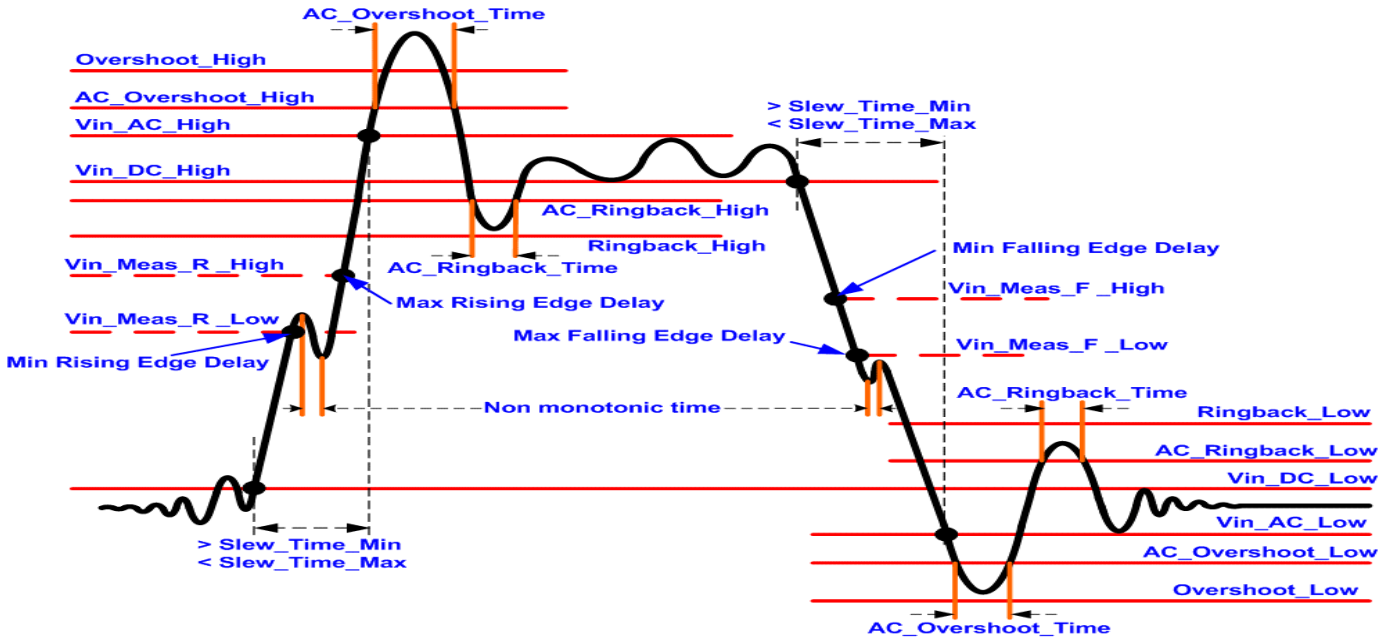

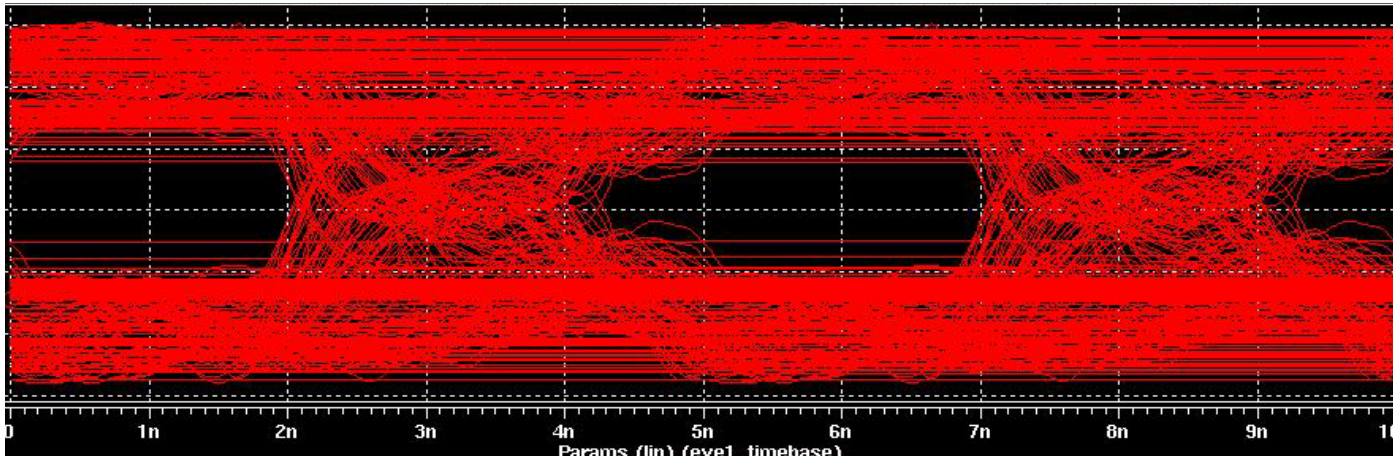

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