Modifying IBIS models
Overview

- Motivation
- Possible simulation types
- considered changes
  - $C_{\text{comp}}$
  - $U(i)$: driver strength, clamps
  - $U(t)$, ramp
  - Missing models
- Conclusion
Motivation

- Short time until simulation will start
- The quality of delivered models is more than ambiguous or
- No model available
- Consideration of available ibis parameter versus datasheet/technology/measurement/experience
- Need for a „worst case model“ but what does that mean?
Types of Simulation

- Signal Integrity
  - under/overshoots
- Timing: setup and hold time of clock net
- Crosstalk
- EMI
  - radiation
C_comp @ receiver

\[ C_{\text{comp}} + C_{\text{pkg}} = \text{Capacitance in Datasheet (min/typ/max)} \]

Normally: \( C_{\text{comp}}_{\text{IO}} > C_{\text{comp}}_{\text{input}} \)

Make \( C_{\text{comp}} \) smaller \( \Rightarrow \) ramp gets faster

\[ C_{\text{comp}} = 1\, \text{pF} / 5\, \text{pF} \]
Diodes @ receiver

flat  gnd-diode => large undershoot
steep  gnd-diode => small undershoot
No/wrong PVT-min-max curves -> scaling $U(I)$

$$I_{\text{max}} = I_{\text{typ}}(1+F)$$
$$I_{\text{min}} = I_{\text{typ}}(1-F)$$
$$F = F_p + F_v + F_T \text{ (independant variables)}$$

For example CMOS 3.3V:

- $F_{\text{process}} = 0.30 +/- 0.15$ (weak/strong 3σ)
- $F_{\text{temperature}} = 0.12 +/- 0.06$ (0,55,100°C)
- $F_{\text{vcc}} = 0.08 +/- 0.02$ (vcc+/- 5%)

would result in $F = 0.50 +/- 0.23$
No/wrong PVT-min-max curves -> scaling $U(t)$

$$\begin{align*}
  t_{\text{max}} &= (1+F)\cdot t_{\text{typ}} \\
  t_{\text{min}} &= (1+F)\cdot t_{\text{typ}} \\
  \text{Get } U_{\text{max/min}} \text{ out of intersection from } I_{\text{max/min}} \\
  F &= F_P + F_V + F_T \text{ (independant variables)}
\end{align*}$$

For example CMOS 3.3V:

- $F_{\text{process}} = 0.27 \pm 0.23$ (weak/strong $3\sigma$)
- $F_{\text{temperature}} = 0.15 \pm 0.09$ ($0,55,100\degree C$)
- $F_{\text{vcc}} = 0.03 \pm 0.02$ ($\text{vcc} \pm/\mp 5\%$)

would result in $F = 0.45 \pm 0.34$
Missing Model: e.g. 4mA Driver

- no 4mA-model from vendor
- We have:
  - 1) model from another vendor, other technology, 4mA
  - 2) model from the same vendor, other technology, 4mA
  - 3) model from the same vendor, similar technology, 4mA
- Copy one model from above
Missing model: e.g. Open_drain

- No OD-model from vendor
- We have:
  - 1) OD-model from another vendor, other technology
  - 2) OD-model from the same vendor, other technology
  - 3) OD-model from the same vendor, similar technology
  - 4) push-pull model available
- conversion of push-pull to open_drain
  - U(t): simulation from 3-state to low
  - U(I): skip pullup curve
Missing model: Open_drain

**Push-pull**

- Dynamic
  - Graph showing dynamic behavior

**Open_drain**

- Static
  - Graph showing static behavior
## Discussion of Changes

<table>
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<th>C_comp @ REC</th>
<th>Overshoot</th>
<th>t_setup</th>
<th>t_hold</th>
<th>Crosstalk</th>
<th>EMI</th>
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**Legend:**

- **+ = no errors**
- **- = errors**
- **o = not relevant**

**SIEMENS**

Katja Koller  Com SC SL TC23  11.03.2005
Summary and Conclusion

- Changing ibis does effect the simulation in a great manner
- Changes are in some simulation type more worst case and in an other more best case
- Every model „worst case“ ➔ NO system design
- More and faster cooperation from vendor is needed
- IF necessary, better adjustment of scaling parameters
Timing: Setup and Hold Time

**t\_setup**: the time, the data has to be stable high, until the clk starts rising (stable before the CK-edge)

**t\_hold**: the time away from the clk goes high, the data has to be stable high (stable after the CK-edge)

**t\_setup + t\_hold** is the minimal data pulse width