IBIS Models: the first step towards High Speed Design Kits

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A Little History ...
In the Beginning … 1980s

74xxx TTL

Standard I/O

Standard I/O

74xxx TTL

Standard I/O

74xxx TTL

Standard I/O

74xxx TTL
Then, speeds increased ...

1990

SPICE
• Slow
• Complex
• Encrypted

SPICE/Encrypted SPICE models

Standard I/O
Then IBIS came to the rescue …

1993

Standard I/O

IBIS Table Models

IBIS
• Fast
• Simple
• Standard

IBIS Table Models

IBIS Table Models

IBIS Table Models
Then came High Speed Serial I/O ... 2002

IBIS Table Models

Standard I/O

High Speed Serial

Standard I/O

IBIS Table Models

SPICE / Encrypted SPICE Models

SPICE
• Slow
• Complex
• Encrypted
IBIS 4.1 …

IBIS Table Models

IBIS Table Models

Standard I/O
High Speed Serial
Standard I/O

IBIS 4.1 Wrappers
SPICE Encrypted SPICE Models

Examples & Documentation
IBIS 4.1 with SPICE

- **IBIS**
  - Simple to use
  - Fast
  - Unencrypted
  - Standard

- **SPICE**
  - Complex
  - Slow
  - Encrypted
  - Proprietary

- **IBIS 4.1/SPICE**
  - Simple
  - Slow
  - Encrypted
  - Partially Proprietary
library IEEE;
use IEEE.electrical_systems.all;
use IEEE.std_logic_1164.all;

entity sgx_hssi_tx_icx_slow is
  generic (ui_real : real := 320.0e-12);
  port (terminal a_drive, a_signal_pos,
    a_signal_neg, pre_emphas2,
    pre_emphas1, pre_emphas0,
    drive_sel2, drive_sel1, drive_sel0,
    termsel1, termsel0 : electrical);
end entity sgx_hssi_tx_icx_slow;

--- Solves speed problem
--- Shields user from SPICE complexity
--- Double IP security
--- Industry Standard, Non Proprietary
IBIS 4.1 with IEEE 1076.1 AMS ...

IBIS Table Models

IBIS Table Models

Standard I/O

High Speed Serial

Standard I/O

IBIS 4.1 Wrappers

IEEE 1076.1 AMS Models

Examples & Documentation
IBIS 4.1 with IEEE 1076.1 AMS

- **IBIS**
  - Simple to use
  - Fast
  - Unencrypted
  - Standard

- **HSPICE**
  - Complex
  - Slow
  - Encrypted
  - Proprietary

- **IBIS 4.1/SPICE**
  - Simple
  - Slow
  - Encrypted
  - Proprietary

- **IBIS 4.1/IEEE1076.1**
  - Simple
  - Fast
  - Unencrypted
  - Standard
**IBIS 4.1 Standard**

**Traditional IBIS Model**

* S-parameter model
* RLC SPICE model,
* Transistor model,
* VHDL-AMS Model

.ends

**SPICE or Behavioral Model**

.component comp
  .subckt comp
  + inp inm outp outm
  *S-parameter model
  *RLC SPICE model,
  *Transistor model,
  *VHDL-AMS Model
.ends

**Multi-Lingual IBIS Wrapper**

**SI Analysis**

**SPICE Analysis**

**VHDL-AMS**

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**Pin**

1. dcp NC
2. dcm NC
3. bpn NC
4. bpp NC

**Diff Pin**

<table>
<thead>
<tr>
<th>1</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>3</td>
</tr>
</tbody>
</table>

**Series Pin Mapping**

2 3 R_1G_ohm

**Circuit Call**

component port_map inp 1
port_map inm 2
port_map outp 3
port_map outm 4
[end circuit call]

**External Circuit**

component language Spice
corner typ comp.sp comp
ports inp inm outp outm
[end external circuit]
What Next?

- Some more modeling enhancements
- High Speed Design Kits
Custom Menus

Kit Items

Circuit Description

IBIS Multi-Lingual Wrappers

SI Analysis

S-Param Models

Transistor Models

Behavioral Models

Eye Masks

RLGC Models

IBIS Table Models

SI Analysis Results
Routing Rules

- All signals within a given "QDR-II Match Group" should be matched length from the pin on the FPGA's (U110 and U148) to the pin on QDR Devices (U101, U102, U106, U108, U117). Maximum deviation is +/- 0.050 inches.
- Keep the distance from the pin on the QDR Device to the termination resistor pack (to VTT_QDRII) to less than 750 mils.
- Keep the distance from the pin on Stratix to the termination resistor pack (to VTT_QDRII) to less than 1250 mils.
- All signals must match lengths between pins (as in (1) above) within +/- 0.200 inches (address, control, data, clocks, etc…). Only nets within a match group must be matched tighter as in rule 1. Feedback clocks are exceptions to this rule – see rule 9.
- All signals are to maintain a spacing that is based on its parallelism with other nets. This is as follows:
  - 5 mils for parallel runs < 0.5 inches (~1X spacing relative to plane distance)
  - 10 mils for parallel runs between 0.5 and 1.0 inches (~2X spacing relative to plane distance)
  - 15 mils for parallel runs between 1.0 and 6.0 inches (~3X spacing relative to plane distance)
- All signals are to maintain 20 mil separation from other, non-related nets.
- All signals must have a total length of less than 4 inches.
- All signals in the Clock Group should be routed single-ended even though they may seem like differential clocks based on their naming conventions. As clock signals they must follow spacing rules as outlined in the CLOCKS section of this document.
Design Kits Development

IC/FPFA Vendors

Customers

EDA Vendors
Design Kits – Benefits to Customers

- Be up and running faster
- Have access to more than just Models, maximize efficiency and productivity
- Saves significant time
- Saves valuable resources
- Saves cost
Design Kits – Benefits to IC/FPGA Vendors

- Facilitates adoption of vendor silicon
- Better service to their customers
Design Kits – Benefits to EDA vendors

- Facilitates adoption of tools
- Maximize tool usage
- Better service to their customers
Should maybe be another place to drive High Speed Design Kits requirements and make proposal for a common format/content?