IBIS in Applications
- Modeling Complex IO with IBIS

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Outlines

• Device Models in EDA Tools
• New Challenges and New Studies
• An Applicable Solution - Macromodeling
• An Industrial Macromodeling Example
Outlines

• Device Models in EDA Tools
  – Transistor Level Models
  – Behavioral Models
  – How EDA tools use Behavioral Models
• New Challenges and New Data
• An Applicable Solution – Macromodeling
• An Industrial Macromodeling Example
Spice Transistor Level Models

- Very Complicated
- A lots of unusable stuff
- Too slow in the simulations

Behavioral Models
Behavioral Model

IBIS model

Block diagram of CMOS buffer

A basic IBIS model consists of:
- four I-V curves: pullup & POWER clamp, pulldown & GND clamp
- two ramps: dv/dt_rise, dv/dt_fall
- die capacitance: C_comp
- packaging: RLC values

for each buffer on a chip

IBIS Model Vendors

Top10 IBIS Model Vendors on Web
IBIS in EDA Tools

- Major EDA Simulators are supporting IBIS now
  - Cadence
  - Mentor
  - Synopsys
  - Zuken
  - Agilent
  - And many, many more ...

SPICE Simulators are taking IBIS now!!!

IBIS in EDA Tools

- Behavioral data in Spice simulators
  \[ I_{pad} = I_{pd}(V_{pad}-V_{gnd})W_{d}(t) + I_{cd}(V_{pad}-V_{gnd,c}) + I_{pu}(V_{pad}-V_{pwr})W_{u}(t) + I_{cu}(V_{pad}-V_{pwr,c}) \]

- Results are accurate
- Much, much faster simulation time
- IP Protected

HSpice Transistor Model vs. IBIS Model
Support Advance IBIS Features

- Driver Schedule
- Series / Series Switch (FET)
- Submodel (Dynamic Clamps, Bus Hold …)
- Differential Pair
- EBD (Board Models)
- ICM (Interconnect Models)
- More …..

IBIS Implementation
- Driver Schedule

<table>
<thead>
<tr>
<th>Model_name</th>
<th>Rise_on_dly</th>
<th>Rise_off_dly</th>
<th>Fall_on_dly</th>
<th>Fall_off_dly</th>
</tr>
</thead>
<tbody>
<tr>
<td>driver1</td>
<td>0.0ns</td>
<td>NA</td>
<td>0.0ns</td>
<td>NA</td>
</tr>
<tr>
<td>driver2</td>
<td>NA</td>
<td>0.666ns</td>
<td>NA</td>
<td>0.666ns</td>
</tr>
</tbody>
</table>

Inverter
Delay
IBIS Implementation - Differential Pair Driver

[Diff Pin]  inv_pin  vdiff  tdelay ......
1  2  0  1ns

[Series Pin Mapping]  pin_2  model_name ......
1  2  Series1

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• Device Models in EDA Tools
• New Challenges and New Data
  – Complex-IO Devices
  – New Data from Survey
• An Applicable Solution – Macromodeling
• An Industrial Macromodeling Example
Then ….. New Challenges

Complex-IO Devices

Pre-emphasis/De-emphasis

Emphasis (t) = Input (t-1)

Main (+ & -)

TX+ Pad 1000 1000
TX- Pad 0111 0111

Picture from Michael Mirmak's presentation in DesignCon East IBIS Summit 2004
Complex-IO Devices

Self calibrating driver
(Calibrating Output Impedance only)
(For DDR2, when controller in a read cycle, the receiver is terminate)
(50 ohms. The resistor also requires to calibrate at run-time)

Note:
1) PMOS side is not being shown here.

Complex-IO Devices

Driver with Slew Rate Control

Note:
1) For simplicity, Nmos and Pmos are used interchangeable.
2) Independent slew control for Rise and Fall.
Complex-IO Devices

And More to Come … …

As Always for Technologies!!

Where is IBIS?

The Original “Box”

- 1st PCI Chipset (33 MHz)
- 1st Pentium uP (66 MHz)
...and the “Box” did grow

- 1st PCI Chipset (33 MHz)
- IBIS
- 1st Pentium uP (66 MHz)

An increasing amount of Complex IO models are missing the box

Our Mission

IBIS

Solve the issues to widen the box

To do so, we’ll need a good understanding of these Complex IO
The Current Situation

IBIS

What is the format of most of the red dots today?

11 Interviews During December 2004

- All are involved with Complex IO
  - Majority were not CDS users
- Good re-introduction to the issues
- The issues are many
  - and the solutions weren’t clear
- Will use this data to propose solutions
- Most want “industry standard solution”
  - but don’t know how to get there
- So who will lead?
High-Speed PCB Web Surveys

• 64% say that more than 20% of the models they receive are Hspice

![Survey Results Image]

http://www.pcbhighspeed.com/discuss/user/non-frames/surveyresults.asp?surveyid=62

• 69% say that this percentage increased in 2004 over 2003

![Survey Results Image]

http://www.pcbhighspeed.com/discuss/user/non-frames/surveyresults.asp?surveyid=63

HSpice Related Interview Questions

• “Do you want to see [External Model] HSpice?” - all “yes”
  – Half qualified this as a non-optimal short-term solution

  This is actually already happening

• “Do you see HSpice as a long-term solution?” - all “no”
  – Unanimous reason: “it’s too slow”

• As such, also unanimous in need to return to behavioral
What has Happened

- IBIS enjoyed 5 years as THE digital IO model format
- Higher frequencies brought new issues and more skeptics
- Gigabit serial links brought rapid transistor model increase in 2004

What Must Happen

- Enable faster behavioral solutions
Features of Behavioral Solution

1. Fast
2. Protects IP
3. Template based
4. Works in many tools
5. Have links to IC design

What behavioral options exist?

AMS Models – the Positives

• Most interviewed at this point are unfamiliar with AMS
  – When asked if they think AMS can be a good solution:
    3 said “yes”, 3 were hopeful, and 4 were unsure, 1 said no
• The experts list the following positives
  – Standards with documented specs
  – Mathematical freedom
  – Conditionals
  – File IO
  – Flexible language
AMS Models – Issues to Solve

• Unfamiliar in SI world, learning curve exists
  – Must seed with templates / training
• Spec nuances/implementations (as with IBIS)
• Not naturally occurring in IO design
  – This is why transistor-level models get used
• IP protection
  – 3 would encrypt, 2 might, 4 are unsure, 2 would not

Any other solutions?

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• An Applicable Solution – Macromodeling
  – What is Macromodeling and Why
  – Our Experiences
• An Industrial Macromodeling Example
What is MacroModeling and Why?

- **Equation-based macromodeling of LVDS drivers**
  - Flexible methodology
    - no specific assumption on device internal structure (preserve IP)
    - handle drivers with enhanced features (e.g., control circuits)
  - Accurate and efficient macromodel (5-10x speed-up)
  - Straightforward SPICE, VHDL-AMS implementations
  - Ready available also for EDA SI tools via the IBIS multilingual extension

**AMS needs Macromodeling Methodology too !!!**

What Our Experience has Shown

- Spice Macromodeling is everywhere
- Cadence has always had SPICE macromodeling
  - And this has made IBIS keyword support quite simple
- Once we had a central IBIS 2.1 driver element
- All later keywords have been macromodeled around it
- In other words, basic SPICE around a B driver element has handled everything IBIS has added for the last 10+ years
- Template is another **KEY** for Complex-IO Modeling
Macromodel from architecture templates

- Most modern devices are based on known DSP circuit architectures

Match template parameters to Layout model to get an accurate macromodel

Known circuit architecture

Macromodel template with parameters

Behavioral SPICE Solutions

- 2.5 Gbps PCIe SerDes Chipset
- 1.5 Gbps S-ATA SerDes
  - http://www.designcon.com/conference/7-ATA.com
- Differential pass-thru receiver
  - http://www.eds.org/pub/ibis/summits/jan00/telian.zip
- Adjustable FPGA SerDes
- Front-side bus driver, impedance control, SSN, & gate choke effect
- Others under NDA, mostly higher speed SerDes
**SPICE Macromodeling**

- Many tools and users have experience with it
- With template help, model makers are succeeding
- Academia is quite engaged in macromodeling research
  
  - [http://www.spi.uni-hannover.de/2004/presentations/spi04_s08_p02_Stievano.pdf](http://www.spi.uni-hannover.de/2004/presentations/spi04_s08_p02_Stievano.pdf)

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Industry example- Altera Stratix GX

"Altera successfully adapted the MacroModel templates to produce fast and accurate models of our multi-gigabit transceivers. Not only did the resulting model correlate well, it also simulates between 20 to 400 times faster than its transistor-level counterpart. And the model can be easily adjusted to match the behaviors of actual silicon measured in the lab."

"Overall, the templates were simple to work with and very valuable amidst the challenges of multi-gigahertz design."

Correlation - Altera Stratix GX

- Transistor Level Model (HSpice)
- Spice Macromodel (Cadence DML)

Transmitter output at factor=5
And, the latest news

- Driver Schedule in IBIS for 4 tap pre-emphasis buffer is working