First steps with [External Model] in IBIS
Overview

- Motivation
- Syntax [External Model]
  - (H)Spice
  - VHDL-AMS (Verilog-A)
- Experiences with Model-Application Pos/Neg
  - (H)SPICE
  - VHDL-AMS
- Summary & Conclusions
Motivation

- HSpice/VHDL-AMS
  - is more accurate in a wider range than ibis (PVT)
  - will be part of the Com simulation flow (HSpice stand alone without additional parameters)
  - describes devices/features which ibis could not (Pre-Emphasis, ODT, SSN, analog parts)
- No ibis available, but hspice/vhdl-ams (no conversion effort to do)
Syntax of [External Model] ((H)Spice)

[Model] AMI5HS-ICX_ODTXXE04-4P0_BI
Model_type I/O

[External Model]
language (H)SPICE

corner typ spicelib/ami500hxpr.typ.hsp ODTE04
corner min spicelib/ami500hxpr.min.hsp ODTE04
corner max spicelib/ami500hxpr.max.hsp ODTE04

|.subckt ODTE04 io int_in en vcc gnd
ports A_signal A_drive A_enable A_puref A_gnd
D_to_A D_drive A_drive A_gnd 0 5 1n 1n
D_to_A D_enable A_enable A_gnd 0 5 1n 1n
A_to_D D_receive A_signal A_gnd 0.8 2

| Parameters - Not supported in SPICE

[End External Model]

[Model Spec]

Vinl 0.899000V 0.800000V 0.932000V
Vinh 1.901000V 1.868000V 2.000000V

[Voltage Range] 5.0V 4.75V 5.25V

[Ramp] (für Primitiv-tools)
**Syntax of [External Model] (VHDL-AMS)**

**[Model]**
AMI5HS-ICX_OTXSE04-4P0_BI

**Model_type**
I/O

**[External Model]**

**language VHDL-AMS**

**corner typ**
IBIS_basic_OUT.vhd IBIS_OUT

```
| port (signal In_D : in std_logic;
|     terminal OUTPUT : electrical;
|     terminal PC_ref : electrical;
|     terminal PU_ref : electrical;
|     terminal PD_ref : electrical;
|     terminal GC_ref : electrical);
```

**ports**
D_drive A_signal A_pcref A_puref A_pdref A_gcref

**Parameter**
abc xyz

**[End External Model]**

**[Model Spec]**

**Vin**
0.899000V 0.800000V 0.932000V

**Vinh**
1.901000V 1.868000V 2.000000V

**[Voltage Range]**
5.0V 4.75V 5.25V

**[Power Clamp Reference]**
5.0V 4.75V 5.25V

**[Ramp]**
(H)Spice-Experiences with [External Model]

- **POS**
  - only one work environment for critical nets (ICX)
  - good availability of HSpice (ICX)
  - helpfull additional Parameter in ibis required:
    - Vinh, Vinl (as appropriate to Model_type)

- **NEG**
  - Berkley spice models very rare
  - NDA for different library users
  - complex library management: additional path reference required (ICX)
  - temperature always default 25°C (requirement for program)
  - no [Series] Models possible
  - enable active low/high not switchable include inverter (ICX)
VHDL-AMS-Experiences with [External Model]

- **POS**
  - large template collection in Macro Model Library
  - very flexible (user can change models himself)
    - logical combinations: if then else (ODT)
    - SSN (feature not yet in ibis/program)
  - faster than (H)Spice
  - modelling of analog/passive components

- **NEG**
  - very few models from vendors
    - Altera Stratix GX AMS SI kit, Intel ICH8 SI, Xilinx V2 Pro, and V2 Pro X Beta
  - program bugs (ICX, SystemVision, SMASH)
  - no temperature value used
  - no [Series] Models possible
  - no simple parser available
Summary and Conclusion

- Simulation time increased in comparison to IBIS
- HSpice/VHDL-AMS should be used only for special/critical signals
- VHDL-AMS problems with availability of models and successful operating of programs
- Library structure major changes with [External Model]
  - different simulation programs require different model formats (Model Selector)
  - new quality check algorithm