SSO Simulation with IBIS

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Overview

- Motivation
- SSN with IBIS in 2000
  - Simulation setup
  - BEHAVIOR – model with Voltage-Controlled Current Sources
  - very good concordance with transistor based models
- Table driven kssn-multiplier
  - Multiplier extraction
  - Results HSPICE vs. VCCS-BEHAVIOR
  - Lacking concordance
- Enhanced VCCS-BEHAVIOR
  - Additional RC – Timing coefficient
  - Improved results
- Summary
Acknowledgements

INFINEON TECHNOLOGIES
- HYB18T512160AF
- DDR2 - Memory

TEXAS INSTRUMENTS
- CDCE706
- PROGRAMMABLE 3-PLL CLOCK SYNTHESIZER / MULTIPLIER / DIVIDER
SSO Simulation Setup
(m+1 switching outputs)

**Overview**

**SSN 2000**

**kssn - table**

**Enhanced VCCS model**

**Summary**

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VCCS-Model enhancement

- A second multiplier for rising \((kssnr)\) and falling \((kssnf)\) edges
- Both multipliers are controlled by the \((Vdd-Vss)\) voltage drop
- Feedback on the *gate source voltage of the output transistors*
- Multiplier generation:
  - Pullup/down V/I-tables as a function of Vdd
  - SSO-V/t-table (Golden Waveform)
VCX16244 SSN analysis results (rising edge)
Enhanced two waveform behavioral model Number of SSO = 6

Overview

SSN 2000

kssn - table

Enhanced VCCS model

Summary

Node OUT: Transistor based Behavioral

Node END: Transistor based Behavioral
kssnr/f Multiplier Generation Method

Overview
SSN 2000
kssn - table
Enhanced VCCS model
Summary

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Overview

SSN 2000

kssn - table

Enhanced VCCS model

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kssn rising coefficient extraction
HYB18T512160AF (DDR2) INFINEON

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kssn falling coefficient extraction
HYB18T512160AF (DDR2) INFINEON

Overview
SSN 2000
kssn - table
Enhanced VCCS model
Summary

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Overview

SSN 2000

kssn - table

Enhanced VCCS model

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kssn falling coefficient extraction (zoom)
HYB18T512160AF (DDR2) INFINEON
Overview

SSN 2000

kssn - table

Enhanced VCCS model

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HYB18T512160AF / INFINEON

kssn rising/falling @ Vdd = 0.5V to 3.6V (1.8V nom.)

Vdd_nom

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TI CDCE706  TEXAS INSTRUMENTS  
kssn rising/falling @ Vdd = 0.5V to 5V (3.3V nom.)

Overview

SSN 2000

kssn - table

Enhanced VCCS model

Summary

Vdd_nom

slew rate max

slew rate min

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SSN 2000

Enhanced VCCS model

Overview

Summary

DDR2 buffer Infineon
Supply voltage drop (L=2x1nH) / Load Tline Zo=50 Ohm

IBIS

VCCS + kssn

Transistor based

w/ pkg

w/o pkg

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Overview

SSN 2000

kssn - table

Enhanced VCCS model

Summary

TI CDCE706 / Voltage drop / Rising edge
VCCS-model with kssn table (L=2x3nH)

transistor based model
VCCS + kssn

IBIS / HSPICE @ NO PKG

VCCS + kssn

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**Overview**

**SSN 2000**

**kssn - table**

**Enhanced VCCS model**

**Summary**

**TI CDCE706 Rising edge vs. Vdd drop**

**Transistor based model**

![Graph showing rising edge vs. Vdd drop for TI CDCE706](image)

**Vdd=3.3V**

**Vdd drop**

L=1nH ... 9nH

**Sig.@Vdd=3.3V**

**Sig.@Vdd drop**

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Overview

SSN 2000

kssn - table

Enhanced VCCS model

Summary

**TI CDCE706** Falling edge vs. Vdd drop
Transistor based model

Vdd drop
L=1nH ...9nH

Vdd=3.3V

Sig.@Vdd drop

Sig.@Vdd=3.3V
## Differences: VCCS 2000 vs. 2006

<table>
<thead>
<tr>
<th></th>
<th>VCCS 2000</th>
<th>VCCS 2006</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transition Time</td>
<td>ca. 5ns</td>
<td>&lt;500ps</td>
</tr>
<tr>
<td>Operation Point</td>
<td>saturation region</td>
<td>linear region</td>
</tr>
<tr>
<td>Vdd/GND drop</td>
<td></td>
<td></td>
</tr>
<tr>
<td>amplitude</td>
<td>ca. 15% Vdd</td>
<td>ca. 40% Vdd</td>
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<tr>
<td>width</td>
<td>ca. 7ns</td>
<td>ca. 1ns</td>
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<tr>
<td>Design of the OUTPUT stage</td>
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<tr>
<td>Time domains</td>
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<td>YES</td>
</tr>
<tr>
<td>Slew rate control</td>
<td>NO/YES</td>
<td>YES</td>
</tr>
<tr>
<td>Vdd-drop Feed back</td>
<td>NO</td>
<td>YES</td>
</tr>
<tr>
<td>Prestage @Vdd_int</td>
<td>NO/YES</td>
<td>YES</td>
</tr>
<tr>
<td>On-die capacitance</td>
<td>NO</td>
<td>YES</td>
</tr>
</tbody>
</table>

**Overview**

- SSN 2000
- Enhanced VCCS model
- Summary
Improvement with prestage capacitance $C_{pre}$

- $k_{ssnr}(V_{dd}-V_{ss}) \cdot k_{pu}(t) \cdot I_{pu}(V_{out})$
- $k_{ssnf}(V_{dd}-V_{ss}) \cdot k_{pd}(t) \cdot I_{pd}(V_{out})$

$C_{pre}$: Vdd-Vss prestage Capacitance

Evaluation:
SPICE simulation using a capacitance bridge

Overview

SSN 2000

kssn - table

Enhanced VCCS model

Summary
Vdd drop improvement with $C_{pre}=30\,pF$

$CDCE706$ with $PKG\ L=2\times3\,nH$ 10 SSO
Vdd drop improvement with $C_{pre}=30\,\text{pF}$

CDCE706 with PKG $L=2\times3\,\text{nH}$ 10 SSO
Enhanced VCCS-Behavior Model with kssn (static) and td_RC (dynamic) coefficients

Enhanced VCCS-Behavior Model
with kssn (static) and td_RC (dynamic) coefficients

- by optimisation through the Vdd_drop @ known L
- by adjustment from I=I(t) table @ L
Vdd drop improvement
DDR2 with PKG L=2x3nH  5 SSO

Overview

SSN 2000

kssn - table

Enhanced VCCS model

Summary
Vdd drop improvement
CDCE706 with PKG L=2x3nH 10 SSO

Overview

SSN 2000

kssn - table

Enhanced VCCS model

Summary
Summary

- With improved IBIS models, SSO can be simulated in a better concordance with transistor based models, IF
  - kssn – table information (BIRD 97.x)
  - current vs. time tables @ known RLC environment (BIRD 95)

- Advantages
  - Signal integrity analysis
    - PDS – Voltage drop
    - Timing simulation

- More investigations have to be done, to evaluate for different technologies, the validity range and the accuracy of the proposed improvement
SSO Simulation with IBIS

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Questions